SemiMod GmbH

REPORT

Topic: SG13G2 MOSFET Model Library in Ngspice - Sanity Check

Author 1   Markus Müller

Author 2   Mario Krattenmacher

Contact: markus.mueller@semimod.de

Contents

1 Introduction

This document shows several **simulated** MOSFET characteristics for the open-source IHP SG13G2 process. The code for generating this document is available on Gitlab and maintained by SemiMod GmbH. The document is automatically generated using the DMT-core, DMT-extraction and Pylatex packages. The transistor width used for normalization of currents is given in the section headings.

2 IHP SG13G2 PSP NMOS $w = 0.35\,\mu\text{m}$ $l = 0.13\,\mu\text{m}$ Sanity Checks

This section gives an overview of the DC Characteristics of the transistor. Next, some DC characteristics @$T = 300\,\text{K}$ are visualized.
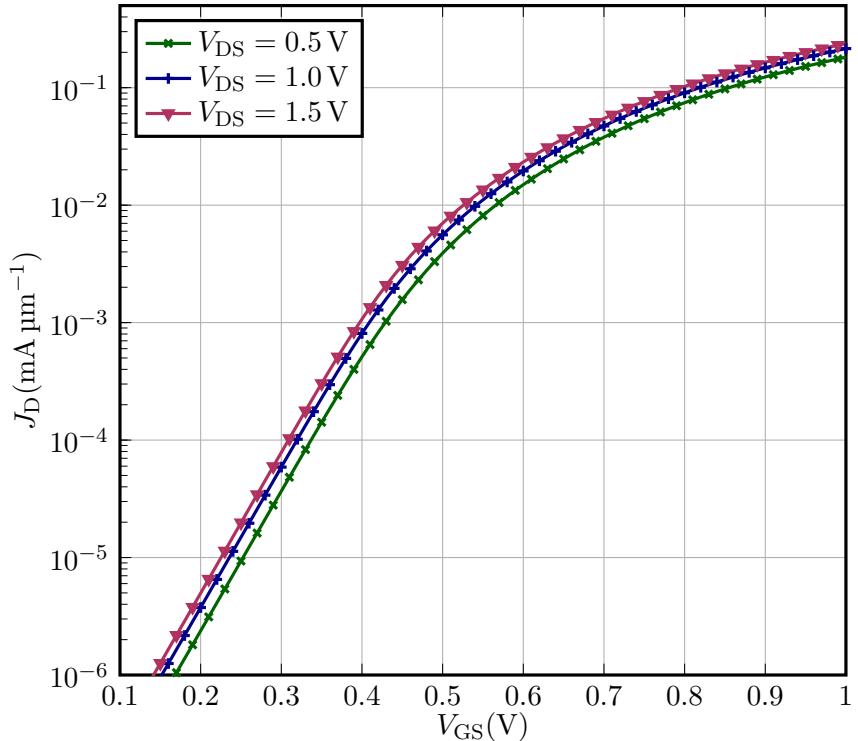

Figure 1: $J_\text{D}(V_\text{GS})$ at V_DS and $T = 300\,\text{K}$.
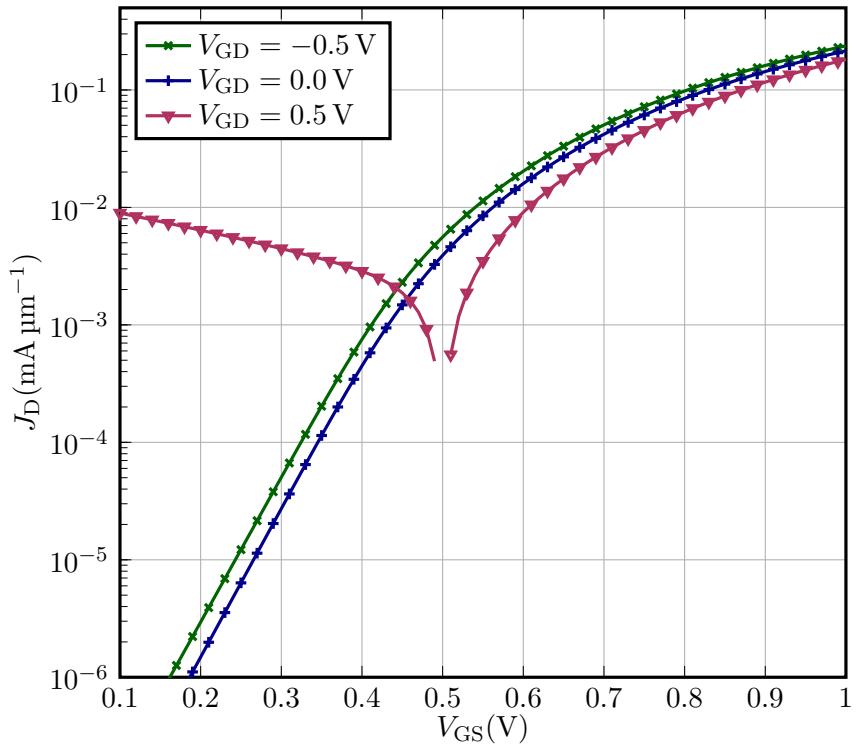
Figure 2: $J_{\mathrm{D}}(V_{\mathrm{GS}})$ at V_{BC} and $T = 300\,\mathrm{K}$.
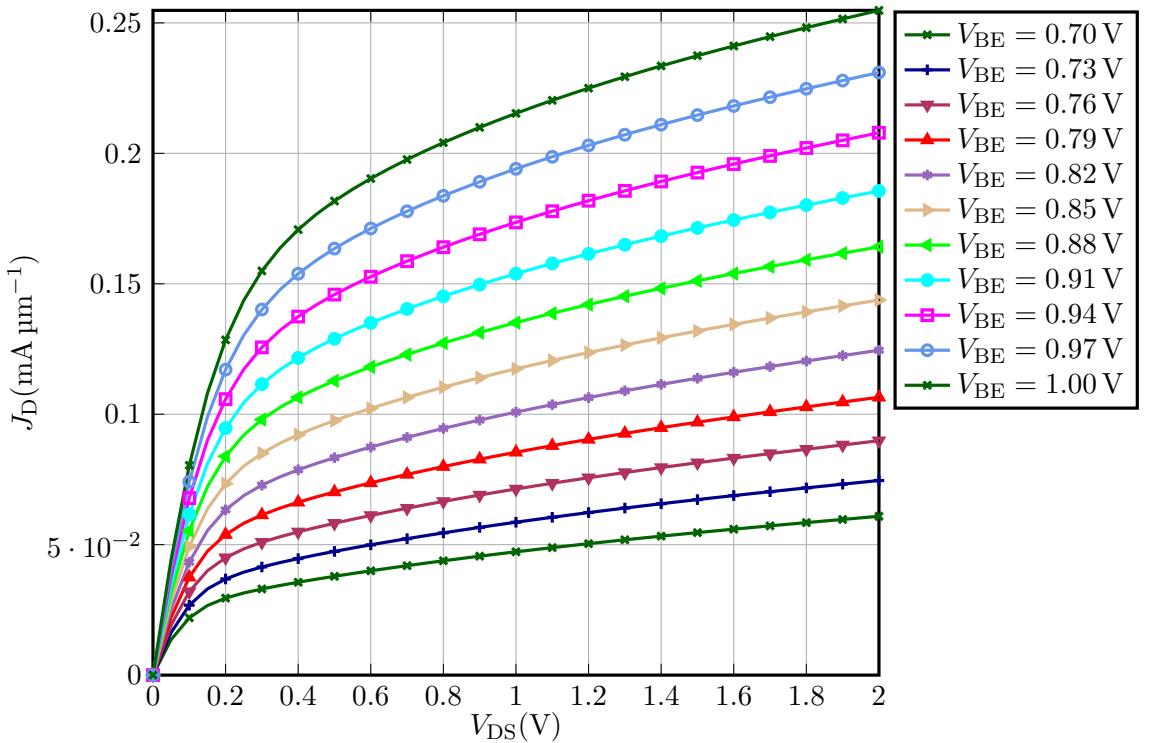
Figure 3: $J_{\mathrm{D}}(V_{\mathrm{DS}})$ at V_{GS} and $T = 300\,\mathrm{K}$.

Next, some AC characteristics @$T = 300\,\mathrm{K}$ are visualized.
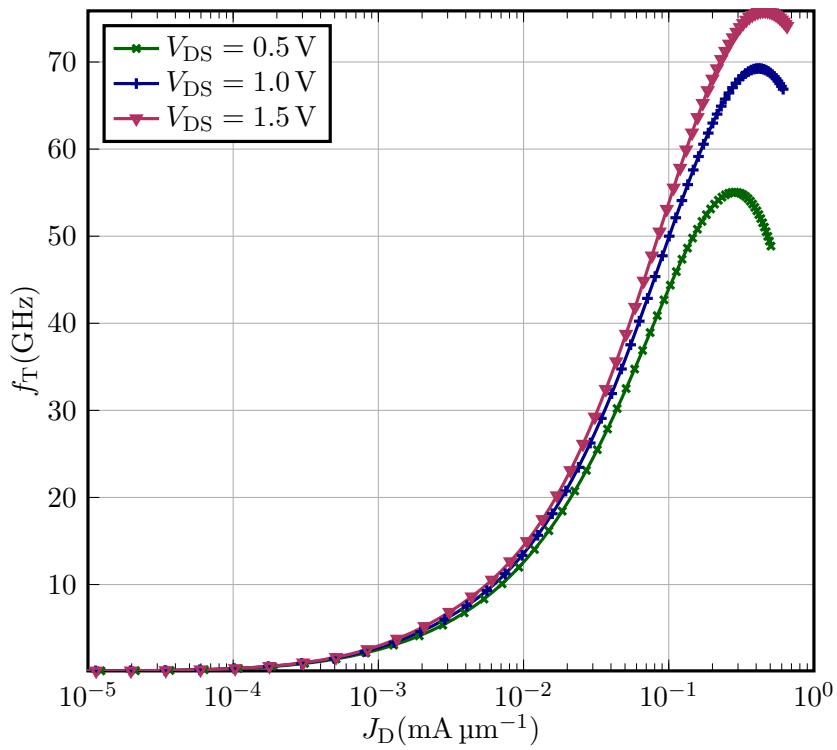
Figure 4: $f_{\mathrm{T}}(J_{\mathrm{D}})$ at V_{DS} and $T = 300\,\mathrm{K}$.
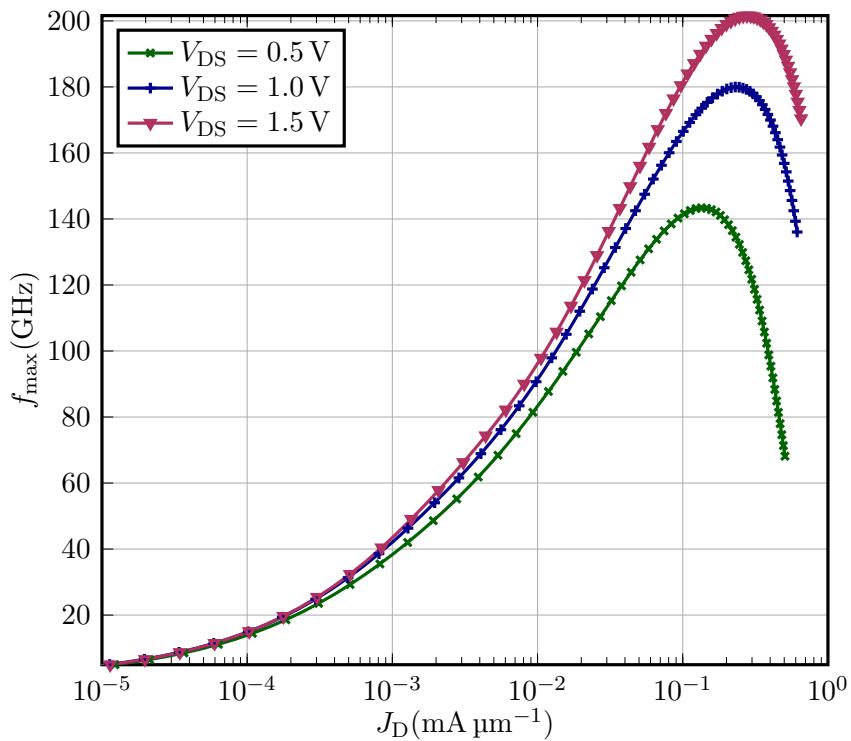
Figure 5: $f_{\mathrm{max}}(J_{\mathrm{D}})$ at V_{DS} and $T = 300\,\mathrm{K}$.

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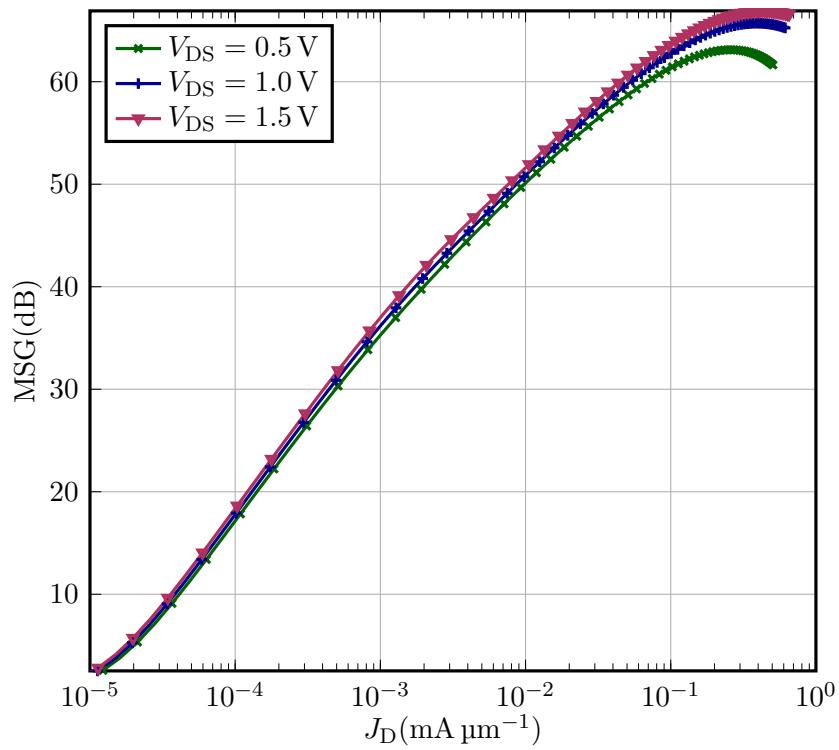
Figure 6: MSG(J_D) at V_DS and $T = 300\,\mathrm{K}$.
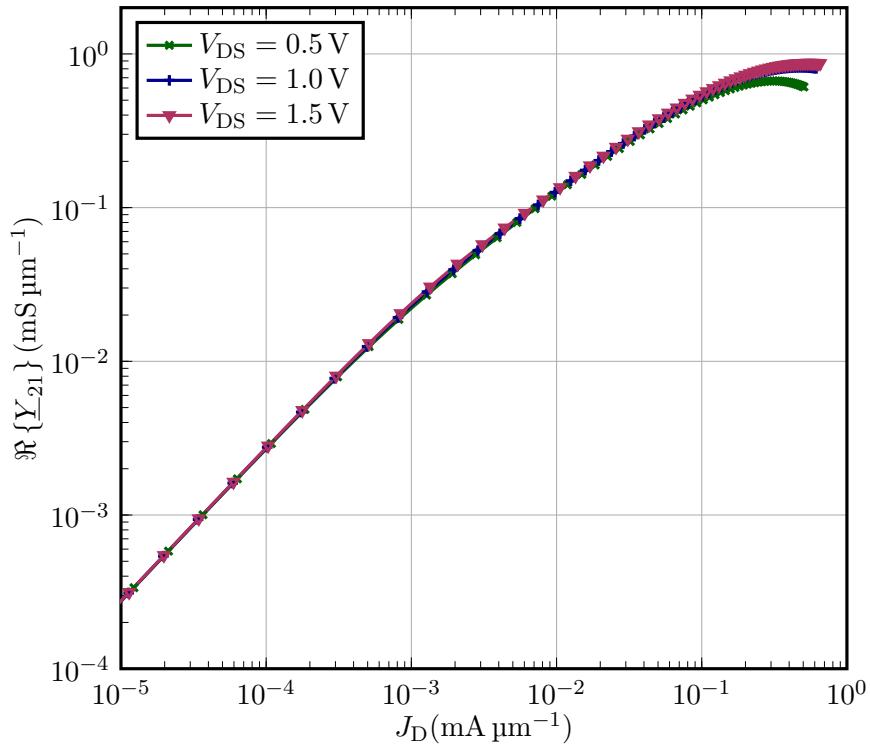
Figure 7: $\Re\left\{\underline{Y}_{21}\right\}(J_\mathrm{D})$ at V_DS and $T = 300\,\mathrm{K}$.

Next, some characteristics at different T and $V_\mathrm{DS} = 1.5\,\mathrm{V}$ are visualized.
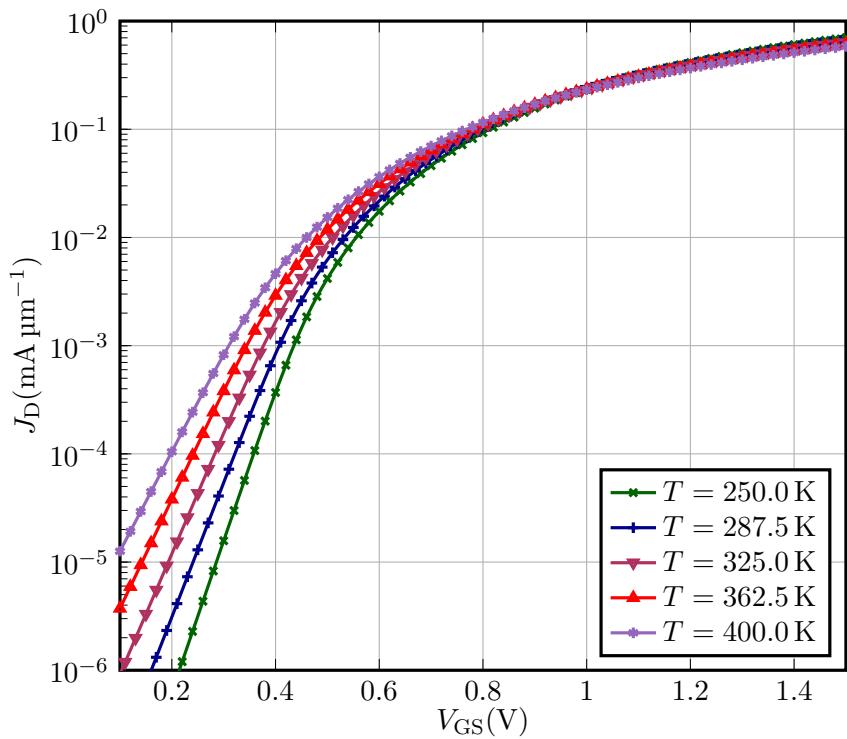
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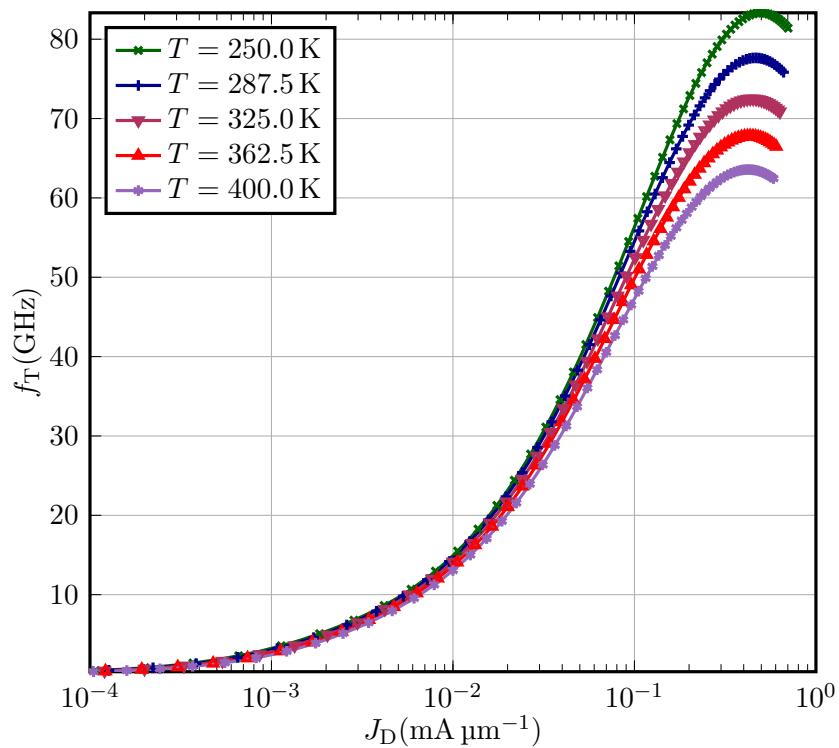
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3 IHP SG13G2 PSP NMOS $w = 0.90\,\mu\mathrm{m}$ $l = 0.13\,\mu\mathrm{m}$ Sanity Checks

This section gives an overview of the DC Characteristics of the transistor. Next, some DC characteristics @$T = 300\,\mathrm{K}$ are visualized.
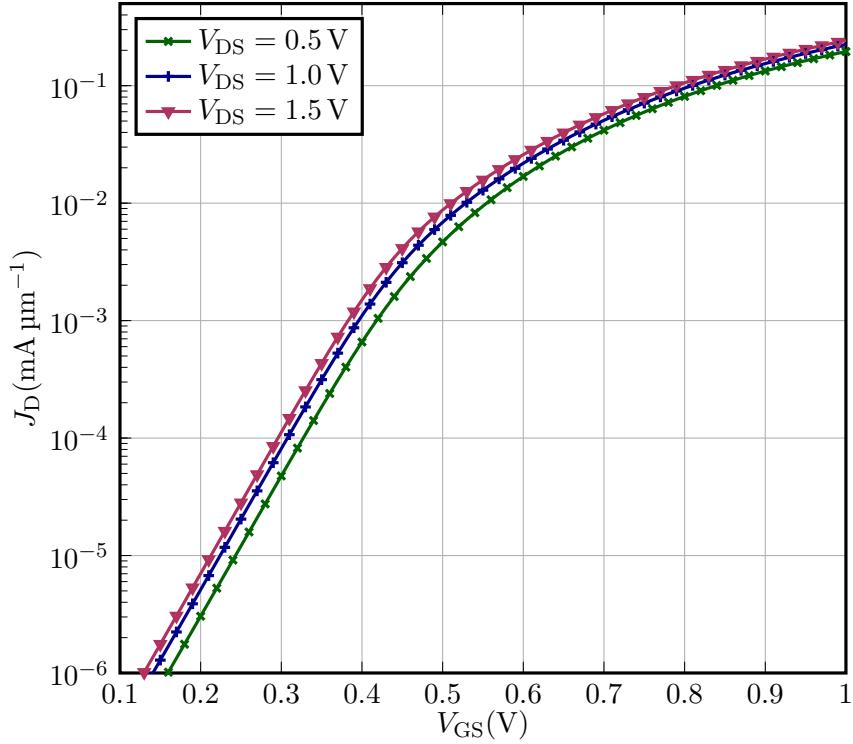

Figure 10: $J_\mathrm{D}(V_\mathrm{GS})$ at V_DS and $T = 300\,\mathrm{K}$.
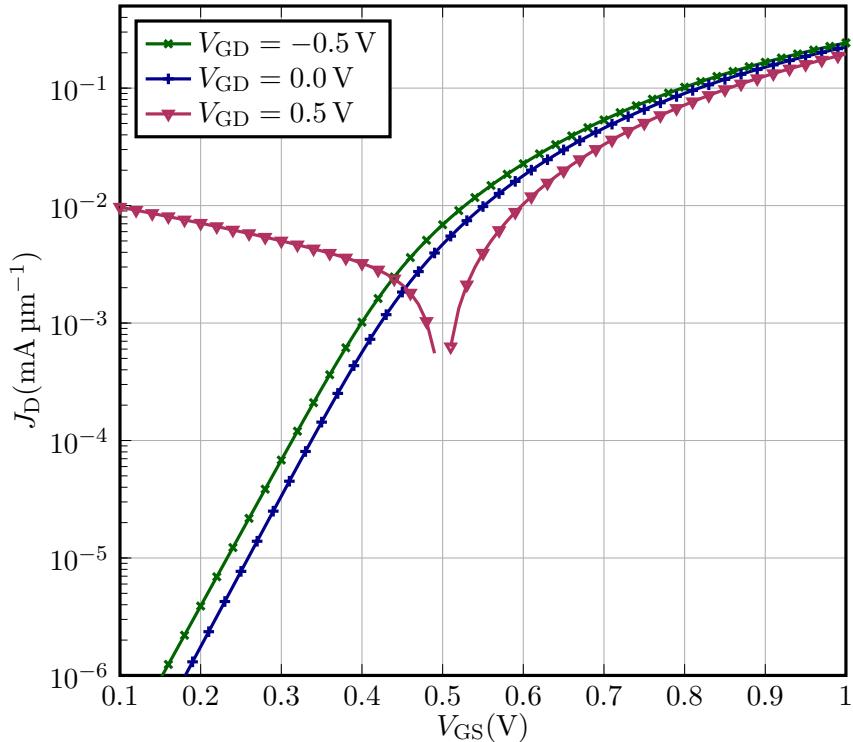
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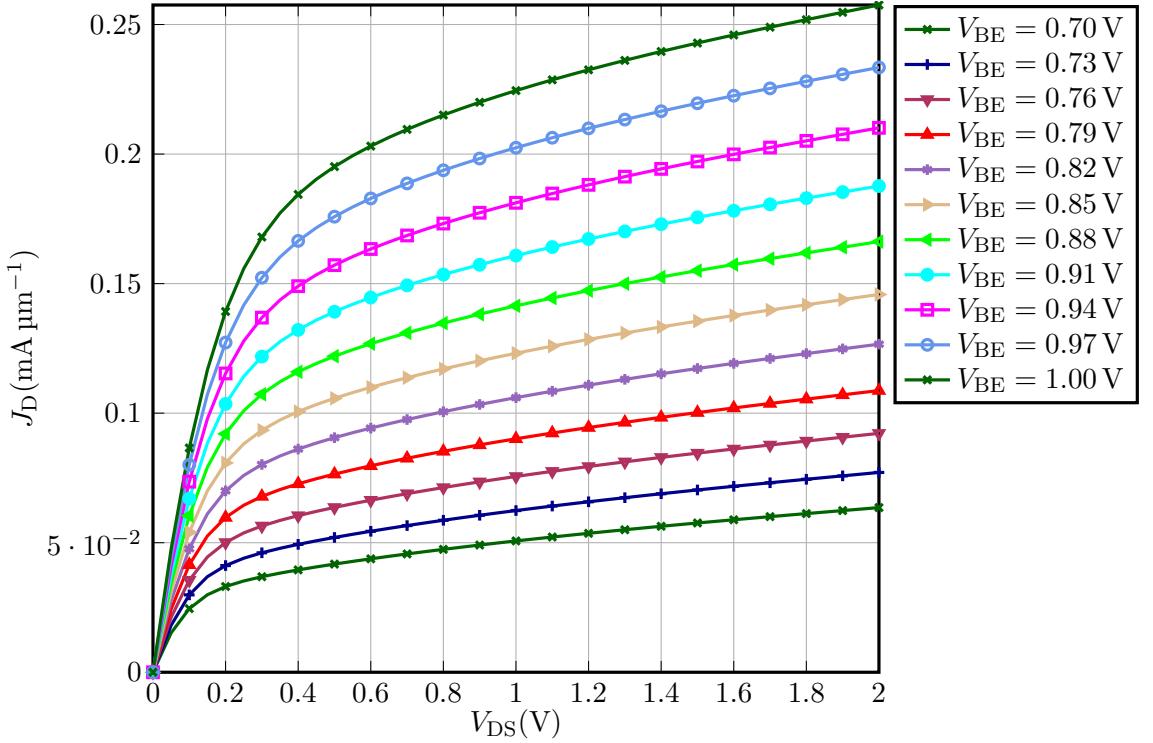
Figure 12: $J_{\mathrm{D}}(V_{\mathrm{DS}})$ at V_{GS} and $T = 300\,\mathrm{K}$.

Next, some AC characteristics @$T = 300\,\mathrm{K}$ are visualized.
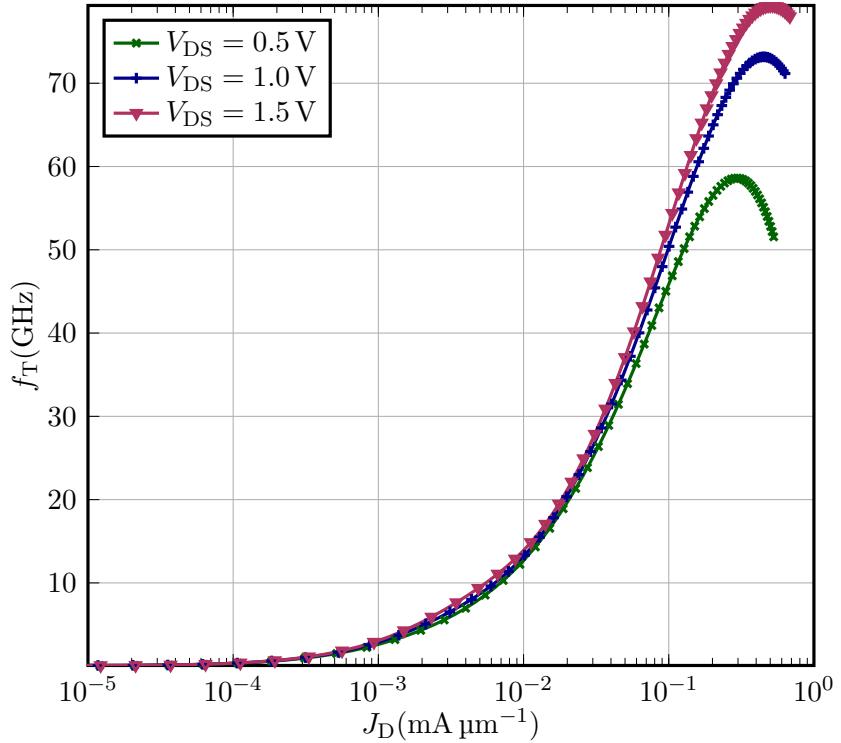
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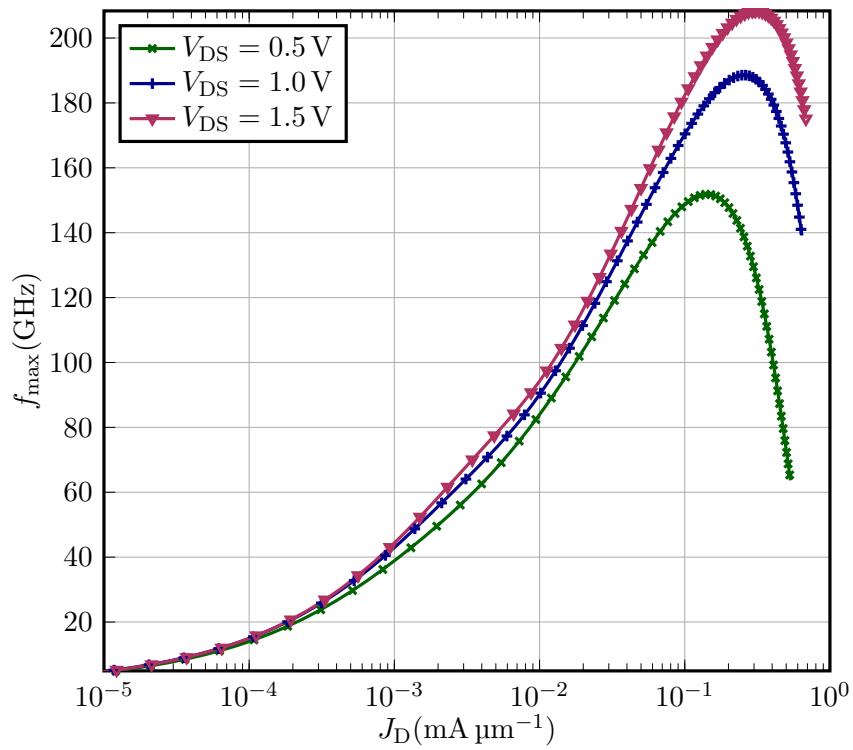
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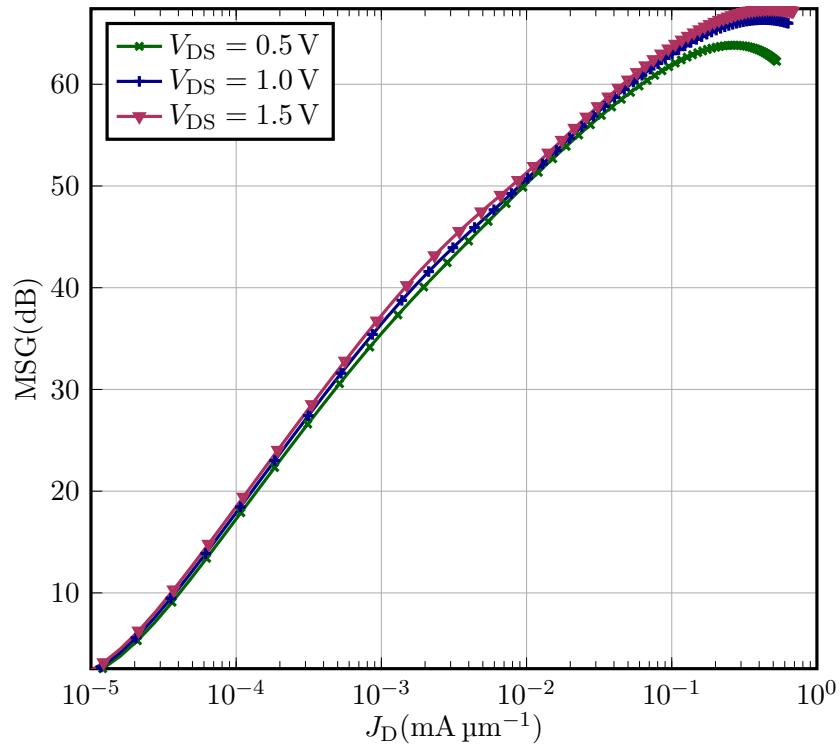
Figure 15: MSG(J_{D}) at V_{DS} and $T = 300\,\mathrm{K}$.
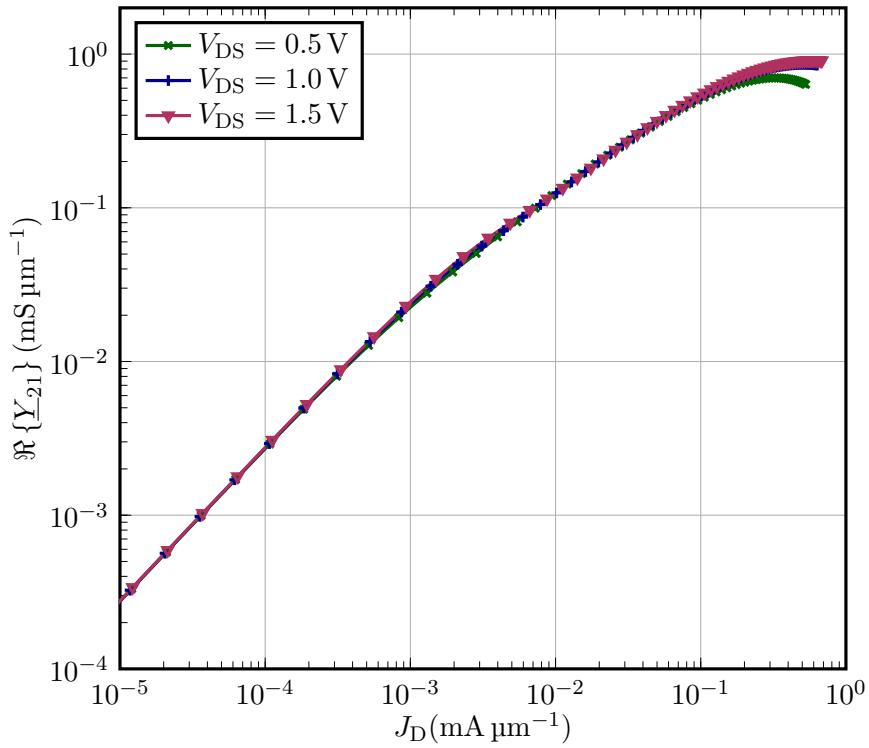
Figure 16: $\Re\{\underline{Y}_{21}\}(J_D)$ at V_{DS} and $T = 300\,\text{K}$.

Next, some characteristics at different T and $V_{DS} = 1.5\,\text{V}$ are visualized.
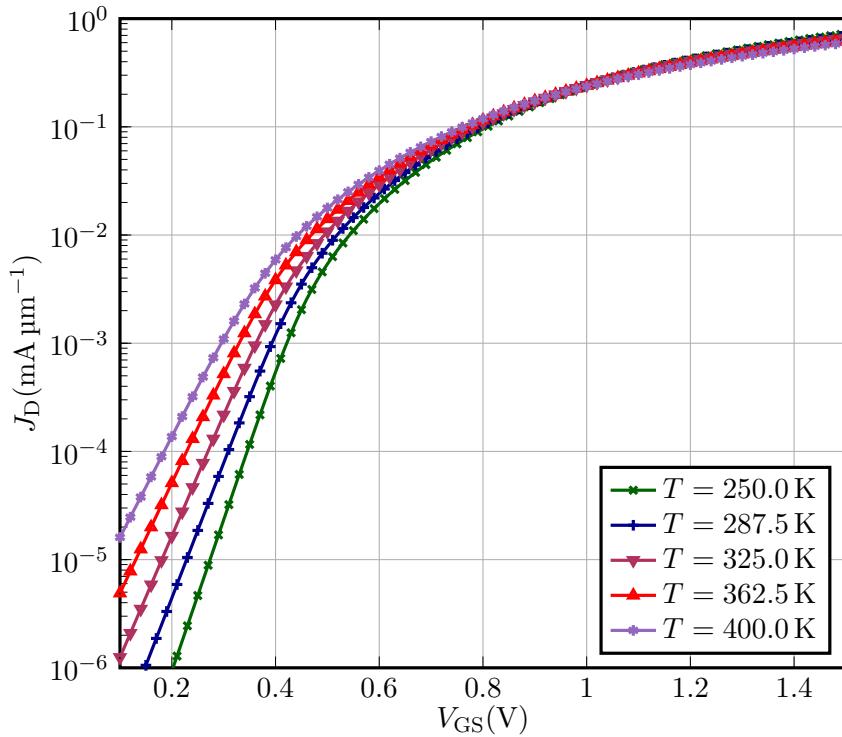

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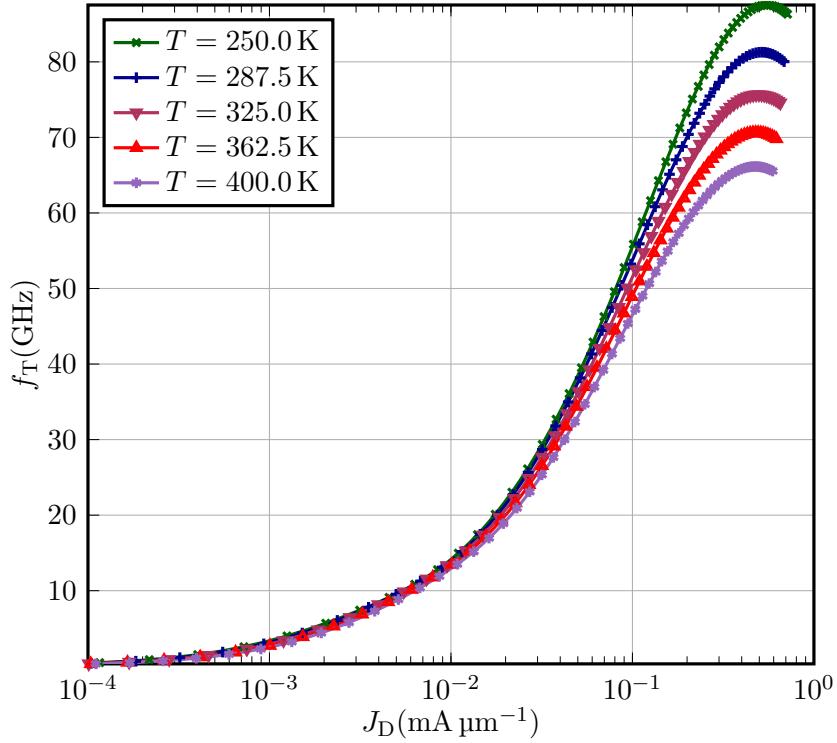
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4 IHP SG13G2 PSP NMOS $w = 0.35\,\mu\mathrm{m}$ $l = 0.25\,\mu\mathrm{m}$ Sanity Checks

This section gives an overview of the DC Characteristics of the transistor. Next, some DC characteristics @$T = 300\,\mathrm{K}$ are visualized.
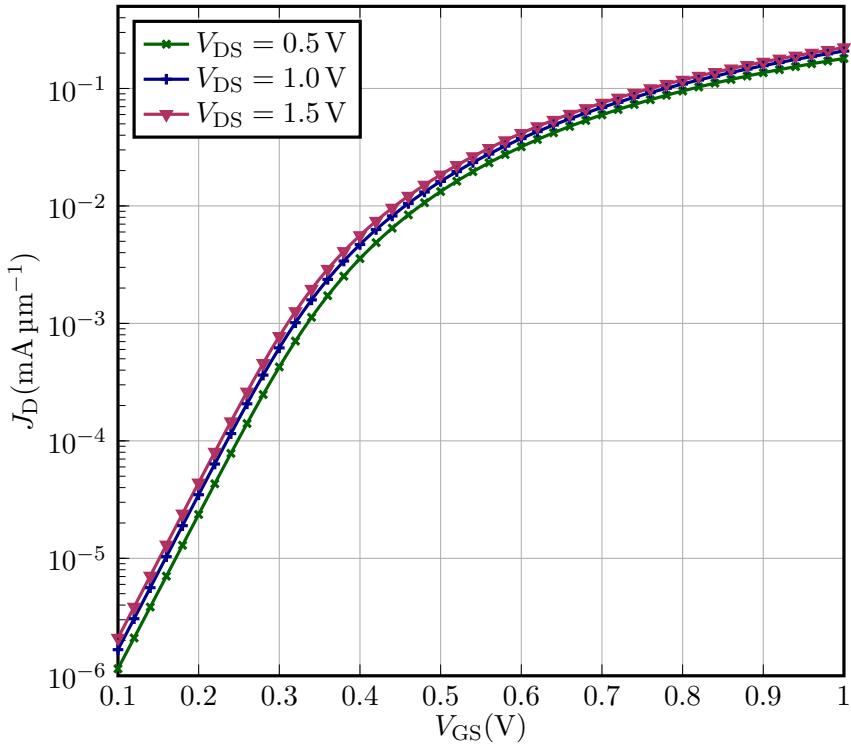

Figure 19: $J_{\mathrm{D}}(V_{\mathrm{GS}})$ at V_{DS} and $T = 300\,\mathrm{K}$.

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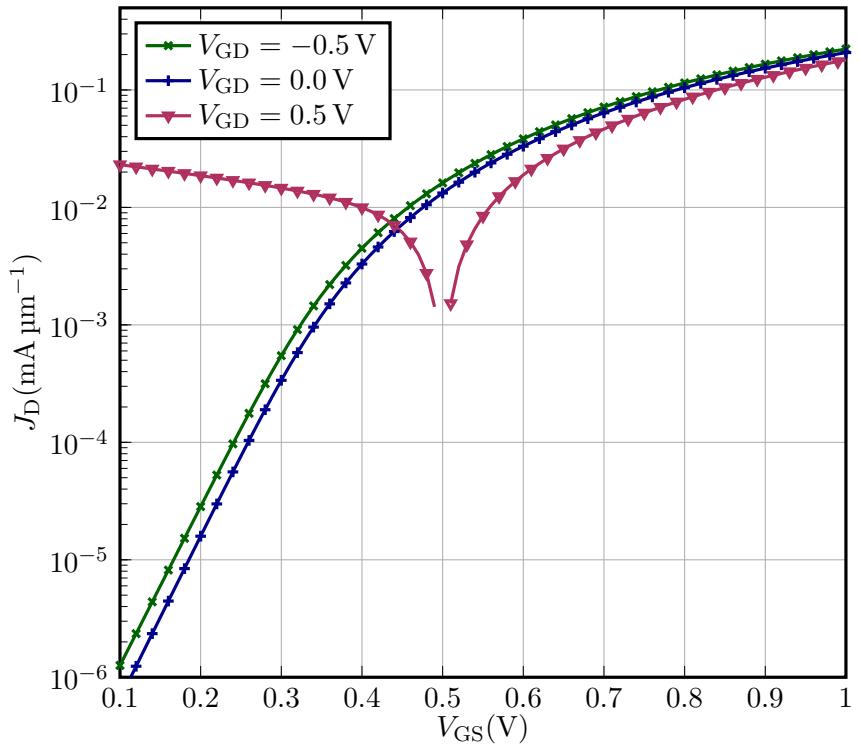
Figure 20: $J_D(V_{GS})$ at V_{BC} and $T = 300\,\mathrm{K}$.
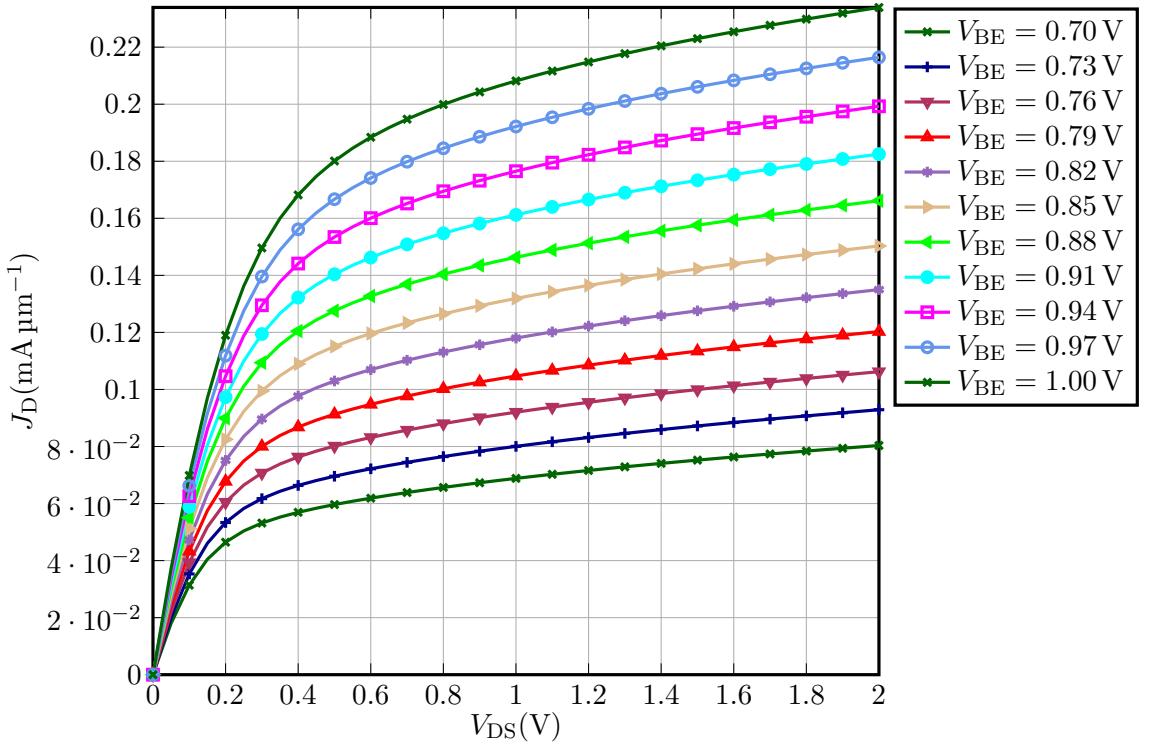
Figure 21: $J_D(V_{DS})$ at V_{GS} and $T = 300\,\mathrm{K}$.

Next, some AC characteristics @$T = 300\,\mathrm{K}$ are visualized.
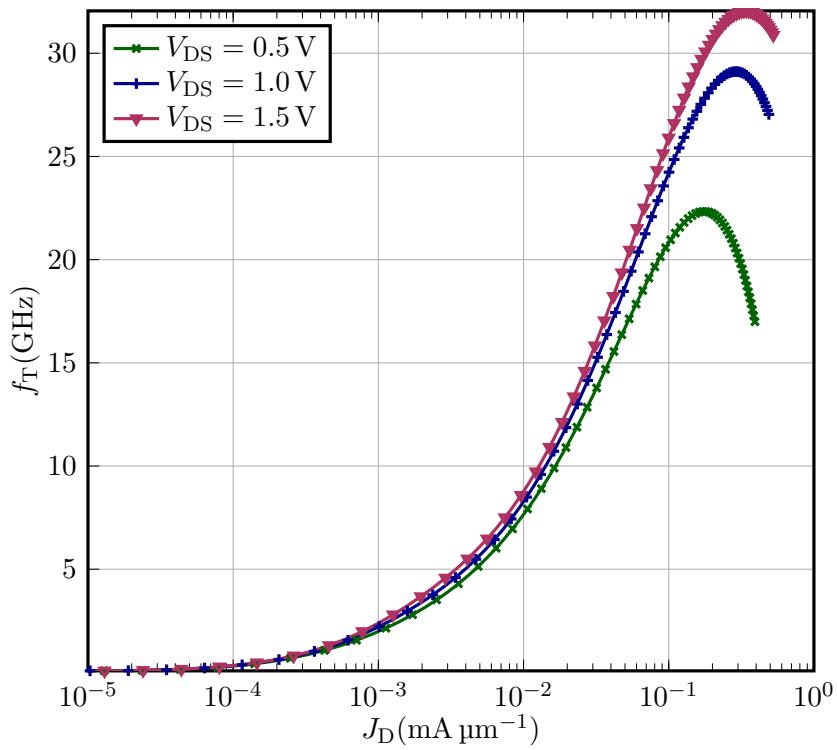
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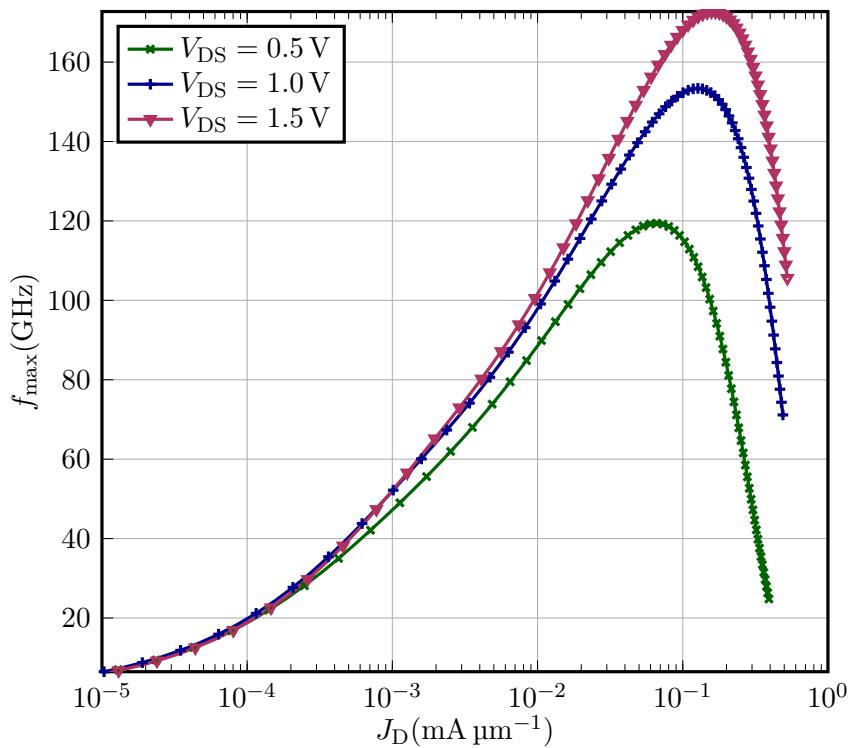
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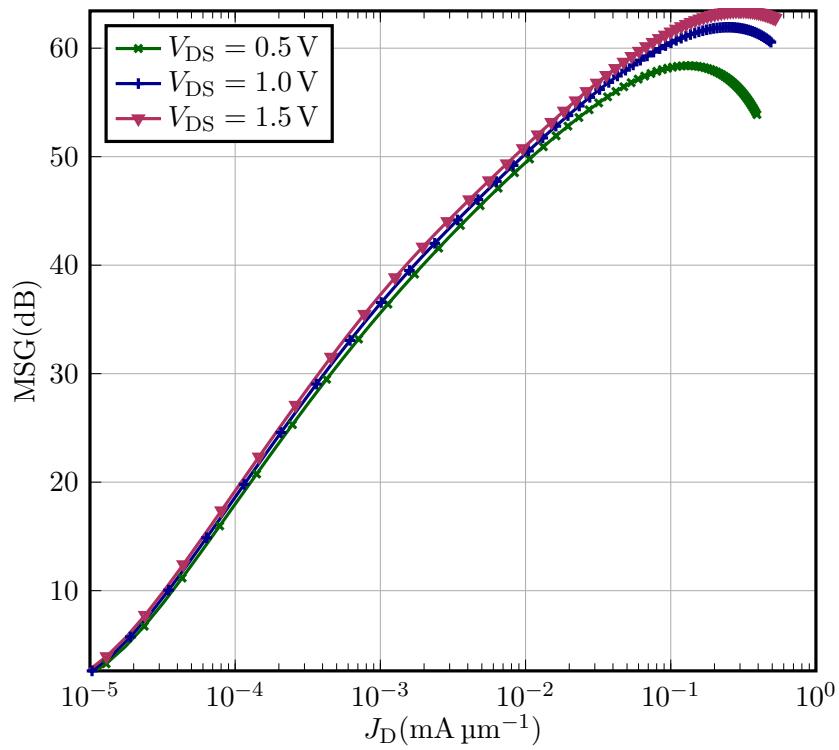
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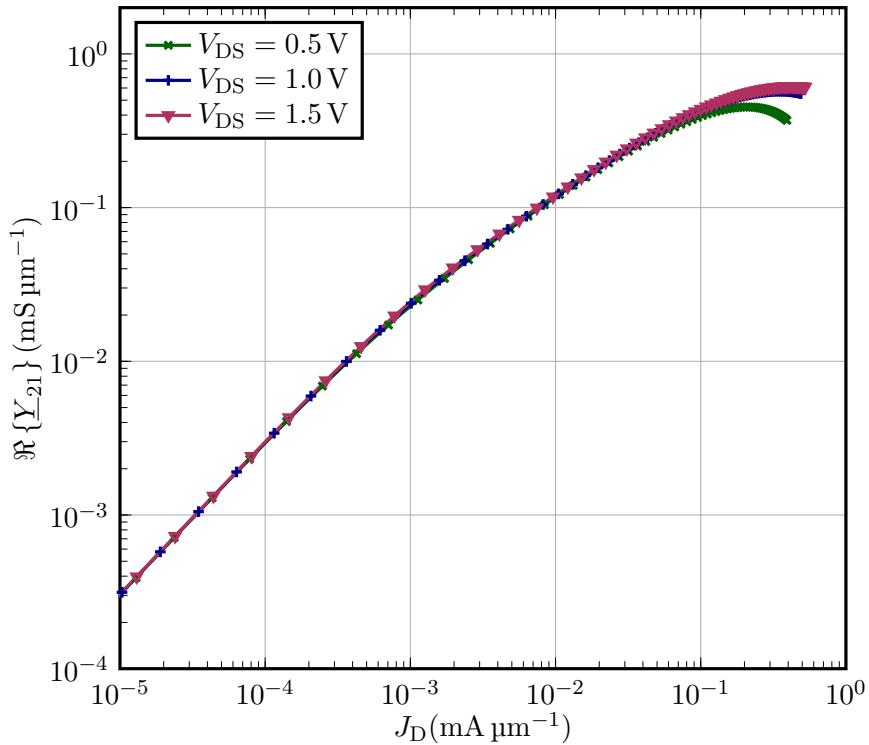
Figure 25: $\Re\left\{\underline{Y}_{21}\right\}(J_\mathrm{D})$ at V_DS and $T = 300\,\mathrm{K}$.

Next, some characteristics at different T and $V_\mathrm{DS} = 1.5\,\mathrm{V}$ are visualized.
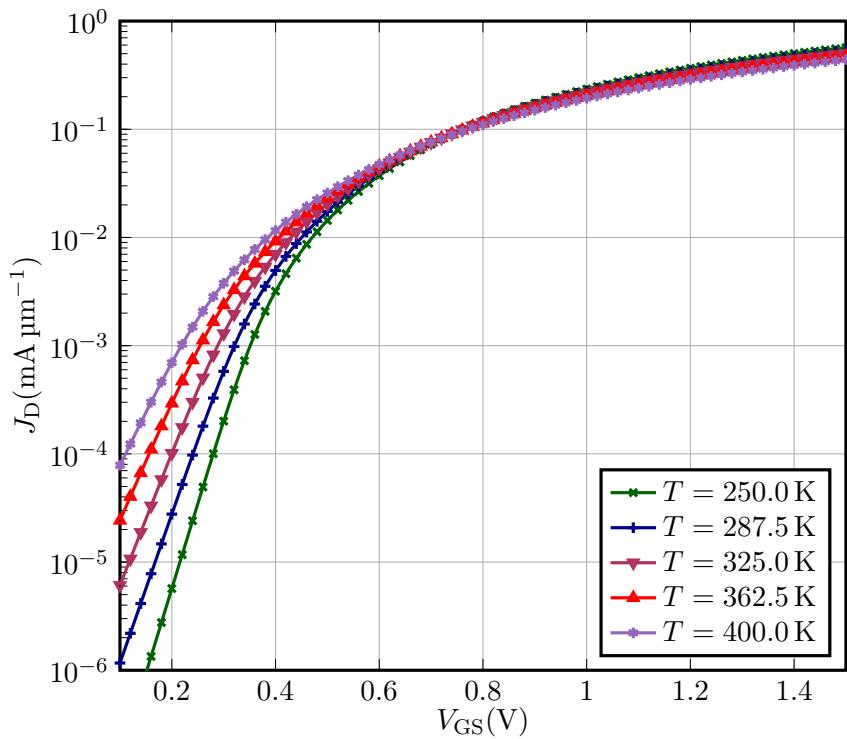
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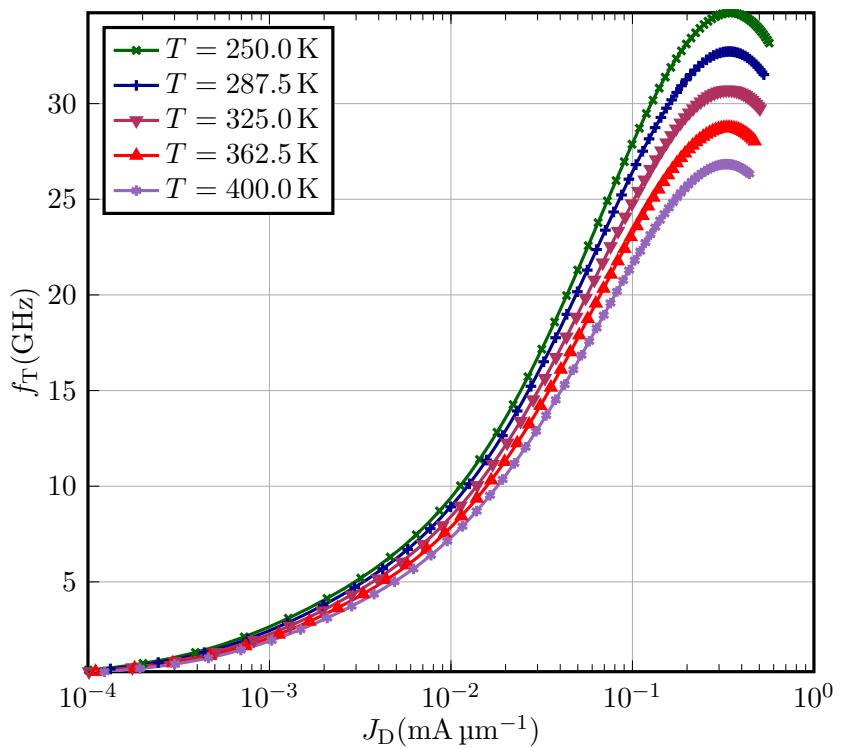
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5 IHP SG13G2 PSP PMOS $w = 0.35\,\mu\mathrm{m}$ $l = 0.13\,\mu\mathrm{m}$ Sanity Checks

This section gives an overview of the DC Characteristics of the transistor. Next, some DC characteristics @$T = 300\,\mathrm{K}$ are visualized.
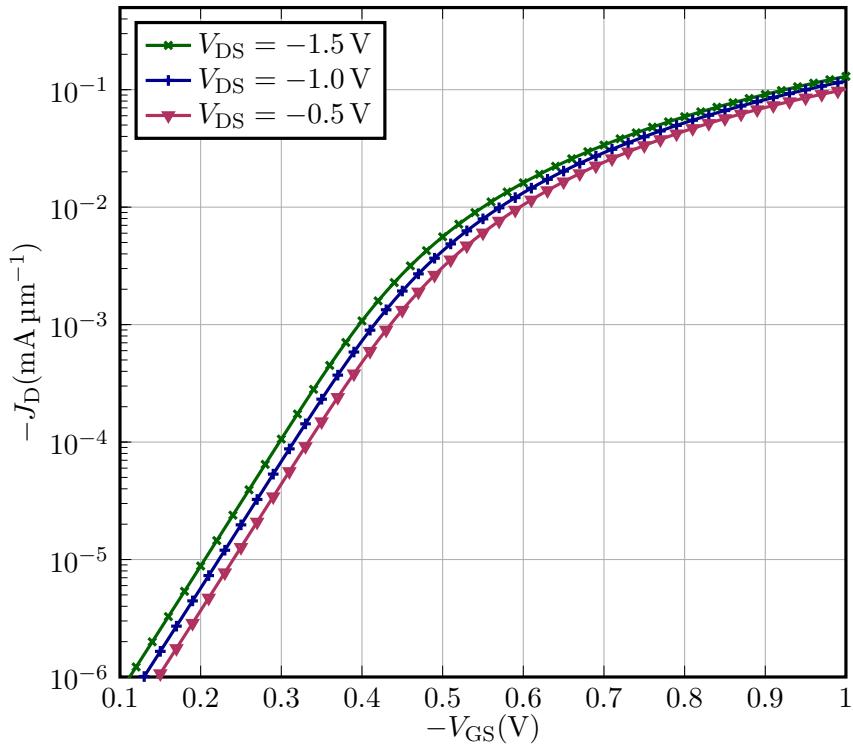

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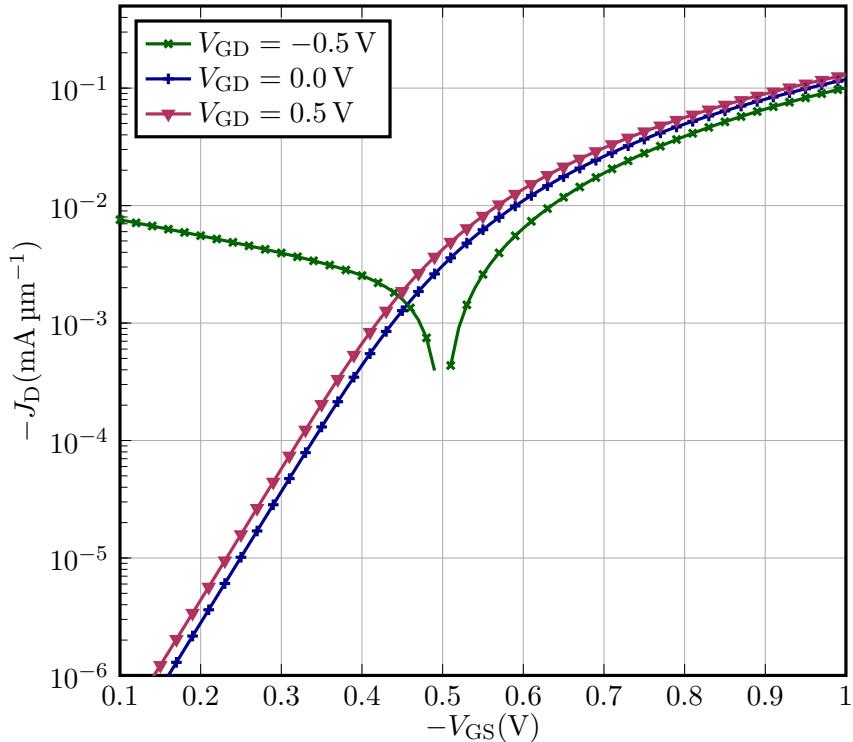
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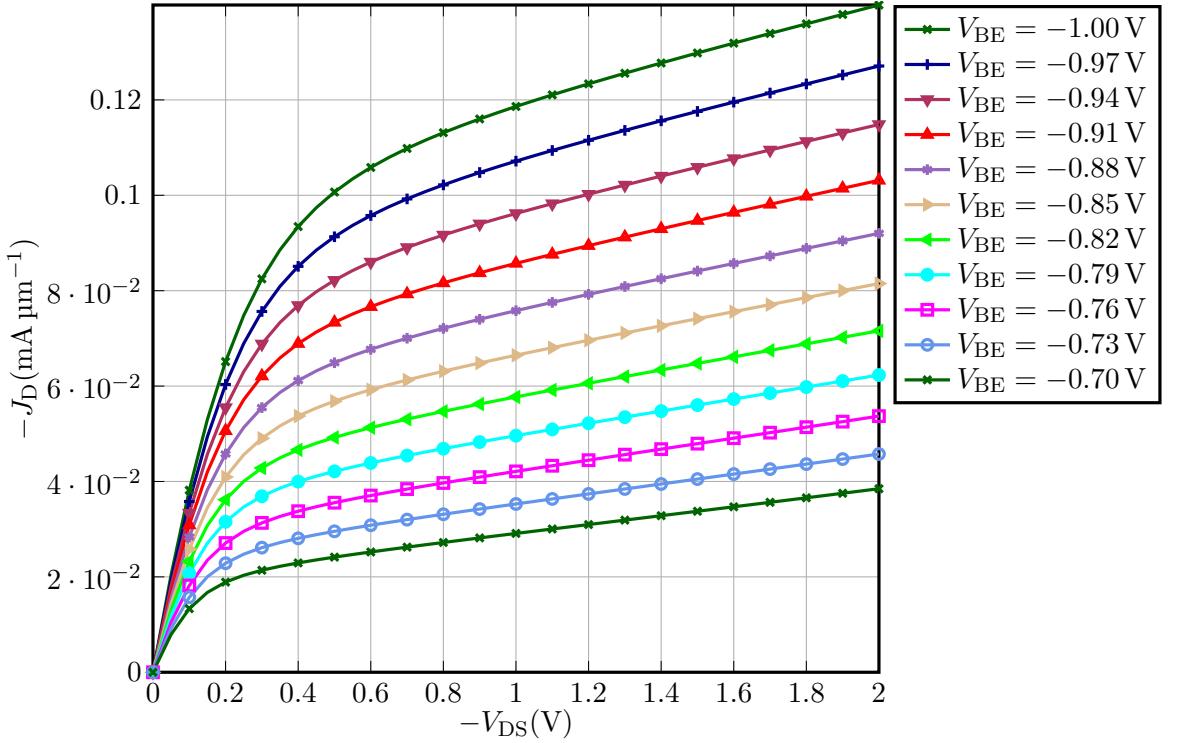
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Next, some AC characteristics @$T = 300\,\mathrm{K}$ are visualized.
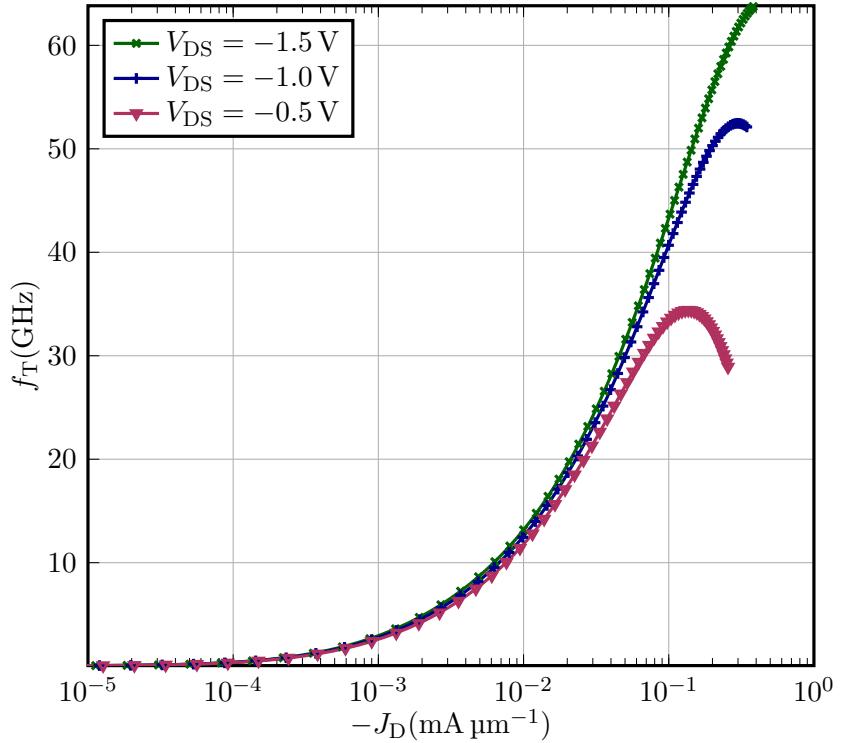
Figure 31: $f_{\mathrm{T}}(J_{\mathrm{D}})$ at V_{DS} and $T = 300\,\mathrm{K}$.
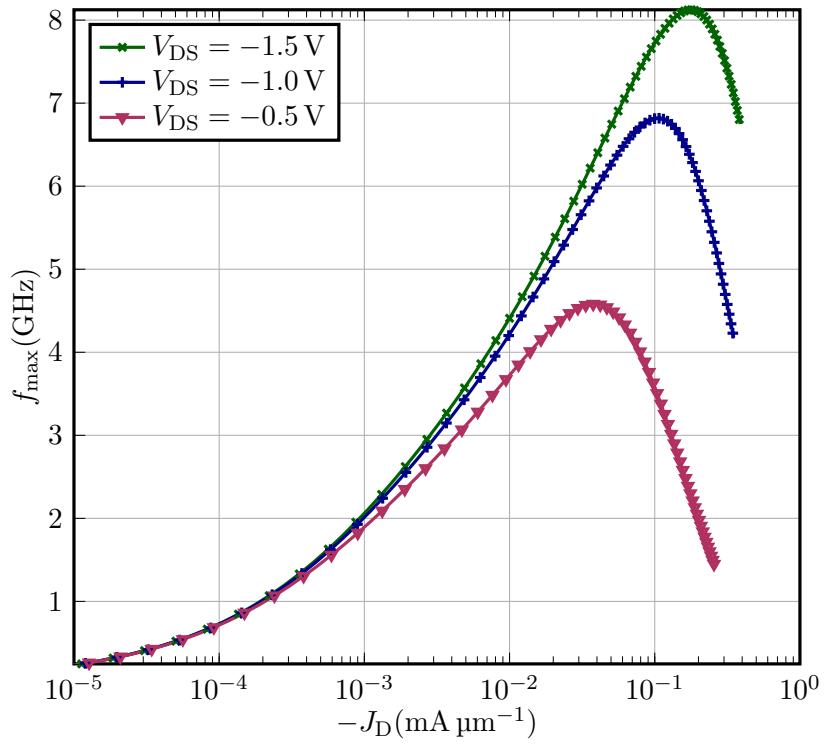
Figure 32: $f_{\max}(J_D)$ at V_{DS} and $T = 300\,\mathrm{K}$.
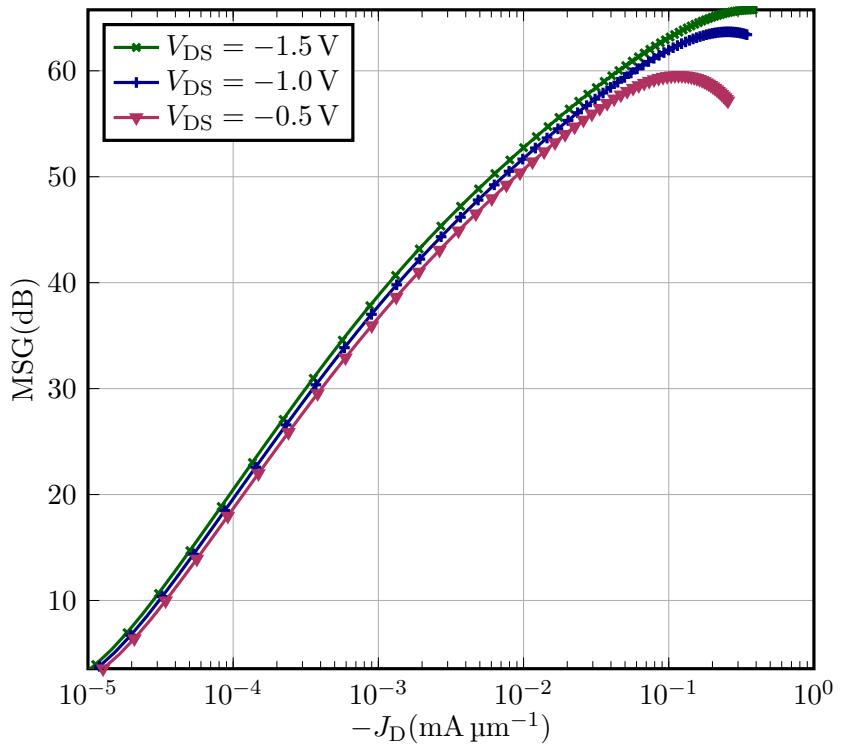
Figure 33: MSG(J_D) at V_{DS} and $T = 300\,\mathrm{K}$.

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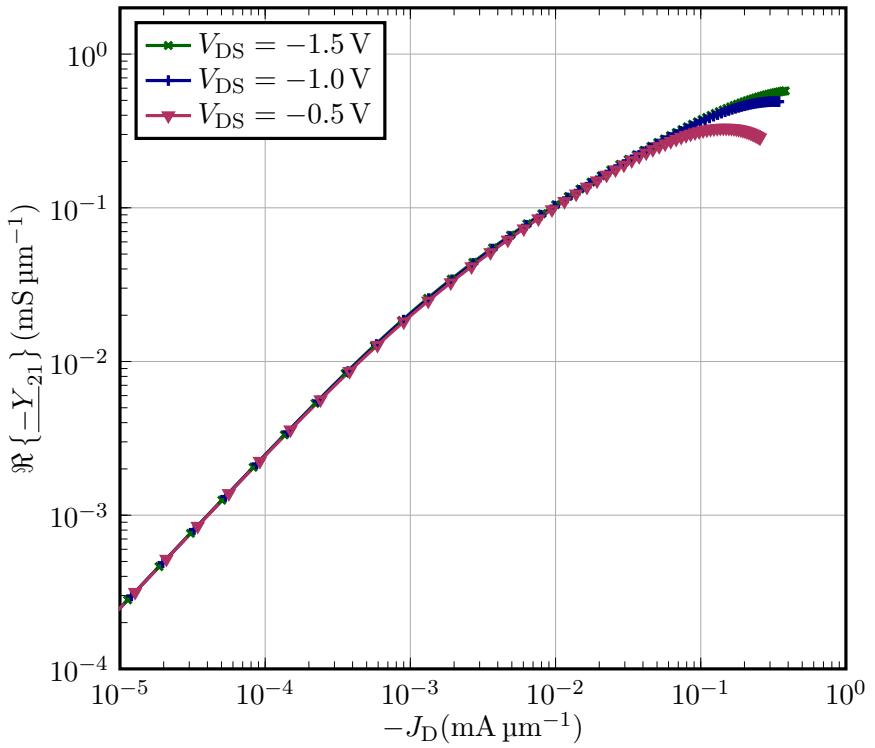
Figure 34: $\Re\left\{\underline{Y}_{21}\right\}(J_\mathrm{D})$ at V_DS and $T = 300\,\mathrm{K}$.

Next, some characteristics at different T and $V_\mathrm{DS} = 1.5\,\mathrm{V}$ are visualized.
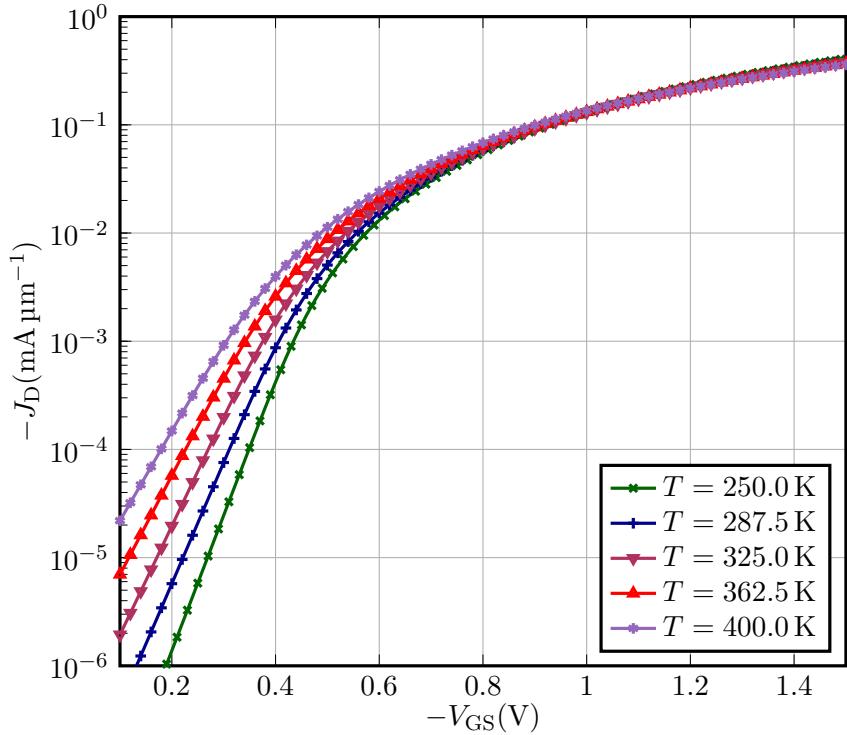
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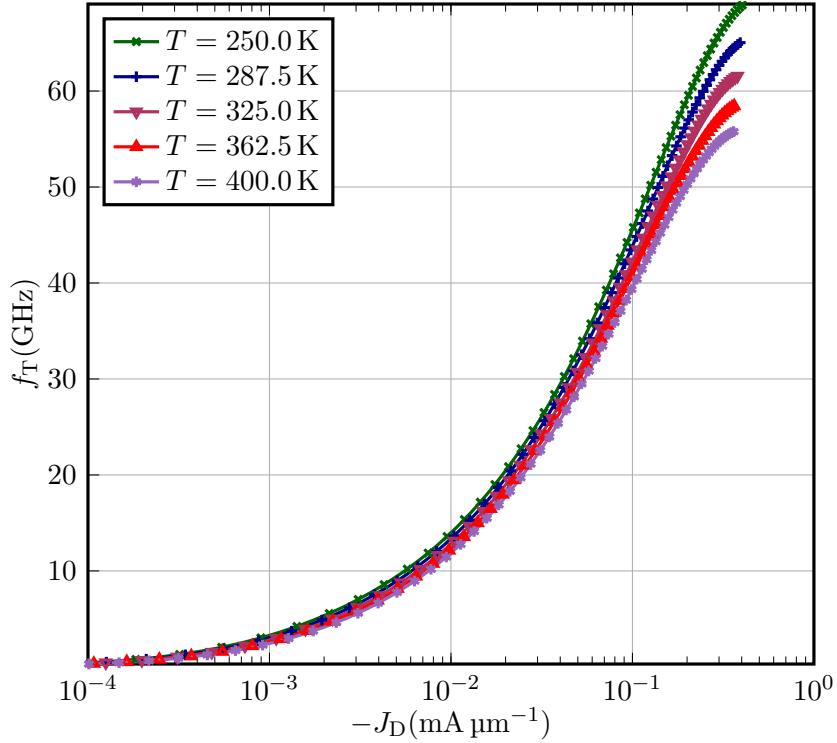
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6 IHP SG13G2 PSP PMOS $w = 0.35\,\mu\mathrm{m}$ $l = 0.35\,\mu\mathrm{m}$ Sanity Checks

This section gives an overview of the DC Characteristics of the transistor. Next, some DC characteristics @$T = 300\,\mathrm{K}$ are visualized.
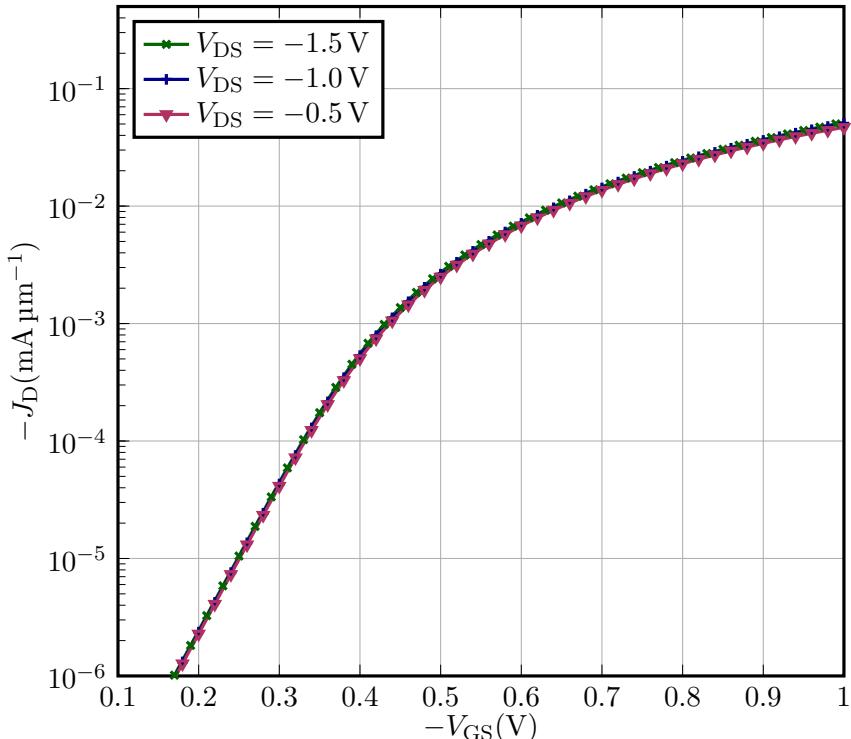

Figure 37: $J_{\mathrm{D}}(V_{\mathrm{GS}})$ at V_{DS} and $T = 300\,\mathrm{K}$.
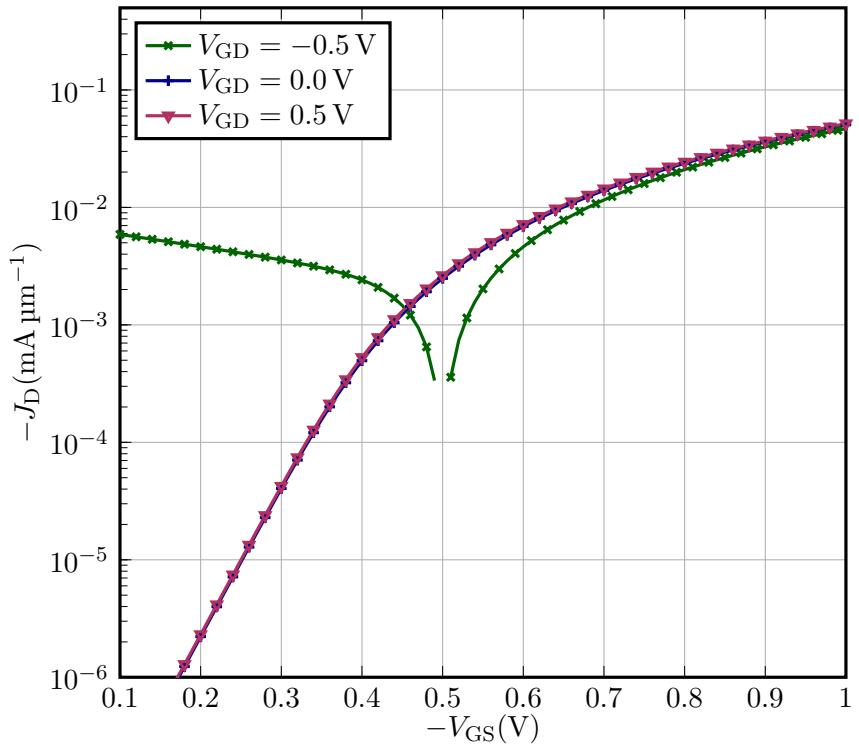
Figure 38: $J_{\mathrm{D}}(V_{\mathrm{GS}})$ at V_{BC} and $T = 300\,\mathrm{K}$.
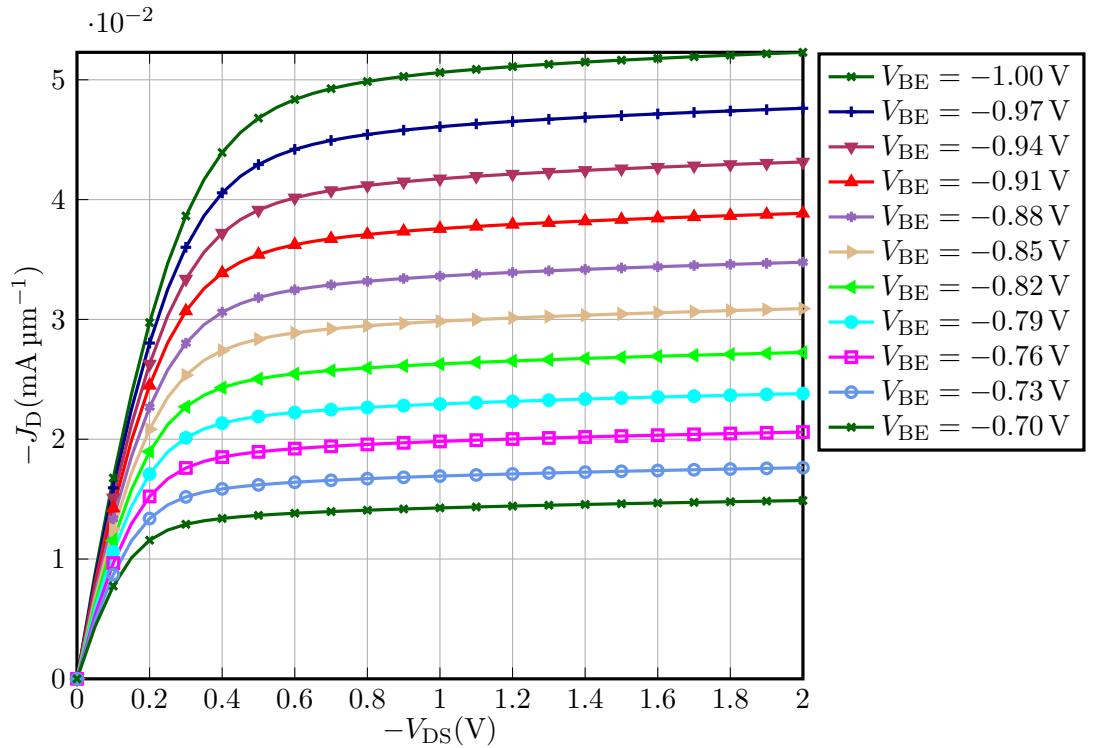
Figure 39: $J_{\mathrm{D}}(V_{\mathrm{DS}})$ at V_{GS} and $T = 300\,\mathrm{K}$.

Next, some AC characteristics @$T = 300\,\mathrm{K}$ are visualized.
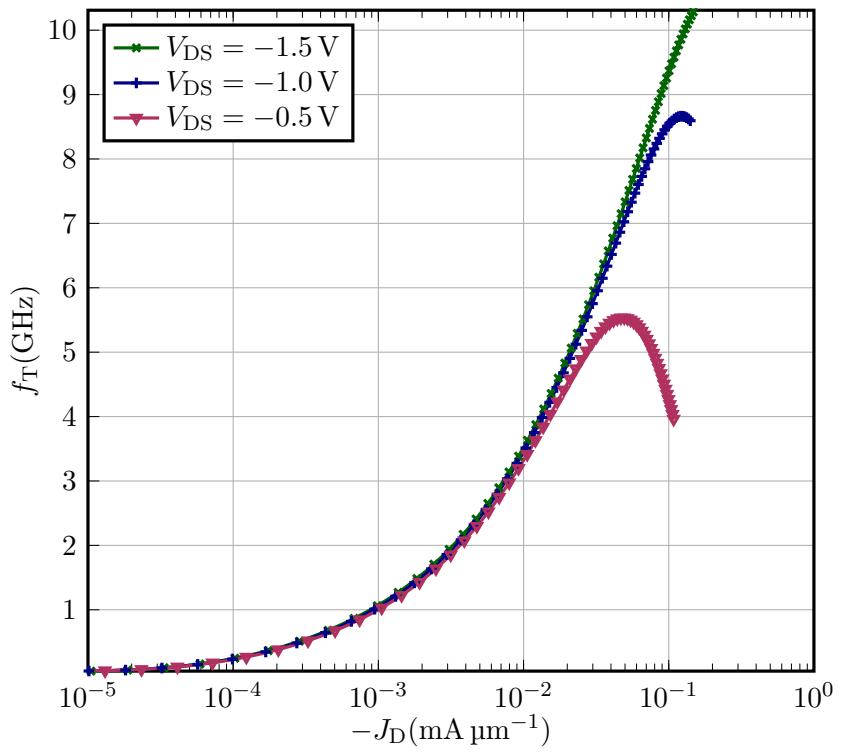
Figure 40: $f_{\mathrm{T}}(J_{\mathrm{D}})$ at V_{DS} and $T = 300\,\mathrm{K}$.
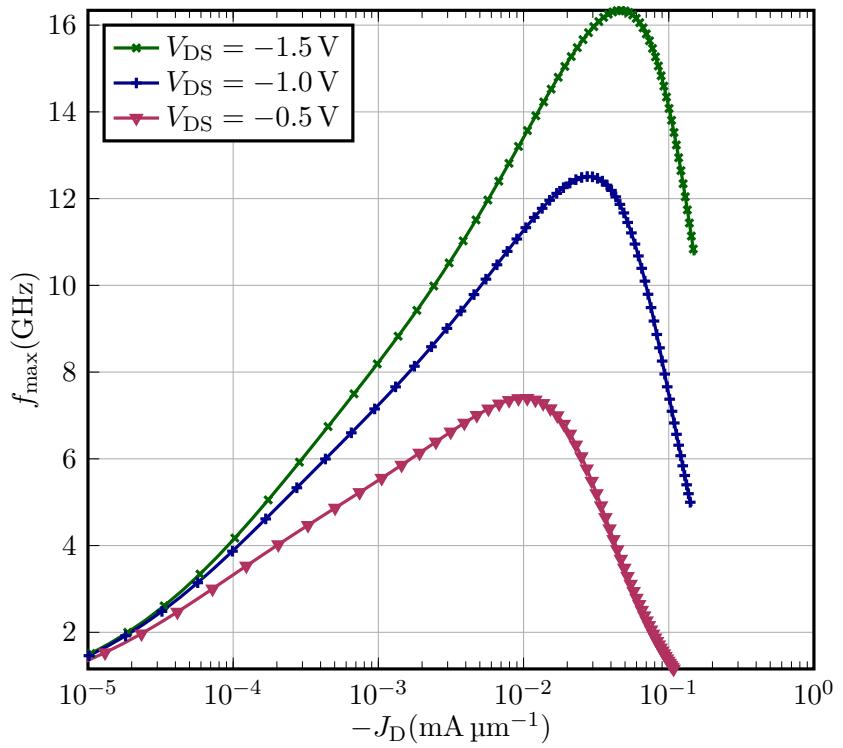
Figure 41: $f_{\max}(J_{\mathrm{D}})$ at V_{DS} and $T = 300\,\mathrm{K}$.

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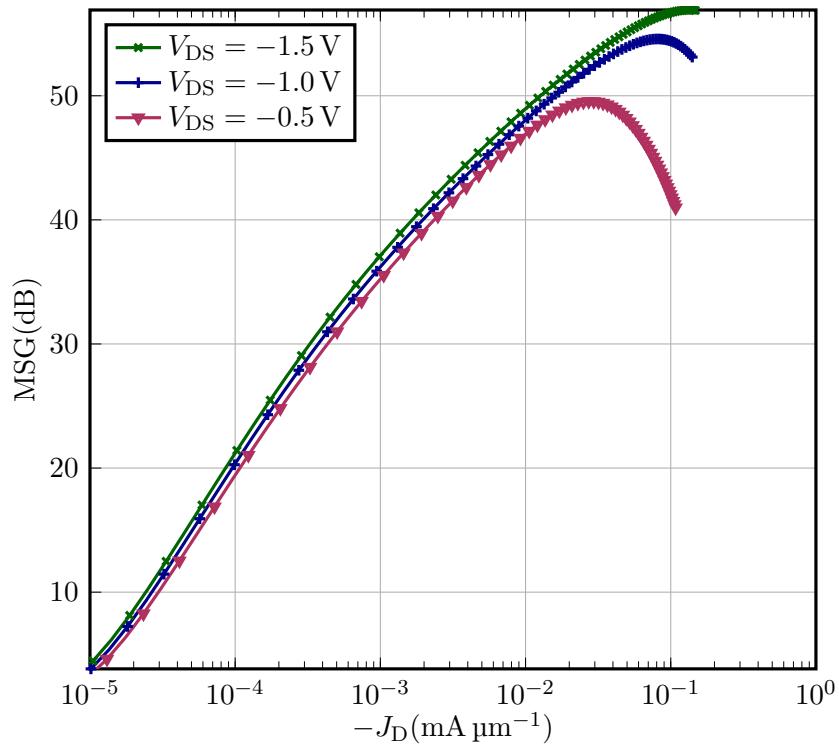
Figure 42: $\mathrm{MSG}(J_{\mathrm{D}})$ at V_{DS} and $T = 300\,\mathrm{K}$.
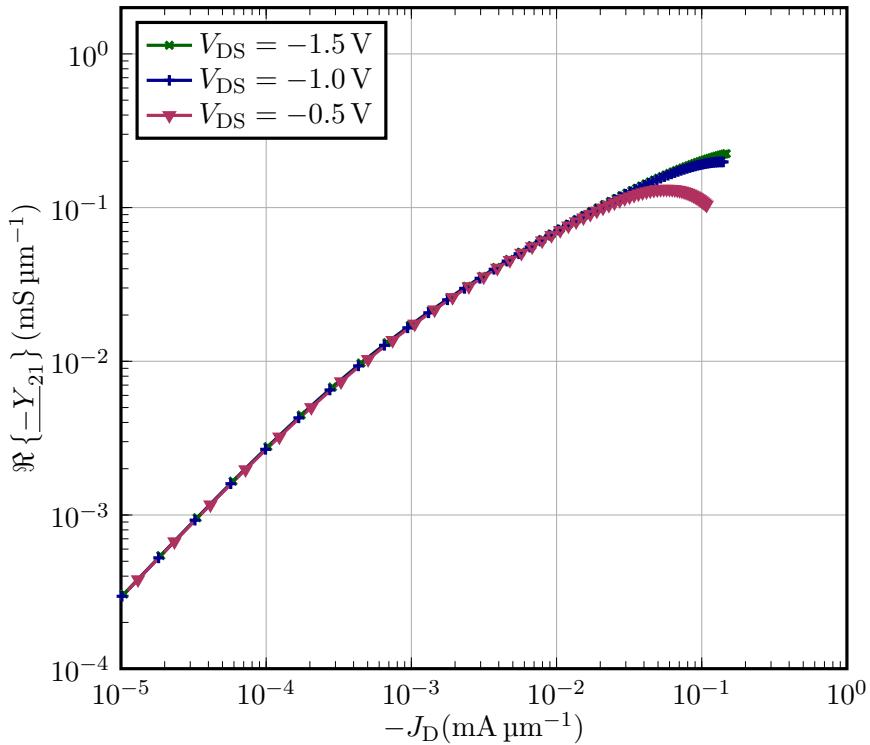
Figure 43: $\Re\left\{\underline{Y}_{21}\right\}(J_{\mathrm{D}})$ at V_{DS} and $T = 300\,\mathrm{K}$.

Next, some characteristics at different T and $V_{\mathrm{DS}} = 1.5\,\mathrm{V}$ are visualized.
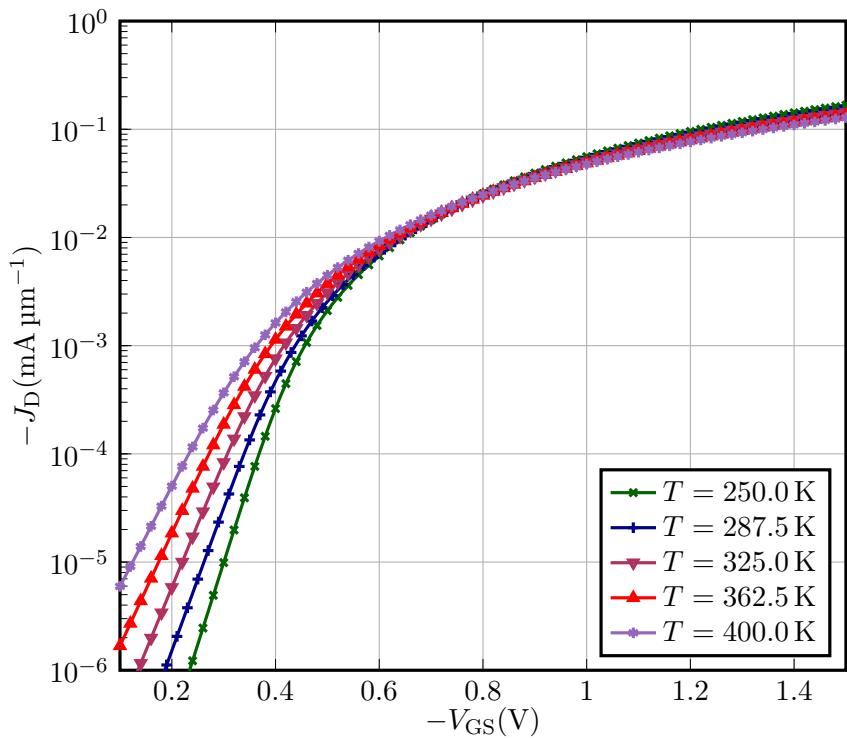
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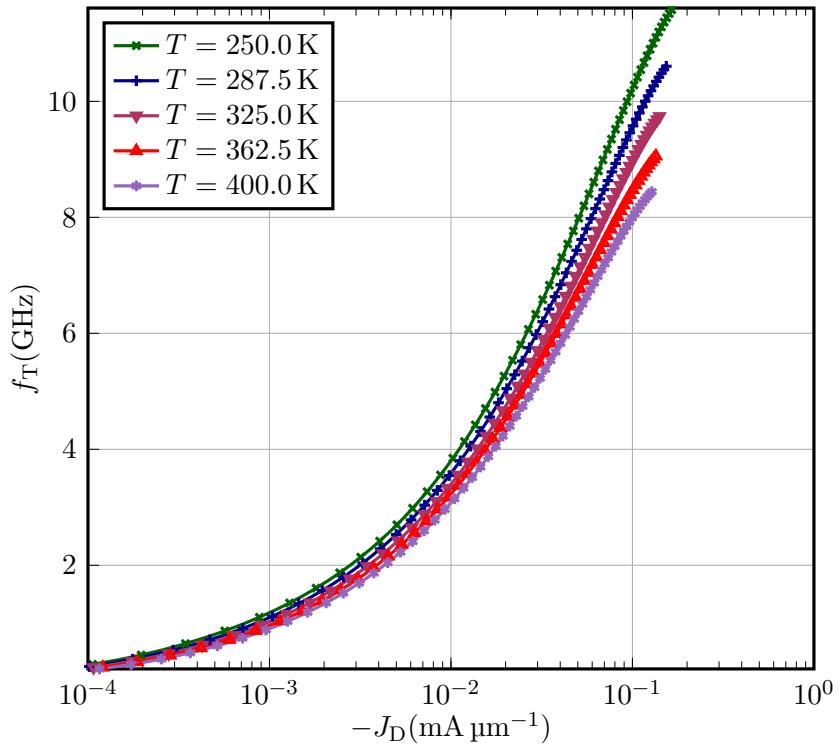
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Figure 46: $J_D(V_{GS})$ at $V_{DS} = 1\,\mathrm{V}$ over device length.
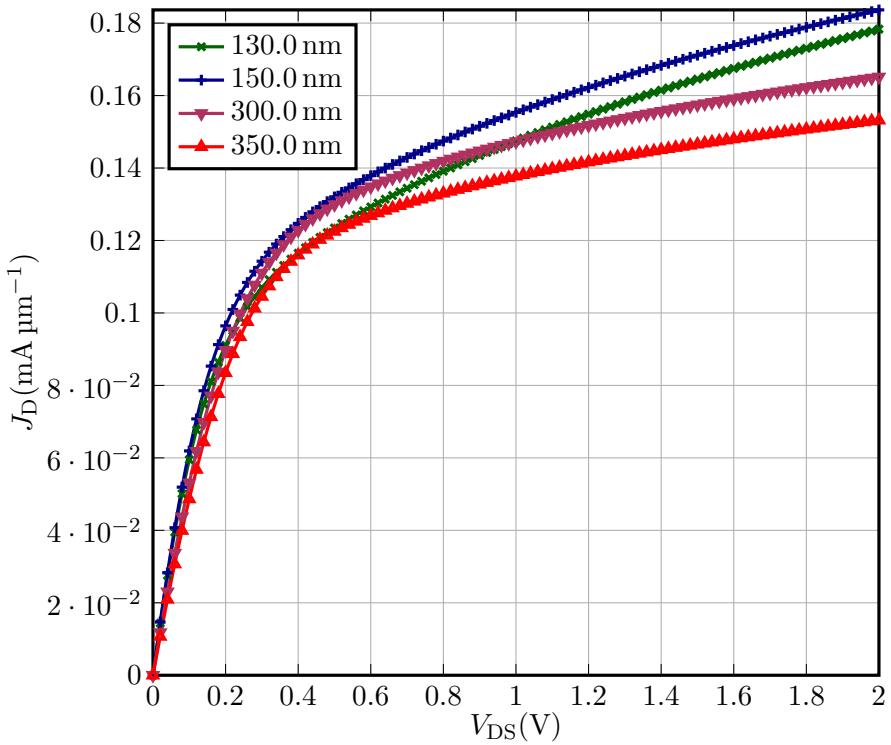
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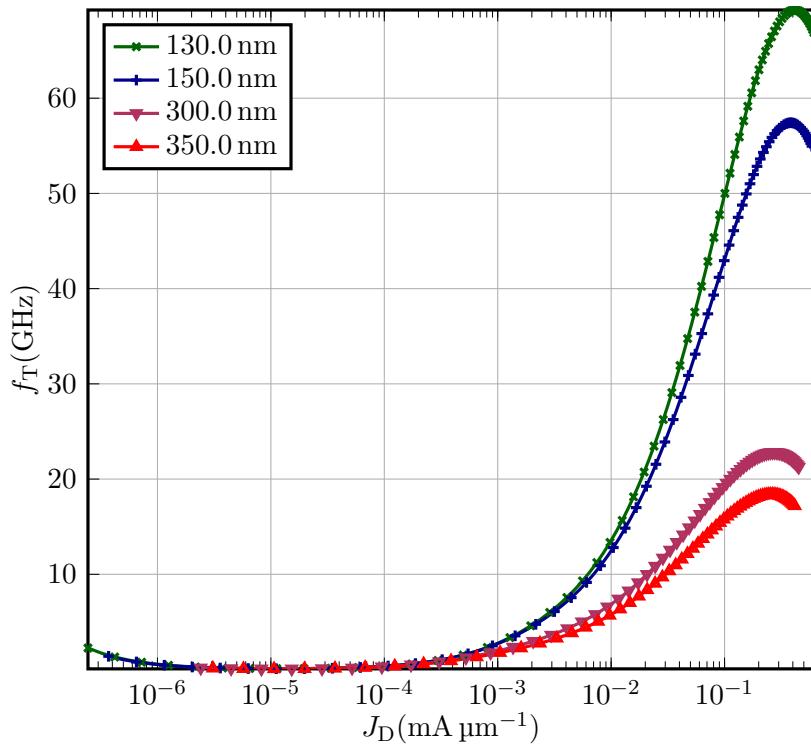
Figure 48: $f_{\mathrm{T}}(J_{\mathrm{D}})$ at $V_{\mathrm{DS}} = 1\,\mathrm{V}$ over device length.

8 IHP SG13G2 PMOS Length Scaling Sanity Checks
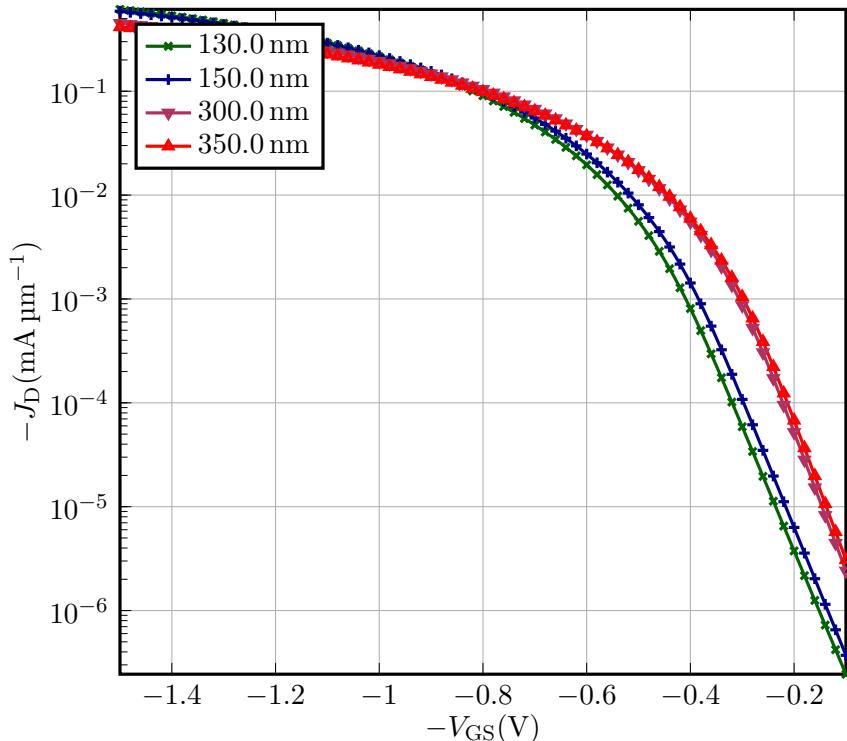
Figure 49: $J_{\mathrm{D}}(V_{\mathrm{GS}})$ at $V_{\mathrm{DS}} = 1\,\mathrm{V}$ over device length.
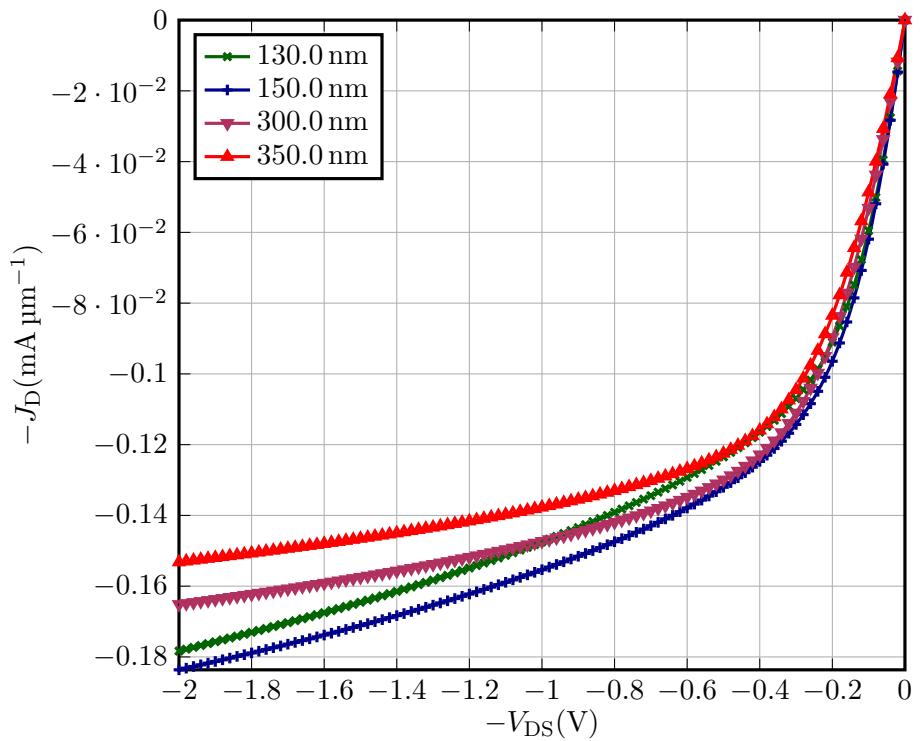
Figure 50: $J_{\mathrm{D}}(V_{\mathrm{DS}})$ at $V_{\mathrm{GS}} = 0.9\,\mathrm{V}$ over device length.
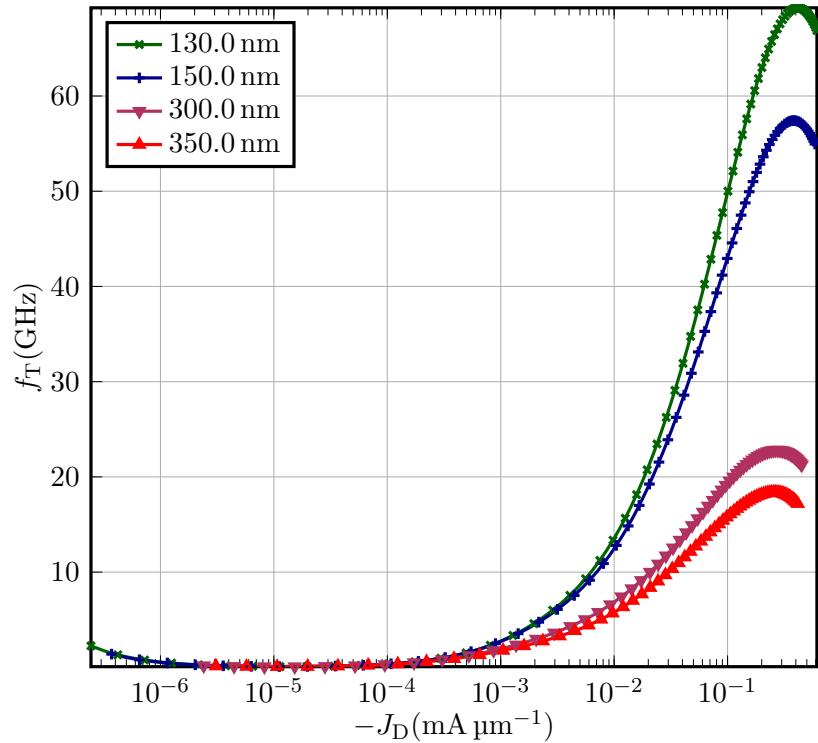
Figure 51: $f_{\mathrm{T}}(J_{\mathrm{D}})$ at $V_{\mathrm{DS}} = 1\,\mathrm{V}$ over device length.

9 IHP SG13G2 NMOS Width Scaling Sanity Checks
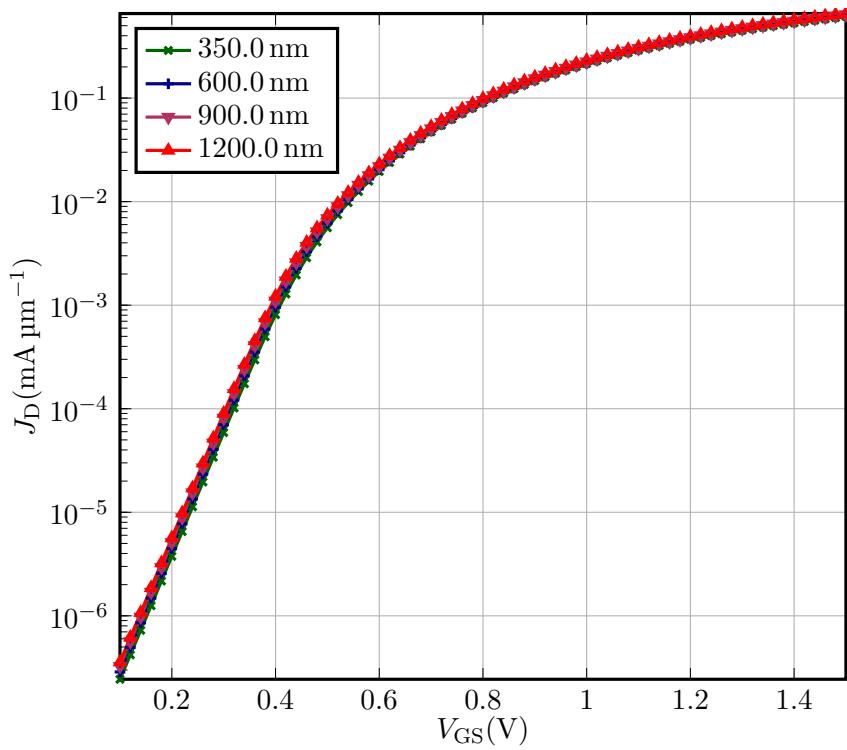
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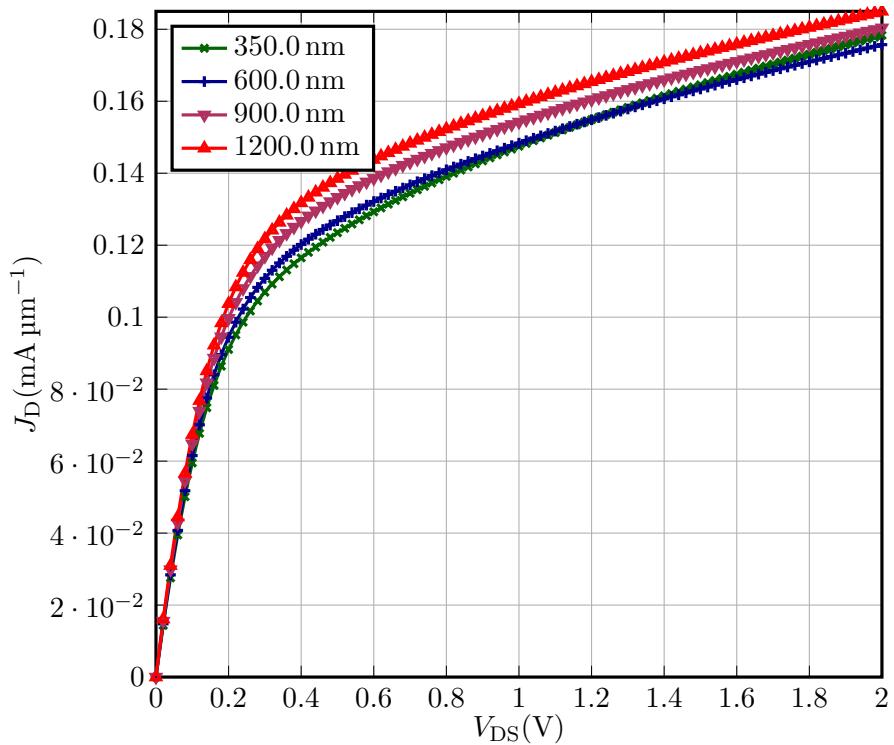
Figure 53: $J_{\mathrm{D}}(V_{\mathrm{DS}})$ at $V_{\mathrm{GS}} = 0.9\,\mathrm{V}$ over device width.
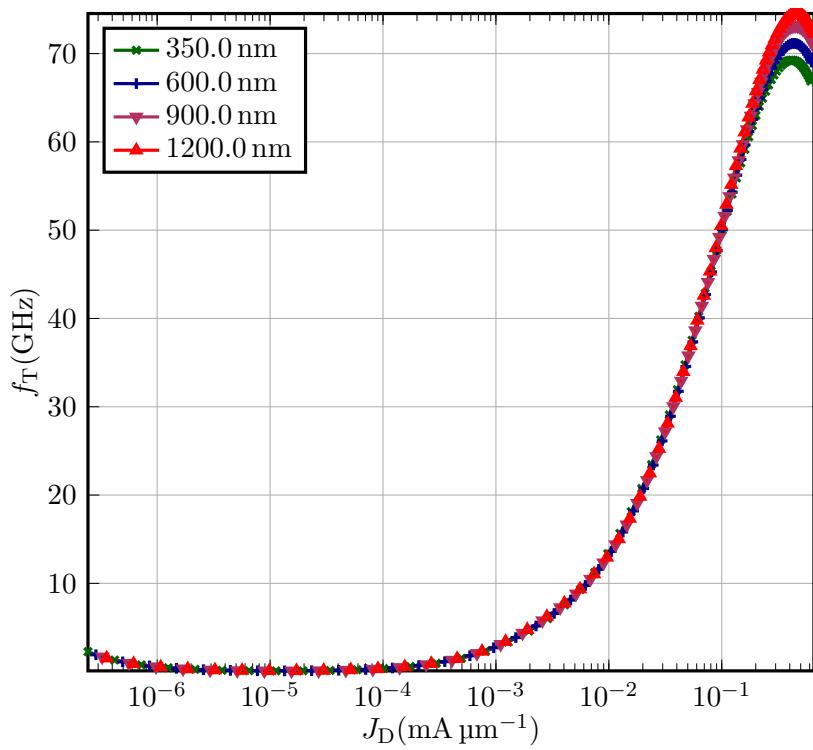
Figure 54: $f_{\mathrm{T}}(J_{\mathrm{D}})$ at $V_{\mathrm{DS}} = 1\,\mathrm{V}$ over device width.

10 IHP SG13G2 PMOS Width Scaling Sanity Checks
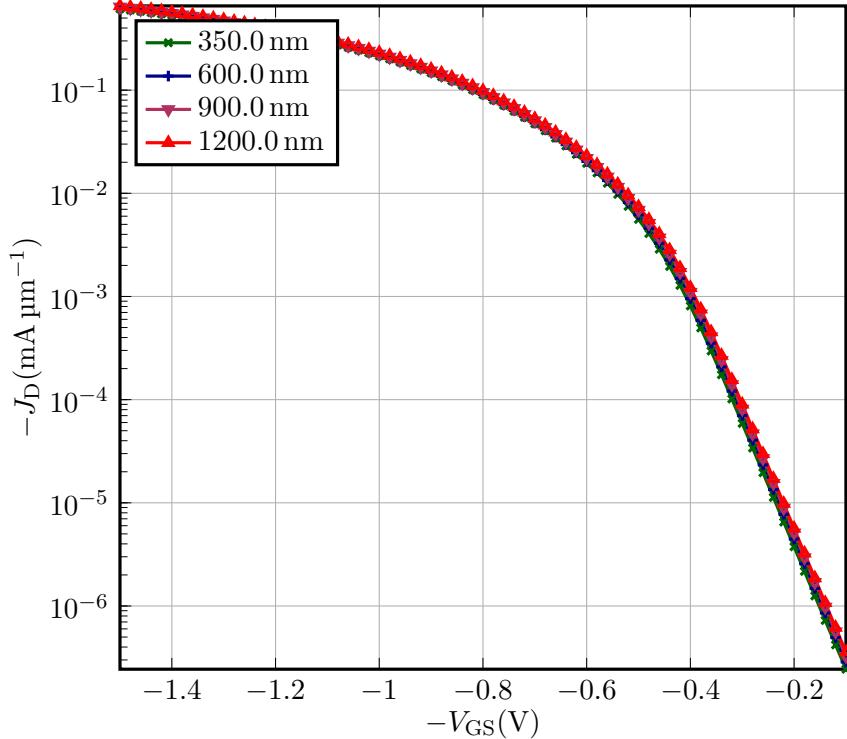
Figure 55: $J_{\mathrm{D}}(V_{\mathrm{GS}})$ at $V_{\mathrm{DS}} = 1\,\mathrm{V}$ over device width.
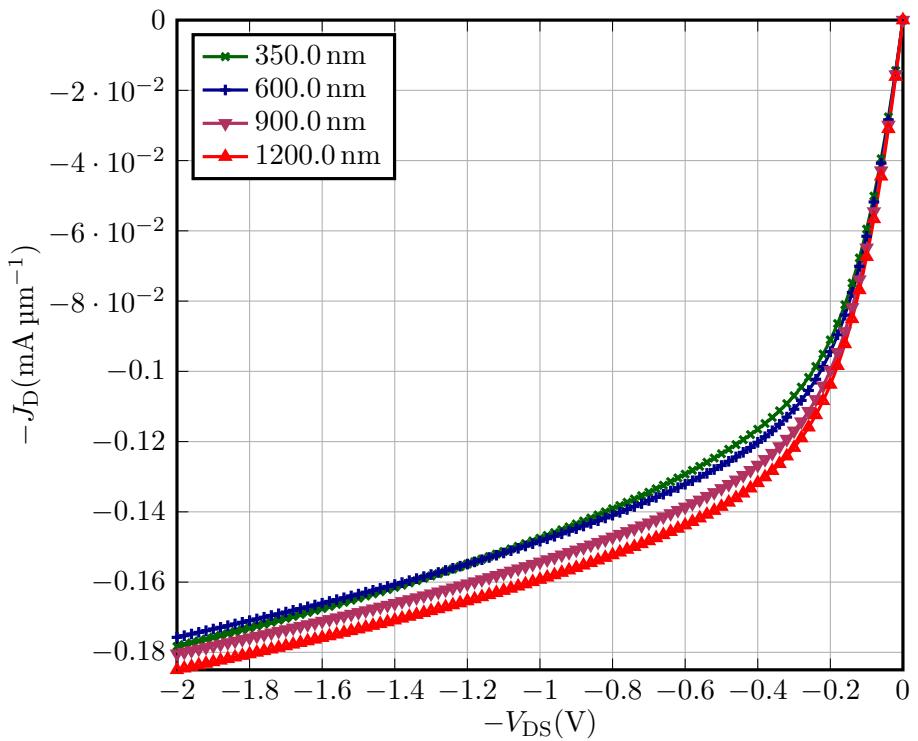
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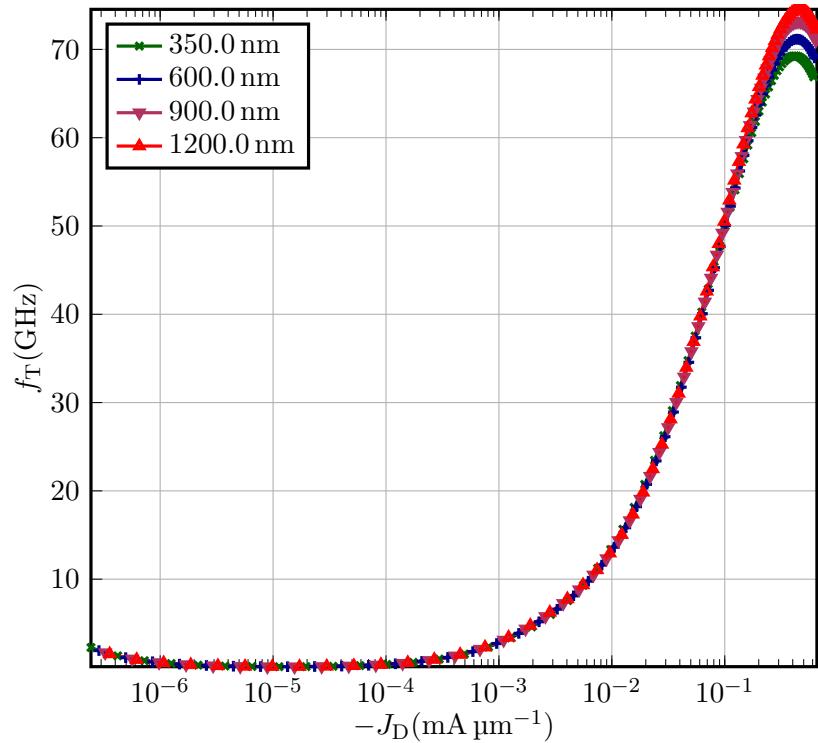
Figure 57: $f_T(J_D)$ at $V_{DS} = 1\,\text{V}$ over device width.

11 IHP SG13G2 NMOS Corner Sanity Checks
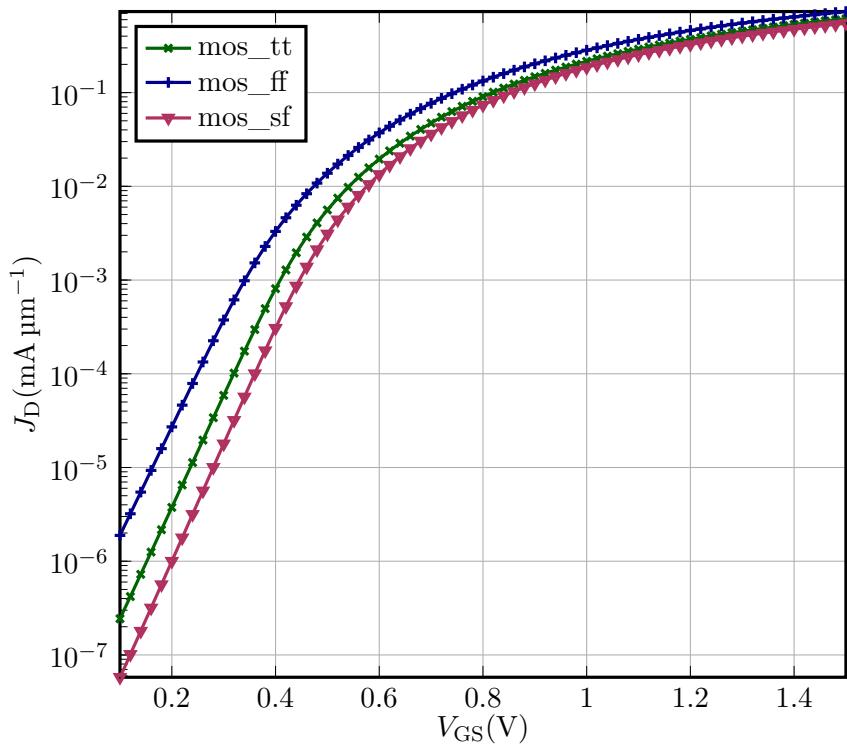
Figure 58: $J_D(V_{GS})$ at $V_{DS} = 1\,\mathrm{V}$ over corners.
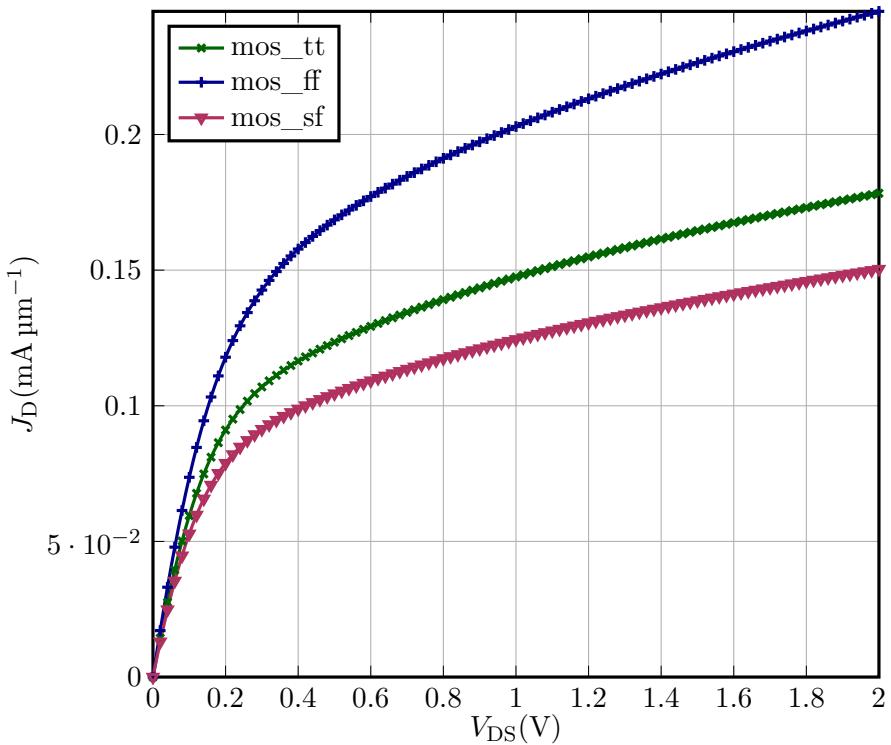

Figure 59: $J_D(V_{DS})$ at $V_{GS} = 0.9\,\mathrm{V}$ over corners.
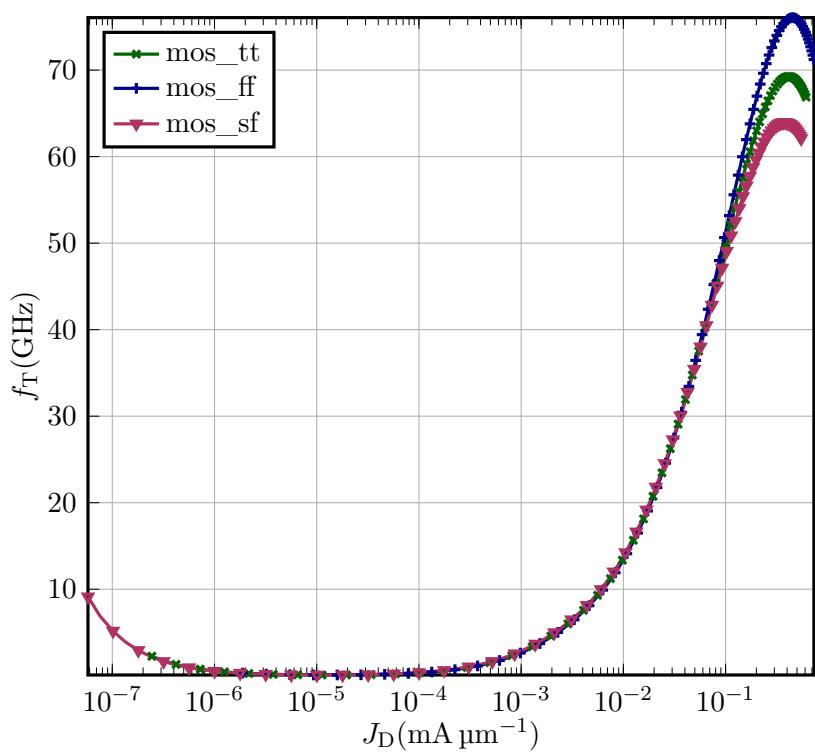
Figure 60: $f_T(J_D)$ at $V_{DS} = 1\,\text{V}$ over corners.