PY32F002B datasheet

32 bits ARM® Cortex® - M0+

Puya Semiconductor (Shanghai) Co., Ltd

Features

- Core
  - 32 bits ARM® Cortex® - M0+
  - Up to 24 MHz as a maximum frequency
- Memories
  - 24 Kbytes Flash memory
  - 3 Kbytes SRAM
- Clock system
  - Internal 24 MHz RC Oscillator (HSI)
  - Internal 32.768 KHz RC Oscillator (LSI)
  - 32.768 KHz low speed crystal oscillator (LSE)
  - External clock input
- Power management and reset
  - Operating voltage：1.7 V ~ 5.5 V
  - Low power modes: Sleep/Stop
  - Power-on/Power-down reset (POR/PDR)
  - Brownout Detect Reset (BOR)
- General purpose input and output (I/O)
  - Up to 18 I/Os，all available as external interrupts
  - Driver current 8mA
- 1 x 12 bits ADC

  —Support up to 8 external input channels and 2 internal channels
  - $V_{ADC-REF}$ internal 1.5 V，V_{CC}
- Timer
  - A 16 bits advanced control timer (TIM1)
  - A general purpose 16-bit timer (TIM14)
  - A low-power timer (LPTIM)，supports wake-up form stop mode
  - An Independent Watching Timer (IWDT)
  - A SysTick timer
- RTC
  - A Serial Peripheral Interface (SPI)
  - A Universal Synchronous/Asynchronous Transceiver (USART) with automatic
  - A I^2C interface，supports standard mode (100 KHz)、fast mode (400 KHz)，support 7 bits addressing mode
- Hardware CRC-32 module
- Two comparators
- Unique UID
- Serial wire debug (SWD)
- Working temperature：-40 ~ 85°C
- Package: TSSOP20, QFN20, SOP16, SOP14, MSOP10

Content

1. Introduction

PY32F002B series microcontrollers are MCUs with high performance 32 bits ARM® Cortex®-M0+ core and wide voltage operating range. It has embedded 24 Kbytes Flash and 3 Kbytes SRAM memory，a maximum operating frequency of 24 MHz, and contains various products in different package types. The chip integrates I²C, SPI, USAR and other communication peripherals, one channel 12 bits ADC，two16bit timers，and two channel comparators.

PY32F002B series microcontrollers' working temperature ranges from -40°C to 85°C with operating voltage from1.7 V ~ 5.5 V. The chip provides sleep and stop low-power operating modes for different low-power applications.

PY32F002B series microcontrollers are suitable for various applications, such as controllers, portable devices, PC peripherals, gaming and GPS platforms, industrial applications.

Table 1-1 PY32F002B Series Product Planning and Features

Peripherals		**PY32F002BF15**	**PY32F002BW15**	**PY32F002BD15**	**PY32F010MA15**
Flash memory (Kbyte)		24			
SRAM (Kbyte)		3			
Timer	Advanced	1 (16-bit)			
	General	1 (16-bit)			
	Low-power	1			
	SysTick	1			
	Watchdog	1			
Communication Interface	SPI	1			
	I²C	1			
	USART	1			
Universal Port		18	14	12	8
Number of ADC channels (external + internal)		8+2	7+2	5+2	7+2
Comparators		2			
Highest Frequency		24 MHz			
Operating Voltage		1.7 V ~ 5.5 V			
Package		TSSOP20,	SOP16	SOP14	MSOP10

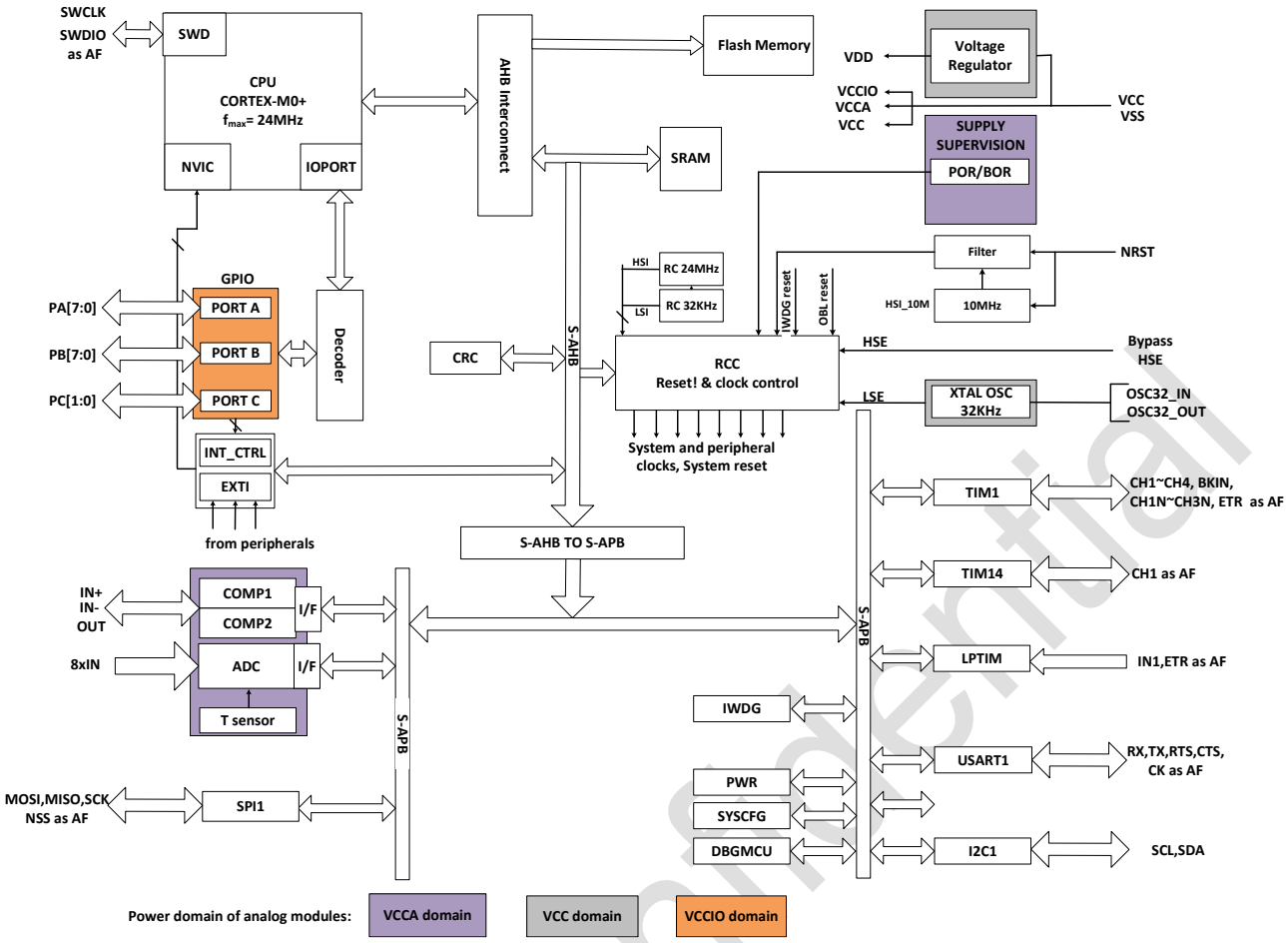


Figure 1-1 Functional Module

2. Functional overview

2.1. Arm® Cortex®-M0+ core

Arm® Cortex®- M0+ is an entry-level 32 bits Arm Cortex processor designed for a wide range of embedded applications. It provides developers with significant benefits, including:

- Simple structure, easy to learn and program
- Ultra-low power consumption, energy-saving operation
- Reduced code density and more

Cortex-M0+ processor has a 32 bits core, optimized for area and power consumption, as well with a 2-stage pipeline Von Neumann architecture. The processor offers high-end processing hardware, including single-cycle multipliers, through a streamlined but powerful instruction set and an extensively optimized design. Moreover, it delivers the superior performance expected from a 32 bits architecture computer, with a higher coding density than other 8 and 16 bits microcontrollers.
Cortex-M0+ is tightly coupled with a Nested Vectored Interrupt Controller(NVIC).

2.2. Memory

The on-chip integrated SRAM is accessed by bytes (8 bits), half-word (16 bits) or word (32 bits).
The on-chip integrated Flash consists of two different physical areas:

- Main flash area, which consists application and user data
- Size-configurable Load Flash area，which houses the customer ISP/IAP bootstrap
- The information area has 768 bytes，and it includes the following parts：
  - Option bytes
  - UID bytes
  - Factory config bytes
  - USER OTP memory

The protection mechanisms of Flash main memory includes the following ones：

- Write protection (WRP)control prevents unwanted writes (confuse by program memory pointer from PC). The minimum protection unit for write protection is 4 Kbytes.
- Option byte write protection has special unlocking design.

2.3. Boot mode

Through configuration bit nBOOT0/ nBOOT1(stored in Option bytes), three different boot modes can be selected, as shown in the following table:

Table 2-1 Boot configuration

Boot mode configuration		Mode	
nBOOT1 bit	**nBOOT0 bit**	**Boot memory size ==0**	**Boot memory size !=0**
X	0	Main flash boots	Main Flash boots
0	1	SRAM boots	SRAM boots
1	1	N/A	Load Flash boots

The Boot loader program is stored in the Load Flash and used to download the Flash program through the USART interface.

2.4. Clock System

After the CPU starts, the default system clock frequency is HSI 24 MHz, and the system clock frequency and system clock source can be reconfigured after program runs. The high frequency clocks than can be selected are:

- 24 MHz configurable internal high precision HIS clock
- A 32.768 KHz configurable LSI clock
- 4 MHz ~ 32 MHz external input clock
- 32.768 KHz LSE clock

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. AHB and APB clock frequencies are up to 24 MHz.

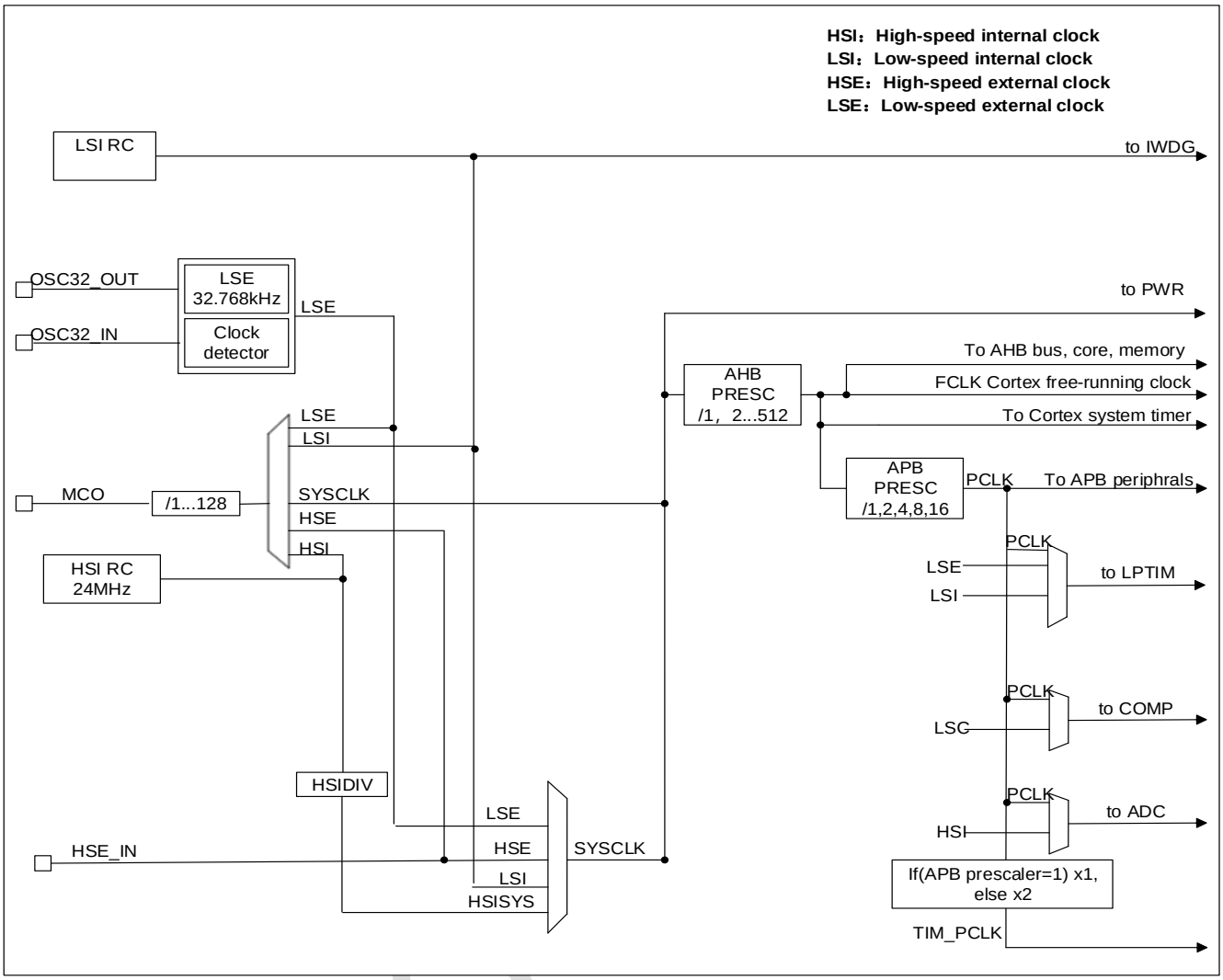


Figure 2-1 System Clock Structure Diagram

2.5. Power Management

2.5.1. Power block diagram

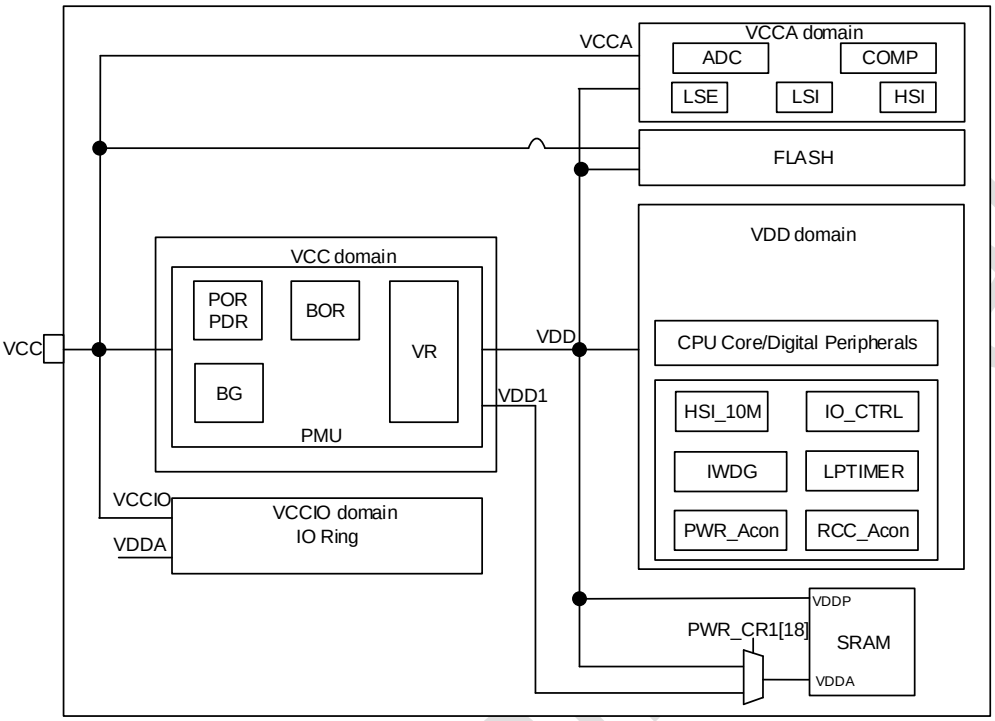


Figure 2-2 Power Block Diagram

Table 2-2 Power Block Diagram

Serial number	Power supply	Power value	Description
1	V_{CC}	1.7 V ~ 5.5 V	The chip is supplied with power through the power pins, and its power supply module is part of the analogue circuit.
2	V_{CCA}	1.7 V ~ 5.5 V	Power to most analogue modules from V_{CC} PAD (a separate power PAD can also be designed).
3	V_{CCIO}	1.7 V ~ 5.5 V	Supply power to IO, from V_{CC} PAD

2.5.2. Power monitoring

2.5.2.1. Power on reset/ Power down rest (POR/PDR)

The embedded Power on reset (POR)/Power down reset (PDR) modules are designed to provide power-on and power-off reset for the chip. The modules keep working in all modes.

2.5.2.2. Brown-out reset (BOR)

In addition to POR/PDR, BOR (brown out reset) has also been implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is turned on，the BOR threshold can be selected by the Option byte, and both the rising and falling detection points can be configured individually.

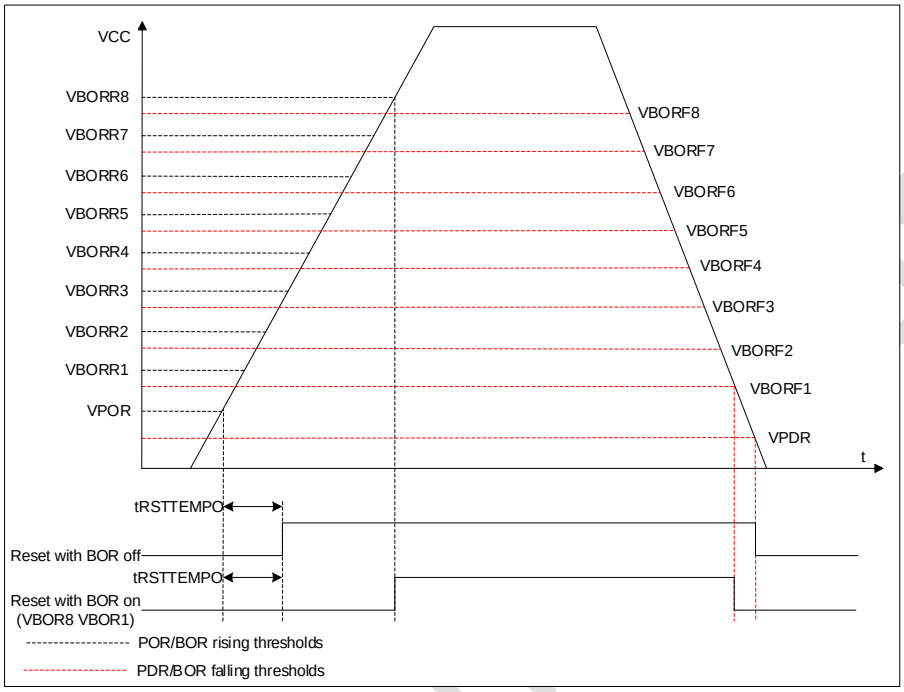


Figure 2-3 POR/PDR/BOR threshold

2.5.3. Voltage regulator

The chip designs two voltage regulators:

- MR (Main regulator) keeps working when the chip is in normal operating state
- LPR (low power regulator) provides a lower consumption option in stop mode

2.5.4. Low power mode

In addition to the normal operating mode, the chip has other two low-power modes:

- **Sleep mode**：Peripherals can be configured to keep working when the CPU clock is off (NVIC，SysTick, etc.). (It's recommended only to enable the modules that must work, and close the module after the module works.)

- **Stop mode**：In this mode, the contents of SRAM and registers are maintained, high speed timer PLL、HIS and HSE are turned off. GPIO, IWDG, NRST, COMP output, LPTIM can wake up stop mode.

2.6. Rest

Two resets are designed in the chip: power and system reset.

2.6.1. Power reset

Aa power reset occurs in the following situations：

- Power on reset/ Power down reset (POR/PDR)
- Brown-out reset (BOR)

2.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Independent Watchdog Reset (IWDG)
- SYSRESETREQ software reset
- option byte load reset (OBL)
- Power reset (POR/PDR, BOR)

2.7. General purpose input and output (GPIO)

The software configures each GPIO as output (push-pull or open-drain), input (floating, pull-up/down, analogue), peripheral multiplexing function, and locking mechanism freeze I/O port configuration function.

2.8. Interrupt

The PY32F002B handles exceptions through the Cortex-M0+ processor's embedded Vectored Interrupt Controller (NVIC) and an Extended Interrupt/Event Controller (EXTI).

2.8.1. Interrupt controller NVIC

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a high-priority interrupt event occurs and a low-priority interrupt event is just waiting to be serviced, the later arriving high-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a high-priority ISR and then starting a pending low-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handing
- Level 4 Interrupt Priority
- Supports one NMI interrupt
- Supports 18 maskable external interrupts
- Supports 10 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Supports tail-chaining optimization
- Hardware Interrupt Vector Retrieval

2.8.2. 2.8.2. External interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from stop mode.

The EXTI controller has multiple channels, including a maximum of 18 GPIOs, 2 COMP outputs, and LPTIM wake up signal. GPIO, COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 ~ 7 channel through the select signal.

Each EXTI line can be independently masked through registers.

The EXTI controller can capture pulses shorter than the internal clock period.

Registers in the EXTI controller latch each event. Even in stop mode, after the processor wakes up from stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.9. Analog to digital converter (ADC)

The chip has a 12 bits SARADC. The module has up to 10 channels to be measured, including 8 external channels and 2 internal channels. Reference voltage can be selected from on-chip precise voltage 1.5 V or V_{CC} power supply.

The conversion mode of each channel can be set to single, continuous, sweep, discontinuous mode. Conversion results are stored in left or right-aligned 16 bits data registers.

An analogue watchdog allows the application to detect if the input voltage exceeds a user-defined high or low threshold.

The ADC has been implemented to operate at a low frequency, resulting in lower power consumption.

At the end of sampling, conversion, and continuous conversion, an interrupt request is generated when the conversion voltage exceeds the threshold when simulating the watchdog.

2.10. Comparator (COMP)

The on-chip general purpose comparators (COMP) can also be used in combination with timers. The comparators can be used as follows:

- Wakeup from low-power mode triggered by an analog signal
- Analog signals conditioning
- Cycle-by-cycle current control loop when combined with a PWM output from a timer

2.10.1. COMP main features

- Each comparator has configurable positive and negative inputs used for flexible voltage selection:
  - Multiplexing I/O pin
  - Power supply V_{CC} and 15 submultiple values (1/16、2/16 ... 15/16) provided by voltage divider
  - Internal reference voltage is 1.5 V, and 15 submultiple values (1/16、2/16 ... 15/16) provided by voltage divider
- The outputs can be redirected to an I/O or to timer inputs for triggering:
  - OCREF_CLR event (cycle by cycle current control)
  - Brakes for fast PWM shutdown

Each COMP has interrupt generation capability which is used to wake up the chip from low power modes (sleep and stop mode) (Via EXTI).

2.11. Timer

The characteristics of PY32F002B are shown in the following table:

Table 2-3 Timer characteristics

Types	Timer	Bit Width	Counting Direction	Prescaler	DMA	Capture/compare channel	Complementary output
Advanced Timer	TIM1	16 bits	Superior, Down, Center aligned	1~65536	support	4	3
General purpose Timer	TIM14	16 bits	Superior	1~65536	-	1	-

2.11.1. Advanced Timer

The advanced timer (TIM1) consists of a 16 bits auto-reload counter driven by a 16 bits programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

TIM1 includes 4 independent channels:

- Input capture
- Output comparison
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If TIM1 is configured as a standard 16-bit timer, it has the same characteristics as the TIMx timer. Full modulation capability (0-100%) if configured as a 16 bits PWM generator.

In the MCU debug mode, TIM1 can freeze counting.

The timer feature with the same architecture is shared so that the TIM1 can work with other timers for synchronization or event chaining through the timer chaining function.

2.11.2. General purpose timer

- The general purpose timer TIM14 consists of 16 bits programmable prescaler
- TIM14 has an independent channel for input capture/ output compare，PWM or single pulse mode output
- In the MCU debug mode，the TIM14 can freeze counting

2.11.3. Lower power timer

- LPTIM is a 16 -bit up counter with a 3 bits prescaler and only support a single count

- LPTIM can be configured as a stop mode wakeup source
- In the MCU debug mode, LPTIM can freeze the count value

2.11.4. IWDG

Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

- The IWDG is clocked by LSI, so even if the main clock fails, it can keep working
- IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.
- Controlling of option byte can enable IWDG hardware mode
- IWDG is the wake-up source of stop mode, which wakes up stop mode by reset
- In the MCU debug mode, IWDG can freeze the count value

2.11.5. SysTick timer

SysTick counters are specifically for real-time operating systems (RTOS) also can use as standard down counters.

SysTick Features:

- 24 bits count down
- Self-loading capability
- An interrupt can be generated when the counter reaches 0 (maskable)

2.12. I²C Interface

I²C (inter-integrated circuit) bus interface connects the microcontroller and the serial I²C bus. It provides multimaster capability and controls all I²C bus specific sequences, protocols, arbitration and timing. Standard (Sm) and fast (Fm) are supported.

I²C Features:

- Slave and master mode
- Multi-host function: can be master or slave
- Support different communication speeds
  - Standard Mode (Sm): Up to 100 kHz

  - Fast Mode (Fm): up to 400 kHz
- As master
  - Generate Clock
  - Generation of Start and Stop
- As slave
  - Programmable I^2C address detection
  - Discovery of the Stop bit
- 7 bits addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^2C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional Clock Stretching
- Software reset
- Analogue noise filter function

2.13. Universal synchronous asynchronous recevicer/ transmitter (USART)

The Universal Synchronous Asynchronous Transceiver (USART) provides a flexible method for full-

duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baudrate generator to provide a wide range of baudrate options. It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baudrate detection is supported.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baudrate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baudrate detection
- Programmable data length of 8 or 9 bits
- Configurable stop bits (1 bit or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Detection flag
  - Receive full buffer
  - Send empty buffer
  - End of transmission
- Parity Control
  - Send check digit
  - Check the received data
- Flagged interrupt sources

- CTS change
- Send empty register
- Send completed
- Receive full data register
- Bus idle detected
- Overflow error
- Frame error
- Noise operation
- Error detection

- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.14. Serial peripheral interface (SPI)

Serial Peripheral Interface (SPI) allows the chip to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in master mode and provides the communication clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or slave mode
- 3 -wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8 bits or 16 bits transmission frame selection
- Support multi-master mode
- 8 master mode baudrate prescaler factors (max 12 M)
- Slave mode frequency (max 1.5 M)

- Both master and slave modes can be managed by software or hardware NSS: dynamic change of
- master/slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Interrupt-causing master mode faults, overloads
- Two 32 bits Rx and Tx FIFOs

2.15. SWD

The ARM SWD interface allows serial debugging tools to be connected to the PY32F002B.

3. Pin configuration

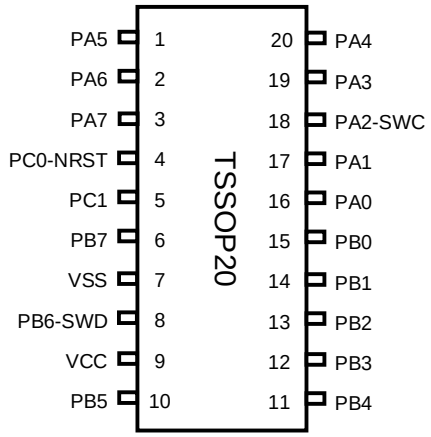


Figure 3-1 TSSOP20 Pinout1 PY32F002BF15P

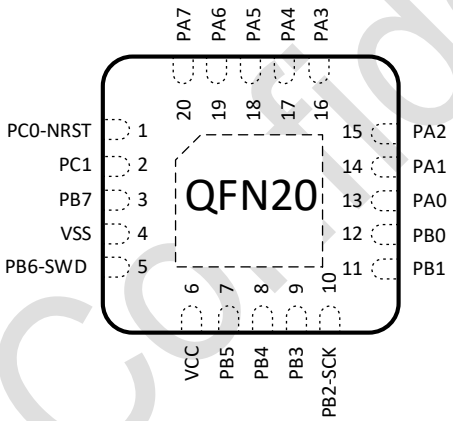


Figure 3-2 QFN20 Pinout1 PY32F002BF15U

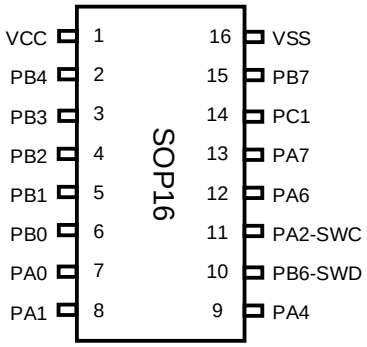


Figure 3-3 SOP16 Pinout1 PY32F002BW15S

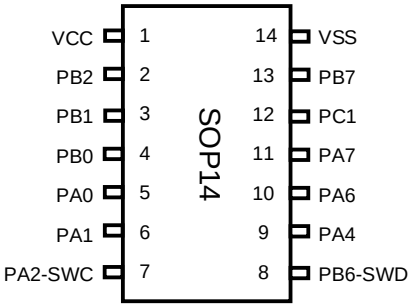


Figure 3-4 SOP14 Pinout1 PY32F002BD15S

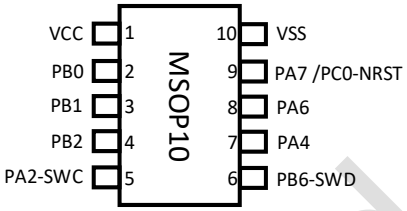


Figure 3-5 MSOP10 Pinout1 PY32F010MA15N

Table 3-1 Pin definition terminology and symbols

Type		Symbol	Definition
Port type		S	Supply pin
		G	Ground pin
		I/O	Input/output pin
		NC	Undefined
Port structure		COM	5 V port, with internal input and output function
		RST	-
Notes		-	Unless other specified, all ports are used as analog inputs between and after reset
Port function	Multiplexing function	-	Function selected by GPIOx_AFR register
	Additional features	-	Directly selected or enabled through peripheral registers

Table 3-2 Pin definition

Package		Reset	Port type	Port structure	Notes	Port function	
QFN20 F1	TSSOP20 F1					Multiplexing function	Additional features
18	1	PA5	I/O	COM		USART_CK TIM1_CH1 TIM14_CH1	
19	2	PA6	I/O	COM		SPI_NSS USART_TX EVENTOUT	ADC_IN3 External_clock_in
20	3	PA7	I/O	COM		SPI_MOSI USART_TX USART_RX TIM1_CH4 MCO	ADC_IN4
1	4	PC0-NRST	I/O	RST	(1)	SWDIO TIM1_CH1N EVENTOUT	NRST ADC_IN5
2	5	PC1-OSCIN	I/O	COM		SPI_MISO	OSCIN
3	6	PB7-OSCOUT	I/O	COM		SPI_MOSI TIM14_CH1	OSCOUT
4	7	V_{SS}	S			Ground	
5	8	PB6(SWDIO)	I/O	COM		SPI_MISO USART_TX I^2C_SDA SWDIO	ADC_IN6
6	9	V_{CC}	S			Digital power supply	
7	10	PB5	I/O	COM		SPI_NSS USART_RX TIM1_CH3 TIM14_CH1	
8	11	PB4	I/O	COM		USART_TX I^2C_SDA TIM1_BKIN	
9	12	PB3	I/O	COM		USART_CK I^2C_SCL TIM1_ETR CMP1_OUT	
10	13	PB2	I/O	COM		SPI_SCK USART_CTS	

Package		Reset	Port type	Port structure	Notes	Port function	
QFN20 F1	TSSOP20 F1					Multiplexing function	Additional features
						TIM1_CH1N	
						TIM1_CH3	
11	14	PB1	I/O	COM		USART_RTS	ADC_IN0
						TIM1_CH2N	CMP1_INP
						TIM1_CH4	CMP1_INM
						MCO	
12	15	PB0	I/O	COM		SPI_SCK	ADC_IN7
						USART_CK	CMP1_INM
						TIM1_CH2	
						TIM1_CH3N	
13	16	PA0	I/O	COM		SPI_MOSI	
						TIM1_CH1	
14	17	PA1	I/O	COM		SPI_MISO	
						TIM1_CH2	
15	18	PA2(SWCLK)	I/O	COM		USART_RX	
						I^2C_SCL	
						SWCLK	
						TIM1_CH4	
						CMP2_OUT	
16	19	PA3	I/O	COM		USART_TX	ADC_IN1
							CMP2_INP
						TIM1_CH2	CMP2_INM
17	20	PA4	I/O	COM		USART_RX	ADC_IN2
						TIM1_CH3	CMP2_INM
						TIM14_CH1	

Table 3-3 SOP16/SOP14/MSOP10 pin definition

Package type			Reset	Port type	Port structure	Notes	Port function	
SOP16 F1	SOP14 F1	MSOP10 F1					Multiplexing function	Additional features
12	10	8	PA6	I/O	COM		SPI_NSS	ADC_IN3
							USART_TX	

Package type			Reset	Port type	Port structure	Notes	Port function	
SOP16 F1	SOP14 F1	MSOP10 F1					Multiplexing function	Additional features
							EVENTOUT	External_clock_in
13	11	9	PA7	I/O	COM		SPI_MOSI USART_TX USART_RX TIM1_CH4 MCO	ADC_IN4
13	11	9	PC0-NRST	I/O	RST	(1)	SWDIO TIM1_CH1N EVENTOUT	NRST ADC_IN5
14	12	-	PC1-OSCIN	I/O	COM		SPI_MISO	OSCIN
15	13	-	PB7-OSCOUT	I/O	COM		SPI_MOSI TIM14_CH1	OSCOUT
16	14	10	V_{SS}	S			Ground	
10	8	6	PB6(SWDIO)	I/O	COM		SPI_MISO USART_TX I^2C_SDA SWDIO	ADC_IN6
1	1	1	V_{CC}	S			Digital power supply	
2	-	-	PB4	I/O	COM		USART_TX I^2C_SDA TIM1_BKIN	
3	-	-	PB3	I/O	COM		USART_CK I^2C_SCL TIM1_ETR CMP1_OUT	
4	2	4	PB2	I/O	COM		SPI_SCK USART_CTS TIM1_CH1N TIM1_CH3	
5	3	3	PB1	I/O	COM		USART_RTS TIM1_CH2N TIM1_CH4 MCO	ADC_IN0 CMP1_INP CMP1_INM
6	4	2	PB0	I/O	COM		SPI_SCK USART_CK	ADC_IN7

Package type			Reset	Port type	Port structure	Notes	Port function	
SOP16 F1	SOP14 F1	MSOP10 F1					Multiplexing function	Additional features
							TIM1_CH2	CMP1_INM
							TIM1_CH3N	
7	5	-	PA0	I/O	COM		SPI_MOSI	
							TIM1_CH1	
8	6	-	PA1	I/O	COM		SPI_MISO	
							TIM1_CH2	
11	7	5	PA2(SWCLK)	I/O	COM	(2)	USART_RX	
							I^2C_SCL	
							SWCLK	
							TIM1_CH4	
							CMP2_OUT	
9	9	7	PA4	I/O	COM		USART_RX	ADC_IN2 CMP2_INM
							TIM1_CH3	
							TIM14_CH1	

1. Selecting PC0 or NRST/SWDIO is configured through option bytes.
2. After reset (when option byte configures 0/0,0/1,1/0), the two pins of PB6 and PA2 are configured as SWDIO and SWCLK AF function, the former internal pull-up resistor, the latter pull-down resistor is activated.
3. After reset (when option byte configures 1/1), the two pins of PC0 and PA2 are configured as SWDIO and SWCLK AF function, the former internal pull-up resistor, the latter pull-down resistor is activated.

3.1. 3.1. Port A multiplexing function mapping

Table 3-4 Port multiplexing function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI_MOSI	-	TIM1_CH1	-	-	-	-	-
PA1	SPI_MISO	-	TIM1_CH2	-	-	-	-	-
PA2	SWC	USART_RX	TIM1_CH4	-	CMP2_OUT	-	I^2C_SCL	-
PA3	-	USART_TX	TIM1_CH2	-	-	-	-	-
PA4	-	USART_RX	TIM1_CH3	-	-	TIM14_CH1	-	-
PA5	-	USART_CK	TIM1_CH1	-	-	TIM14_CH1	-	-
PA6	SPI_NSS	USART_TX	-	-	-	-	-	EVENTOUT
PA7	SPI_MOSI	USART_TX	TIM1_CH4	USART_RX	MCO	-	-	

3.2. 3.2. Port B multiplexing function mapping

Table 3-5 Port B multiplexing function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI_SCK	USART_CK	TIM1_CH2	TIM1_CH3N	-	-	-	-
PB1	-	USART_RTS	TIM1_CH2N	TIM1_CH4	MCO	-	-	-
PB2	SPI_SCK	USART_CTS	TIM1_CH1N	TIM1_CH3	-	-	-	-
PB3	-	USART_CK	TIM1_ETR	-	CMP1_OUT	-	I^2C_SCL	-
PB4	-	USART_TX	TIM1_BKIN	-	-	-	I^2C_SDA	-
PB5	SPI_NSS	USART_RX	TIM1_CH3	-	-	TIM14_CH1	-	-
PB6	SWD	USART_TX	SPI_MISO	-	-	-	I^2C_SDA	-
PB7	SPI_MOSI	-	-	-	-	TIM14_CH1	-	-

3.3. Port C multiplexing function mapping

Table 3-6 multiplexing function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0-NRST	SWD	-	TIM1_CH1N	-	-	-	-	EVENTOUT
PC1-OSCIN	SPI_MISO	-	-	-	-	-	-	-

4. Memory map

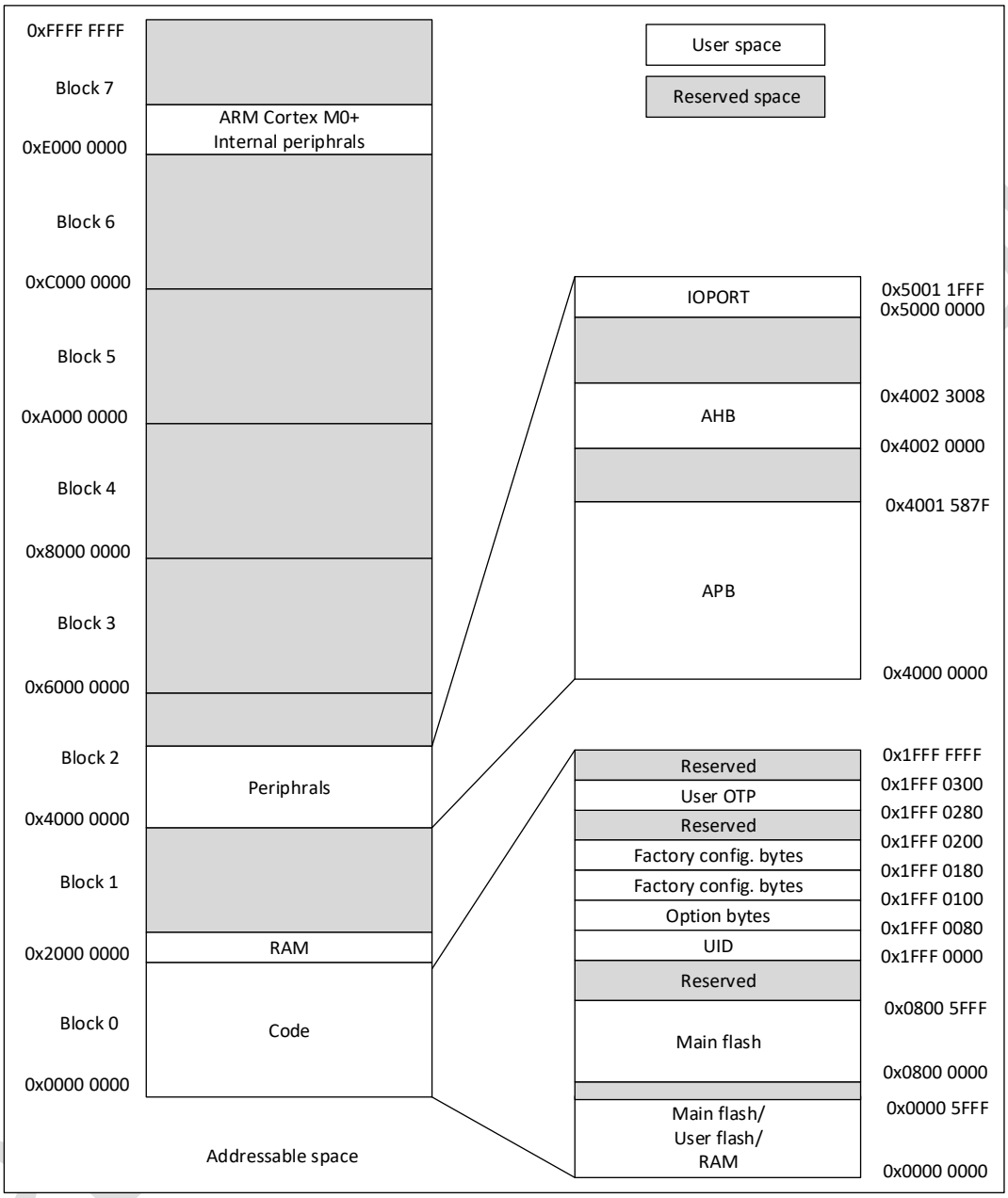


Figure 4-1 Memory map

Table 4-1 Memory address

Type	Boundary Address	Size	Memory Area	Description
SRAM	0x2000 C000-0x3FFF FFFF	-	Reserved	-
	0x2000 0000-0x2000 0BFF	3 KBytes	SRAM	-
Code	0x1FFF 0300-0x1FFF FFFF	-	Reserved	-
	0x1FFF 0280-0x1FFF 02FF	128 Bytes	USER OTP memory	Store user data
	0x1FFF 0180-0x1FFF 01FF	128 Bytes	Factory config. bytes	Sore triming data (include HSI triming data)、Power-on read check code
	0x1FFF 0100-0x1FFF 017F	128 Bytes	Factory config. bytes	Store the HSI trimming data used by users, flash erasing time configuration parameters
	0x1FFF 0080-0x1FFF 00FF	128 Bytes	Option bytes	Chip software and hardware option bytes information
	0x1FFF 0000-0x1FFF 007F	128 Bytes	UID	Unique ID
	0x0800 6000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0800 5FFF	24 KBytes	Main flash memory	-
	0x0000 6000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0000 5FFF	24 KBytes	According to the boot configuration: 1) Main flash memory 2) Load flash 3) SRAM	-

1. Except for 0x1FFF 0E00-0x1FFF 0E7F, the above spaces are marked as reserved spaces, which cannot be written and read as 0 with response error.

Table 4-2 Peripheral register address

Bus	Boundary Address	Size	Peripheral
-	0xE000 0000-0xE00F FFFF	1 Mbytes	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	256 MBytes	Reserved(1)
	0x5000 1400-0x5000 17FF	1 KBytes	Reserved(1)

Bus	Boundary Address	Size	Peripheral
	0x5000 1000-0x5000 13FF	1 KBytes	Reserved(1)
	0x5000 0C00-0x5000 0FFF	1 Kbytes	Reserved(1)
	0x5000 0800-0x5000 0BFF	1 Kbytes	GPIOC
	0x5000 0400-0x5000 07FF	1 Kbytes	GPIOB
	0x5000 0000-0x5000 03FF	1 Kbytes	GPIOA
AHB	0x4002 3400-0x4FFF FFFF	-	Reserved
	0x4002 300C-0x4002 33FF	1 Kbytes	Reserved
	0x4002 3000-0x4002 3008		CRC
	0x4002 2400-0x4002 2FFF	-	Reserved
	0x4002 2000-0x4002 23FF	-	Flash
	0x4002 1C00-0x4002 1FFF	3 KBytes	Reserved
	0x4002 1900-0x4002 1BFF	1 Kbytes	Reserved
	0x4002 1800-0x4002 18FF		EXTI(2)
	0x4002 1400-0x4002 17FF	1 Kbytes	Reserved
	0x4002 1080-0x4002 13FF	1 KBytes	Reserved
	0x4002 1000-0x4002 107F		RCC(2)
	0x4002 0C00-0x4002 0FFF	1 KBytes	Reserved
	0x4002 0040-0x4002 03FF	1 KBytes	Reserved
	0x4002 0000-0x4002 003C		Reserved
APB	0x4001 5C00-0x4001 FFFF	32 KBytes	Reserved
	0x4001 5880-0x4001 5BFF	1 KBytes	Reserved
	0x4001 5800-0x4001 587F		DBG
	0x4001 4C00-0x4001 57FF	3 KBytes	Reserved

Bus	Boundary Address	Size	Peripheral
	0x4001 4850-0x4001 4BFF	1 KBytes	Reserved
	0x4001 4800-0x4001 484C		Reserved
	0x4001 4450-0x4001 47FF	1 KBytes	Reserved
	0x4001 4400-0x4001 404C		Reserved
	0x4001 3C00-0x4001 43FF	2 KBytes	Reserved
	0x4001 381C-0x4001 3BFF	1 KBytes	Reserved
	0x4001 3800-0x4001 3018		USART1
	0x4001 3400-0x4001 37FF	1 Kbytes	Reserved
	0x4001 3010-0x4001 33FF	1 Kbytes	Reserved
	0x4001 3000-0x4001 300C		SPI1
	0x4001 2C50-0x4001 2FFF	1 Kbytes	Reserved
	0x4001 2C00-0x4001 2C4C		TIM1
	0x4001 2800-0x4001 2BFF	1 Kbytes	Reserved
	0x4001 270C-0x4001 27FF	1 Kbytes	Reserved
	0x4001 2400-0x4001 2708		ADC
	0x4001 0400-0x4001 23FF	8 Kbytes	Reserved
	0x4001 0220-0x4001 03FF	1 KBytes	Reserved
	0x4001 0200-0x4001 021F		COMP1/2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 B400-0x4000 FFFF	19 KBytes	Reserved
	0x4000 B000-0x4000 B3FF	1 KBytes	Reserved
	0x4000 8400-0x4000 AFFF	11 KBytes	Reserved
	0x4000 7C28-0x4000 7FFF	1 KBytes	Reserved

Bus	Boundary Address	Size	Peripheral
	0x4000 7C00-0x4000 7C24		LPTIM
	0x4000 7400-0x4000 7BFF	2 KBytes	Reserved
	0x4000 7018-0x4000 73FF	1 KBytes	Reserved
	0x4000 7000-0x4000 7014		PWR(3)
	0x4000 5800-0x4000 6FFF	6 KBytes	Reserved
	0x4000 5434-0x4000 57FF	1 KBytes	Reserved
	0x4000 5400-0x4000 5430		I^2C
	0x4000 4800-0x4000 53FF	3 KBytes	Reserved
	0x4000 441C-0x4000 47FF	1 KBytes	Reserved
	0x4000 4400-0x4000 4418		Reserved
	0x4000 3C00-0x4000 43FF	1 KBytes	Reserved
	0x4000 3810-0x4000 3BFF	1 KBytes	Reserved
	0x4000 3800-0x4000 380C		Reserved
	0x4000 3400-0x4000 37FF	1 KBytes	Reserved
	0x4000 3014-0x4000 33FF	1 KBytes	Reserved
	0x4000 3000-0x4000 0010		IWDG
	0x4000 2C0C-0x4000 2FFF	1 KBytes	Reserved
	0x4000 2C00-0x4000 2C08		Reserved
	0x4000 2830-0x4000 2BFF	1 KBytes	Reserved
	0x4000 2800-0x4000 282C		Reserved
	0x4000 2420-0x4000 27FF	1 KBytes	Reserved
	0x4000 2400-0x4000 241C		Reserved
	0x4000 2054-0x4000 23FF	1 KBytes	Reserved

Bus	Boundary Address	Size	Peripheral
	0x4000 2000-0x4000 0050		TIM14
	0x4000 1800-0x4000 1FFF	2 KBytes	Reserved
	0x4000 1400-0x4000 17FF	1 KBytes	Reserved
	0x4000 1030-0x4000 13FF	1 KBytes	Reserved
	0x4000 1000-0x4000 102C		Reserved
	0x4000 0800-0x4000 0FFF	2 KBytes	Reserved
	0x4000 0450-0x4000 07FF	1 Kbytes	Reserved
	0x4000 0400-0x4000 044C		Reserved
	0x4000 0000-0x4000 03FF	1 KBytes	Reserved

1. The address space marked as Reserved by AHB in the above table cannot be written, read is 0, and a hardfault is generated. The address space marked as Reserved by APB cannot be written, read back as 0, but no hardfault will be generated.
2. Not only supports 32 bits word access, but also supports halfword and byte access.
3. Not only supports 32 bits word access, but also supports half word access

5. Electrical characteristics

5.1. Test conditions

All voltage is referenced to V_{SS} unless otherwise specified.

5.1.1. Min and Max

Unless otherwise specified, the chip is screened by mass production testing at ambient temperature TA =25°C and TA =TA(max), guaranteed to reach the minimum value and maximum value under the worst ambient temperature, supply voltage and clock frequency conditions.

Based on electrical characterization results, design simulations, and/or process parameters noted below the table, not tested in production. Minimum and maximum values are referenced to sample testing and averaged plus or minus three times the standard deviation.

5.1.2. Typical value

Unless otherwise specified, typical data is based on TA =25°C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are obtained by sampling a standard batch, tested under all temperature ranges, and 95% of the chip error is less than or equal to the given value.

5.2. Absolute maximum ratings

If the applied voltage exceeds the absolute maximum value given in the table below, it may cause permanent damage to the chip. Only the strength ratings that can be tolerated are listed here, and it does not imply that the functional operation of the device is correct under these conditions. Operating under maximum conditions for a long time may affect the reliability of the chip.

Table 5-1 Voltage characteristics(1)

Symbol	Describe	Minimum value	Maximum value	Unit
V_{CC}	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	V_{CC}+0.3	V

1. Power supply V_{CC} and ground V_{SS} pins must always be connected to the external power supply within the allowable range.

Table 5-2 Current characteristics

Symbol	Description	Maximum	Unit
I_{VCC}	Total current flowing into V_{CC} pin supply current)(1)	80	mA
I_{VSS}	Total current flowing out of V_{SS} pin (outflow current) (1)	80	mA
$I_{IO(PIN)}$	Output sink current for all IOs	20	mA
	Source current for all IOs	-20	

1. Power supply V_{CC} and ground V_{SS} pins must always be connected to the external power supply within the allowable range.

Table 5-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-65 ~ +150	°C
T_O	Range of working temperature	-40 ~ +85	°C

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Condition	Minimum	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	MHz
V_{CC}	Standard working voltage	-	1.7	5.5	V
V_{IN}	IO input voltage	-	-0.3	V_{CC} + 0.3	V
T_A	Ambient temperature	-	-40	85	°C
T_J	Junction temperature	-	-40	90	°C

5.3.2. Power on and down operating conditions

Table 5-5 Power on and Power down operation conditions

Symbol	Parameter	Condition	Minimum	Maximum value	Unit
t_{VCC}	V_{CC} rise rate	-	0	∞	μs/V
	V_{CC} fall rate	-	20	∞	

5.3.3. Embedded reset module features

Table 5-6 Embedded Reset Module Features

Symbol	Parameter	Condition	Minimum	Typical value	Maximum value	Unit
$V_{POR/PDR}$	POR/PDR reset threshold	Rising edge	1.5	1.6	1.7	V
		Falling edge	1.45	1.55	1.65	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	50	-	mV
V_{BOR}	BOR threshold voltage	BOR_LEV[2:0]=000 (Rising edge)	1.7	1.8	1.9	V
		BOR_LEV[2:0]=000 (Falling edge)	1.6	1.7	1.8	V
		BOR_LEV[2:0]=001 (Rising edge)	1.9	2	2.1	V
		BOR_LEV[2:0]=001 (Falling edge)	1.8	1.9	2	V
		BOR_LEV[2:0]=010 (Rising edge)	2.1	2.2	2.3	V
		BOR_LEV[2:0]=010 (Falling edge)	2	2.1	2.2	V
		BOR_LEV[2:0]=011 (Rising edge)	2.3	2.4	2.5	V
		BOR_LEV[2:0]=011 (Falling edge)	2.2	2.3	2.4	V
		BOR_LEV[2:0]=100 (Rising edge)	2.5	2.6	2.7	V
		BOR_LEV[2:0]=100 (Falling edge)	2.4	2.5	2.6	V
		BOR_LEV[2:0]=101 (Rising edge)	2.7	2.8	2.9	V
		BOR_LEV[2:0]=101 (Falling edge)	2.6	2.7	2.8	V
		BOR_LEV[2:0]=110 (Rising edge)	2.9	3	3.1	V
		BOR_LEV[2:0]=110 (Falling edge)	2.8	2.9	3	V
		BOR_LEV[2:0]=111 (Rising edge)	3.1	3.2	3.3	V
		BOR_LEV[2:0]=111 (Falling edge)	3	3.1	3.2	V
V_BOR_{hyst}	BOR hysteresis	-	-	100	-	mV

1. Guaranteed by design, not tested in production.

2. Data is based on assessment results and is not tested in production.

5.3.4. Operating current characteristics

Table 5-7 Run mode current

Symbol	Condition						Typical value(1)	Maximum value	Unit
	System clock	Frequency	Code	Run	Peripheral clock	FLASH sleep			
I_{DD}(run)	HSI	24 MHz	While(1)	Flash	ON	DISABLE	1.1	-	mA
					OFF	DISABLE	0.9	-	
	LSI	32.768 kHz			ON	DISABLE	160.4	-	μA
					OFF	DISABLE	159.6	-	
	LSI	32.768 kHz			ON	ENABLE	108.3	-	μA
					OFF	ENABLE	107.7	-	

1. Data is based on assessment results and is not tested in production.

Table 5-8 Sleep mode current

Symbol	Condition				Typical value(1)	Maximum value	Unit
	System clock	Frequency	Peripheral clock	FLASH sleep			
IDD(sleep)	HSI	24 MHz	ON	DISABLE	0.8	-	mA
			OFF	DISABLE	0.5	-	
	LSI	32.768 kHz	ON	DISABLE	159.3	-	μA
			OFF	DISABLE	158.9	-	
	LSI	32.768 kHz	ON	ENABLE	85.3	-	μA
			OFF	ENABLE	84.8	-	

1. Data is based on assessment results and is not tested in production.

Table 5-9 Stop mode current

Symbol	Condition				Typical value(1)	Maximum value	Unit
	V_{CC}	MR/LPR	LSI	Peripheral clock			
I_{DD}(stop)	1.7~5.5 V	MR	-	-	75.3	-	μA
			ON	IWDG+LPTIM	1.7	-	
				IWDG	1.7	-	

Symbol	Condition				Typical value(1)	Maximum value	Unit
	V_{CC}	MR/LPR	LSI	Peripheral clock			
				LPTIM	1.7	-	
			OFF	No	1.5	-	

1. Data is based on assessment results and is not tested in production.

5.3.5. Low power mode wake-up time

Table 5-10 Low power mode wake-up time

Symbol	Parameters(1)		Condition	Typical value(2)	Maximum value	unit
$T_{WUSLEEP}$	Wake-up time from sleep		-	0.6	-	μs
T_{WUSTOP}	Wake-up time from stop	Powered by MR	Execute program in Flash, HSI(24 Mhz)as system clock	6.4	-	
		Powered by LPR	Execute program in Flash, HIS as system clock(24 M)	10.6	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.

2. Data is based on assessment results and is not tested in production.

5.3.6. External clock sourse characteristics

5.3.6.1. External high-speed clcok

In the external clock input mode of the HSE, (The HSEEN of RCC_CR is set)， the corresponding IO serves as the external clock input port.

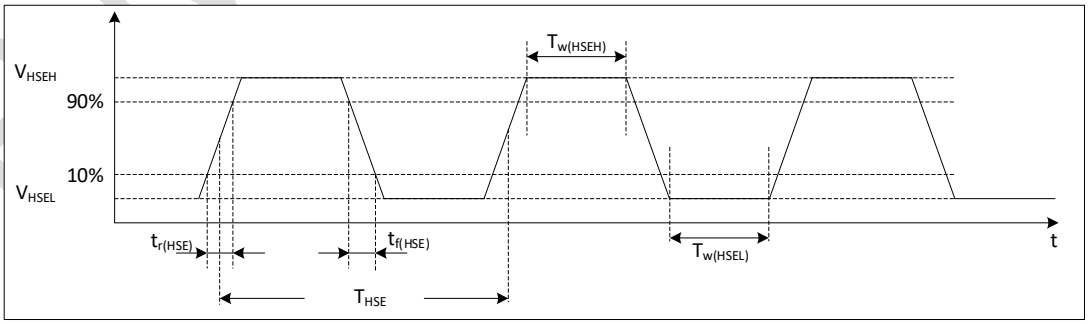


Figure 5-1 External high-speed clock timing diagram

Table 5-11 External high-speed clock features

Symbol	Parameters(1)	Minimum	Typical value	Maximum value	Unit
f_{HSE_ext}	User external clock frequency	0	4	32	MHz
V_{HSEH}	Input pin high level voltage	0.7 * V_{CC}	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	Vss	-	0.3 * V_{CC}	V
$t_{W(HSEH)}$ $t_{W(HSEL)}$	Enter high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Enter the rise or fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

5.3.6.2. External low-speed clock

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), when the low-speed start-up circuit in the chip stops working, the corresponding IO is used as a standard GPIO.

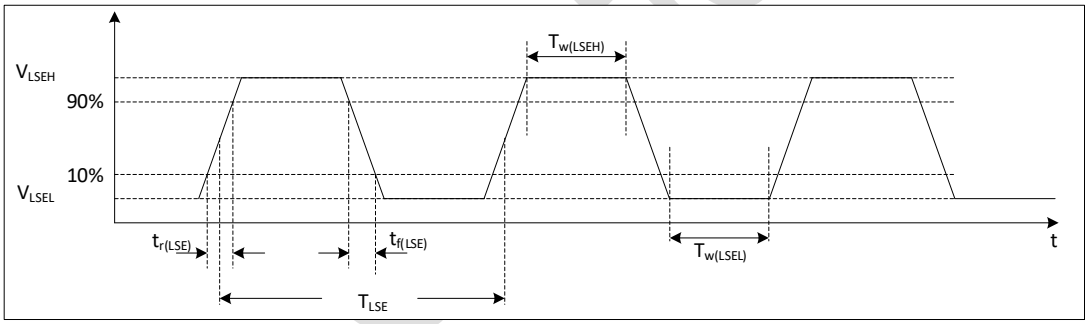


Figure 5-2 External low-speed clock timing diagram

Table 5-12 External low-speed clock features

Symbol	Parameters(1)	Minimum	Typical value	Maximum	Unit
f_{LSE_ext}	User external clock frequency	-	32.768	1000	KHz
V_{LSEH}	Input pin high level voltage	0.7 * V_{CC}	-	-	V
V_{LSEL}	Input pin low level voltage	-	-	0.3 * V_{CC}	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	Enter high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Enter the rise or fall time	-	-	50	ns

1. Guaranteed by design, not tested in production.

5.3.6.3. External low-speed crystal

An external 32.768 KHz crystal/ceramic resonator. In the application, the crystal and load capacitors should be as close as possible to the pins to minimize output distortion and start-up settling time.

Table 5-13 External low-speed crystal characteristics

Symbol	Parameter	Condition(1)	Minimum	Typical value	Maximum	Unit
I_{DD}(4)	LSE power consumption	LSE_DRIVER [1:0] = 00	-	100	-	nA
		LSE_DRIVER [1:0] = 01	-	700	-	
		LSE_DRIVER [1:0] = 10	-	1200	-	
		LSE_DRIVER [1:0] = 11	-	1600	-	
$t_{SU(LSE)}$(3) (4)	Start Time	-	-	3	-	s

1. Crystal/ceramic resonator characteristics are based on the manufacturer datasheet.
2. Guaranteed by design, not tested in production.
3. t_{SU}(LSE) is the start-up time from enable (by software) to the clock oscillation reaches stability, measured for a standard crystal/resonator, which can vary greatly from one crystal/resonator to another.
4. Data is based on assessment results and is not tested in production.

5.3.7. Internal high frequency clock sourse HSI characteristics

Table 5-14 Internal high frequency clock source characteristics

Symbol	Parameter	Condition	Minimum	Typical value	Maximum	Unit
f_{HSI}	HSI frequency	T_A = 25°C,V_{CC} = 3.3 V	23.83(2)	24	24.17(2)	MHz
			47.66(2)	48	48.34(2)	
$\Delta_{Temp(HSI)}$	HSI frequency temperature drift 24 MHz	V_{CC} = 2.0 V ~ 5.5 V T_A = -40°C ~ 85°C	-2(2)	-	2(2)	%
		V_{CC} = 1.7 V ~ 5.5 V T_A = 0°C ~ 85°C	-2(2)	-	2(2)	
		V_{CC} = 1.7 V ~ 5.5 V T_A = -40°C ~ 85°C	-4(2)	-	2(2)	

Symbol	Parameter	Condition	Minimum	Typical value	Maximum	Unit
f_{TRIM}(1)	HSI fine-tuning accuracy	-	-	0.1	-	%
D_{HSI}(1)	Duty cycle	-	45	-	55	%
$t_{Stab(HSI)}$	HSI stabilization time	-	-	2	4(1)	μs
$I_{DD(HSI)}$ (2)	HSI power consumption	24 MHz	-	193	-	μA

1. Guaranteed by design, not tested in production.

2. Date is based on assessment results and is not tested in production.

5.3.8. Internal low frequency clock source LSI characteristics

Table 5-15 Internal low frequency clock characteristics

Symbol	Parameter	Condition	Minimum	Typical value	Maximum	Unit
f_{LSI}	LSI frequency	T_A = 25°C,V_{CC} = 3.3 V	31.6	32.6	33.6	KHz
$\Delta_{Temp(LSI)}$	LSI frequency temperature drift	V_{CC} = 1.7 V ~ 5.5 V T_A = 0°C ~ 85°C	-10(2)	-	10(2)	%
		V_{CC} = 1.7 V ~ 5.5 V T_A = -40°C ~ 85°C	-20(2)	-	20(2)	
f_{TRIM}(1)	LSI fine-tuning accuracy	-	-	0.2	-	%
$t_{Stab(LSI)}$ (1)	LSI stabilization time	-	-	150	-	μs
$I_{DD(LSI)}$ (1)	LSI power consumption	-	-	210	-	nA

1. Guaranteed by design, not tested in production.

2. Data is based on assessment results and is not tested in production.

5.3.9. Mmemory chaeracteristics

Table 5-16 Memory characteristics

Symbol	Parameter	Condition	Typical value	Maximum(1)	Unit
t_{prog}	Page program	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase	-	3.5	5.0	ms

Symbol	Parameter	Condition	Typical value	Maximum(1)	Unit
I_{DD}	Page programe	-	2.1	2.9	mA
	Page/sector/mass erase	-	2.1	2.9	

1. Guaranteed by design, not tested in production.

Table 5-17 Memory erase times and date retention

Symbol	Parameter	Condtion	Minimum(1)	Unit
N_{END}	Erase and write time	T_A = -40°C ~ 85°C	100	Kcycle
t_{RET}	Date retention period	10 Kcycle T_A = 55°C	20	Year

1. Data is based on assessment results and is not tested in production.

5.3.10. EFT characteristics

Symbol	Parameter	Condition	Grade	Typical value	Unit
EFT to IO	-	IEC61000-4-4	A	2	KV
EFT to Power	-	IEC61000-4-4	A	4	KV

5.3.11. ESD & LU characteristics

Table 5-18 ESD & LU characteristics

Symbol	Parameter	Condition	Typical value	Unit
$V_{ESD(HBM)}$	Static Discharge Voltage(human body model)	ESDA/JEDEC JS-001-2017	6	KV
$V_{ESD(CDM)}$	Static Discharge Voltage(charging equipment model)	ESDA/JEDEC JS-002-2018	1	KV
$V_{ESD(MM)}$	Static discharge voltage(machine model)	JESD22-A115C	200	V
LU	Static Latch-Up	JESD78E	200	mA

5.3.12. Port characteristics

Table 5-19 IO static characteristics

Symbol	Parameter	Condtion	Minimum	Typical value	Maximum	Unit
V_{IH}	Input high level voltage	V_{CC} = 1.7 V ~ 5.5 V	0.7 * V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC} = 1.7 V ~ 5.5 V	-	-	0.3 * V_{CC}	V
V_{hys}(1)	Schmitt hysteresis voltage	-	-	200	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}	Pull-up resistor	-	30	50	70	KΩ
R_{PD}	Pull-down resistor	-	30	50	70	KΩ
C_{IO}(1)	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

Table 5-20 Output Voltage Characteristics

Symbol	Parameter(1)	Condtion	Minimum	Maximum value	Unit
V_{OL} (2)	COM IO output low level	I_{OL} = 20 mA, V_{CC} ≥ 5.0 V	-	0.4	V
V_{OL}		I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	-	0.4	V
V_{OL} (2)		I_{OL} = 4 mA, V_{CC} = 1.8 V	-	0.5	V
V_{OH} (2)	COM IO output high level	I_{OH} = 18 mA, V_{CC} ≥ 5.0 V	V_{CC}-0.6	-	V
V_{OH}		I_{OH} = 8 mA, V_{CC} ≥ 2.7 V	V_{CC}-0.4	-	V
V_{OH} (2)		I_{OH} = 4 mA, V_{CC} = 1.8 V	V_{CC}-0.5	-	V

1. IO types can refer to the terms and symbols defined by the pins.

2. Guaranteed by design, not tested in production.

5.3.13. NRST pin characteristics

Table 5-21 NRST pin characteristics

Symbol	Parameter	Condition	Minimum	Typical value	Maximum	Unit
V_{IH}	Input high level voltage	V_{CC} = 1.7 V ~ 5.5 V	0.7 * V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC} = 1.7 V ~ 5.5 V	-	-	0.2 * V_{CC}	V
V_{hys}(1)	Schmitt hysteresis voltage	-	-	300	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}(1)	Pull-up resistor	-	30	50	70	KΩ
R_{PD}(1)	Pull-down resistor	-	30	50	70	KΩ
C_{IO}	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

5.3.14. ADC characteristics

Table 5-22 ADC characteristics

Symbol	Parameter	Condition	Minimum	Typical value	Maximum	Unit
I_{DD}	Power consumption	@1 MSPS	-	300	-	uA
C_{IN}(1)	Internal sample and hold capacitors	-	-	5	-	pF
F_{ADC}	Convert clock frequency	V_{CC} = 1.7 V ~ 2.0 V	1	4	8(2)	MHz
		V_{CC} = 2.0 V ~ 5.5 V	1	8	16(2)	MHz
Tsamp(1)		F_{ADC}=8 MHz	0.438	-	29.94	μs
		V_{CC} = 1.7 V ~ 2.0 V	3.5	-	239.5	1/F_{ADC}
		F_{ADC}=16 MHz	0.219	-	14.97	μs
		V_{CC} = 2.0 V ~ 5.5 V	3.5	-	239.5	1/F_{ADC}
Tconv(1)	-	-	-	12 * Tclk	-	-
Teoc(1)	-	-	-	0.5 * Tclk	-	-
DNL(2)	-	-	-	±2	-	LSB
INL(2)	-	-	-	±3	-	LSB
Offset(2)	-	-	-	±2	-	LSB

1. Guaranteed by design, not tested in production.

2. Data is based on assessment results and is not tested in production.

5.3.15. Comparator characteristics

Table 5-23 Comparator features(1)

Symbol	Parameter	Condition	Minimum	Typical value	Maximum	Unit
V_{IN}	Input voltage range	-	0	-	V_{CC}-1.5	V
t_{START}	Startup time to reach propagation delay specification	-	-	-	5	μs
t_D	Propagation delay	Output low to high	-	-	200	ns
		Output high to low	-	-	150	
V_{offset}	Offset error	-	-	±5	-	mV
V_{hys}	hysteresis	No hysteresis	-	0	-	mV
I_{DD}	Consumption	-	-	70	-	μA

1. Guaranteed by design, not tested in production.

5.3.16. Temperature sensor characteristics

Table 5-24 Temperature sensor characteristics

Symbol	Parameter	Minimum	Typical value	Maximum	Unit
T_L(1)	VTS linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5°C)	0.74	0.76	0.78	V
t_{START}(1)	Start-up time entering in continuous mode	-	70	120	μs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	μs

1. Guaranteed by design, not tested in production.

2. Data is based on assessment results and is not tested in production.

5.3.17. Internal reference voltage characteristics

Table 5-25 Internal reference voltage characteristics

Symbol	Parameter	Minimum	Typical value	Maximum	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$T_{start\_vrefint}$	Start time of internal reference voltage	-	10	15	μs
T_{coeff}	Temperature coefficient	-	-	100(1)	ppm/°C
I_{vcc}	Current consumption from V_{CC}	-	12	20	μA

1. Guaranteed by design, not tested in production.

5.3.18. ADC internal reference voltage characteristics

Table 5-26 Internal reference voltage characteristics

Symbol	Parameter	Condition	Minimum	Typical value	Maximum	Unit
VREF15	Internal 1.5 V reference voltage	T_A = 25°C V_{CC} = 3.3 V	1.485	1.5	1.515	V
T_{coeff}	Temperature coefficient	T_A = -40°C ~ 85°C	-	-	120(1)	ppm/°C
$T_{start\_VREFBUF}$	Start time of internal reference voltage	-	-	10	15	μs

1. Guaranteed by design, not tested in production.

5.3.19. COMP internal reference voltage characteristics (4bit DAC)

Table 5-28 Internal reference voltage characteristics

Symbol	Parameter	Condition	Minimum	Typical value	Maximum	Unit
ΔV_{abs}	Absolute variation	-	-	-	±0.5	LSB

Symbol	Parameter	Condition	Minimum	Typical value	Maximum	Unit
$T_{start\_VREFCMP}$	Start time of internal reference voltage	-	-	10	15	μs

1. Guaranteed by design, not tested in production.

5.3.20. Timer characteristics

Table 5-27 Timer characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	41.667	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 24 MHz	-	12	
Res_{TIM}	Timer resolution	TIM1/14	-	16	bit
$t_{COUNTER}$	16 bits counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	0.041667	2730	μs

Table 5-28 LPTIM characteristics (clock selection LSI)

Prescaler	PRESC[2:0]	Minimum overflow value	Maximum overflow value	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table 5-29 IWDG characteristics (clock selection LSI)

Prescaler	PR[2:0]	Minimum overflow value	Maximum overflow value	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

5.3.21. Communication port characteristics

5.3.21.1. I²Cbus interface features

I²C interface meets the requirements of the I²C bus specification and user manual:

- Standard-mode (Sm): 100 Kbit/s
- Fast-mode (Fm): 400 Kbit/s

Timing is guaranteed by design, provided the I²C peripheral is properly configured and the I²C CLK frequency is greater than the minimum required in the table below.

Table 5-30 Minimum I²C CLK frequency

Symbol	Parameter	Condition	Minimum	Unit
$f_{I2CCLK(min)}$	Minimum I²C CLK freq uency	Standard-mode	2	MHz
		Fast-mode	9	

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-31 I²C filter characteristics

Symbol	Parameter	Minimum	Maximum	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

5.3.21.2. Serial Peripheral Interface SPI Characterisitcs

Table 5-32 SPI characteristics

Symbol	Parameter	Condition	Minimum	Maimum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	24	MHz
		Slave mode	-	12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	-	-	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode, f_{PCLK} = 48 MHz,presc = 4	-	-	ns
		Slave mode, f_{PCLK} = 48 MHz,presc = 4	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	-	-	ns
$t_{h(SI)}$		Slave mode	-	-	
$t_{a(SO)}$	Data output access time	Slave mode, presc = 4	-	-	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	-	-	ns
$t_{v(SO)}$	Data output valid ime	Slave mode (after enable edge), presc = 4	-	-	ns
$t_{v(MO)}$	Data output valid ime	Master mode (after enable edge)	-	-	ns
$t_{h(SO)}$	Data output hold time	Slave mode, presc = 4	-	-	ns
$t_{h(MO)}$		Master mode	-	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

1. The Master generates 1 pclk to receive control signal before the receive edge.
2. Slave has a maximum of 1 PCLK based on the sending edge of SCK delay, considering IO delay, etc., define 1.5 PCLK.
3. In the case that the SCK duty cycle sent by the Master is wide between the receiving edge and the sending edge, the Slave updates the data before the sending edge.

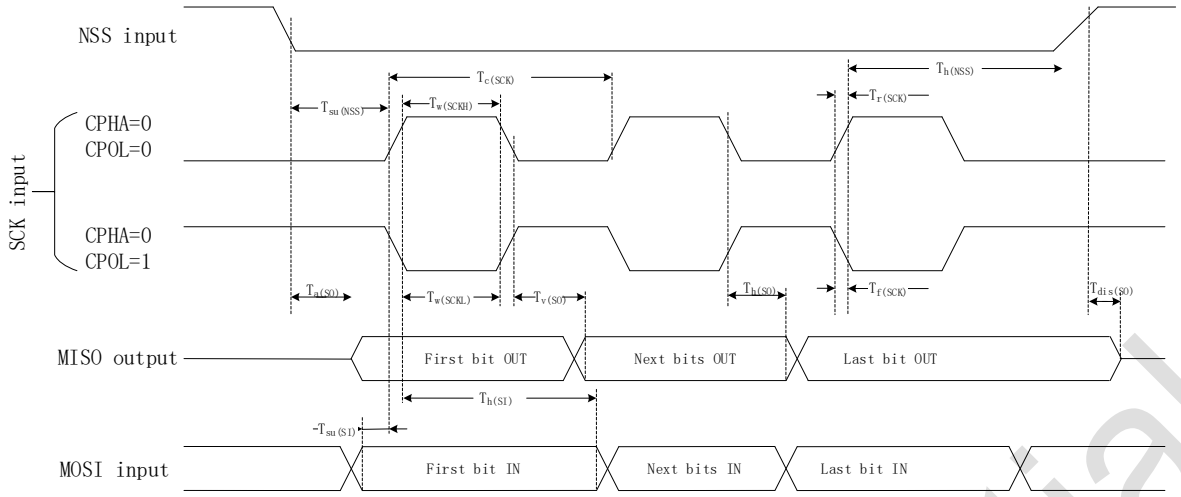


Figure 5-3 SPI timing diagram–slave mode and CPHA=0

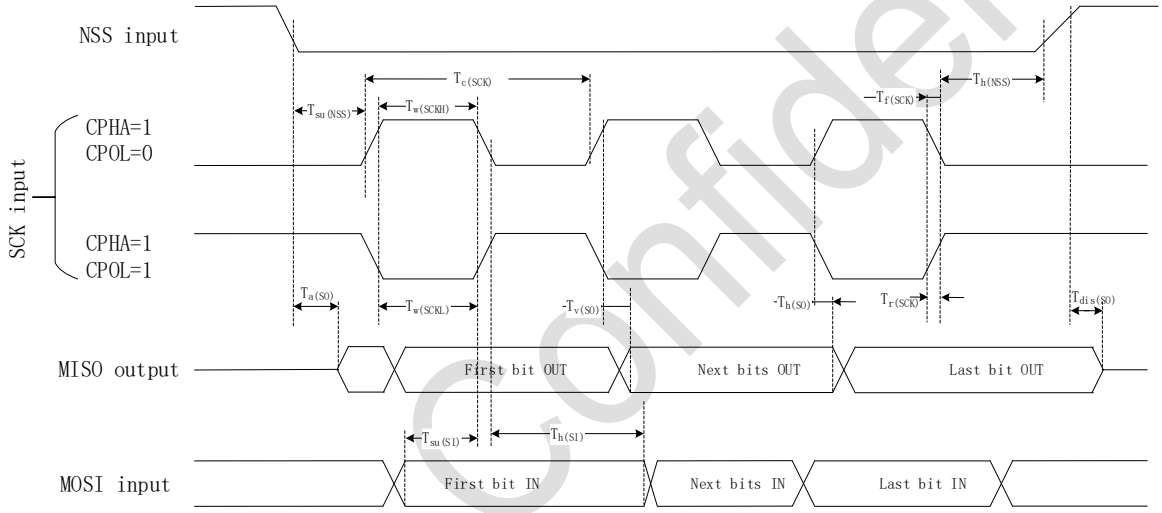


Figure 5-4 SPI timing diagram–slave mode and CPHA=1

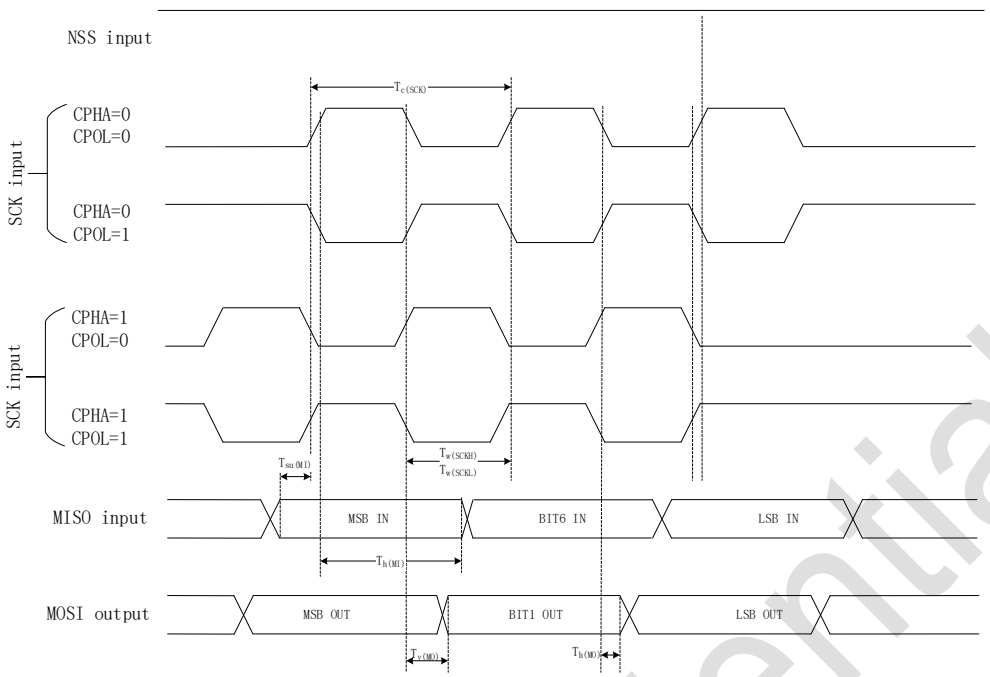


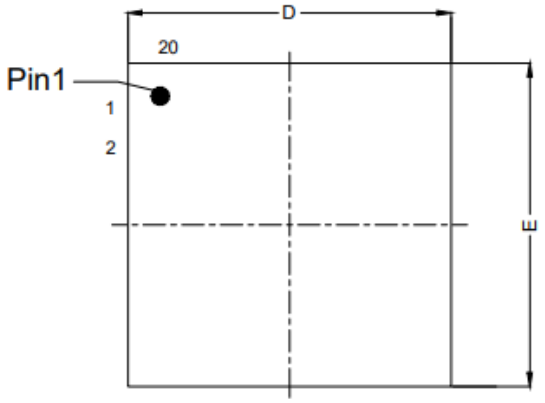
Figure 5-5 SPI timing diagram–master mode

6. Package information

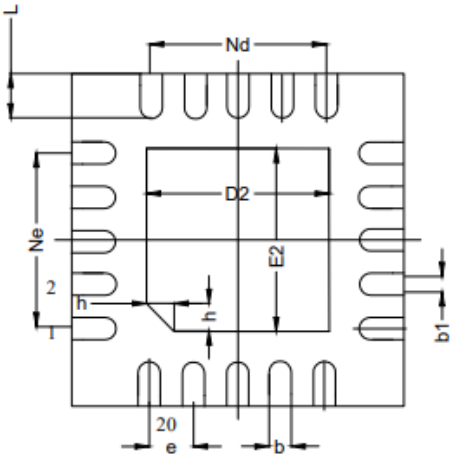
6.1. QFN20 package information

TOP VIEW

SIDE VIEW



BOTTOM VIEW



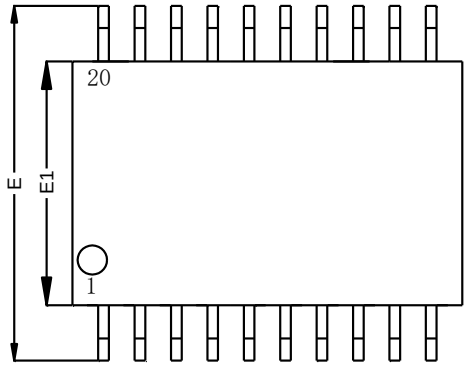
Common Dimensions
(Unit of Measure=millimeters)

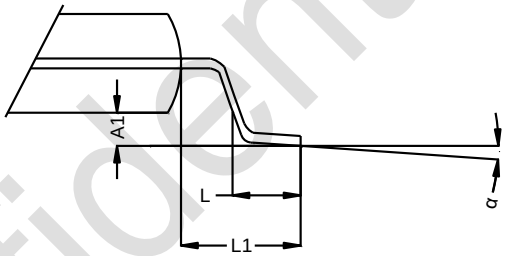
Symbol	Min	Typ	Max
A	0.450	0.500	0.550
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c		0.127REF	
D	2.900	3.000	3.100
D2	1.600	1.700	1.800
E	2.900	3.000	3.100
E2	1.600	1.700	1.800
e		0.400BSC	
Nd		1.600BSC	
Ne		1.600BSC	
L	0.300	0.350	0.400
h	0.250	0.300	0.350

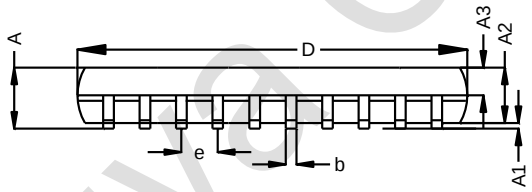
Note: 1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN20L 3x3X0.50-0.4PITCH POD	QRPD-0054	1.0

6.2. TSSOP20 package information







Common Dimensions

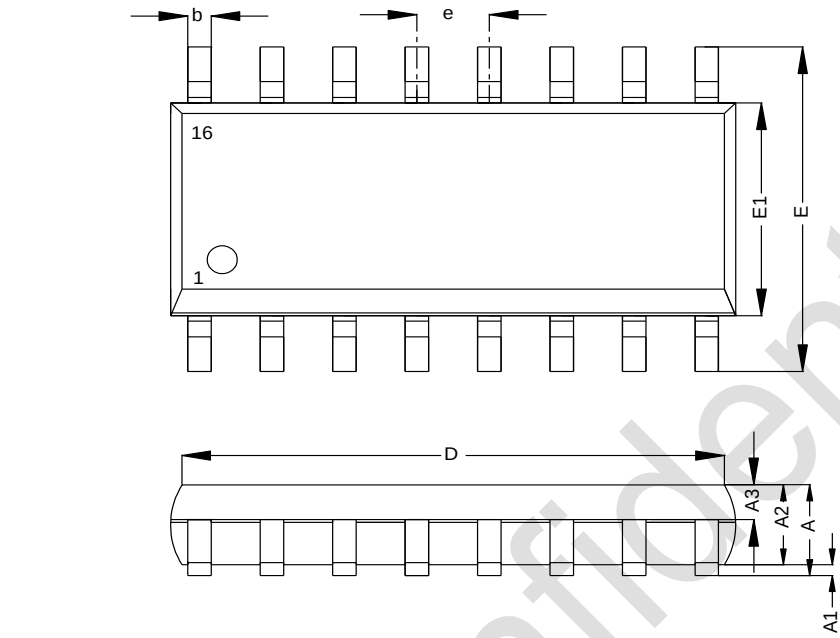
(Unit of Measure=millimeters)

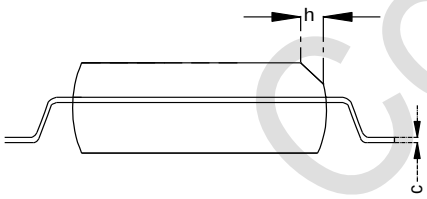
Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
A3	0.340	0.440	0.540
b	0.200	-	0.280
c	0.100	-	0.190
D	6.400	6.500	6.600
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	0.650BSC		
L	0.450	0.600	0.750
L1	1.000REF		
θ	0	-	8°

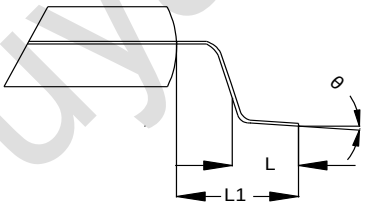
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	TSSOP20	TSSOP-20	B

6.3. SOP16 package information







Common Dimensions

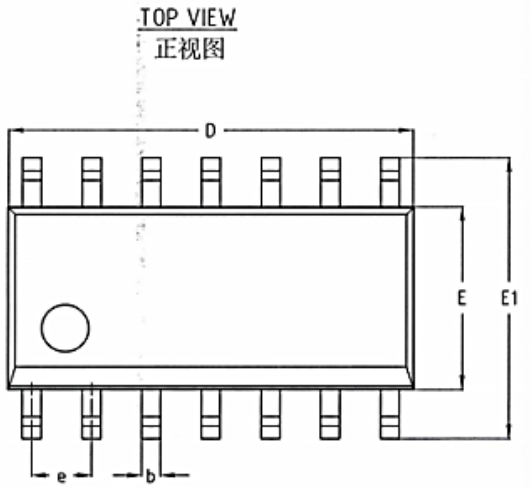
(Unit of Measure=millimeters)

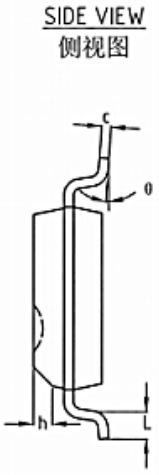
Symbol	Min	Typ	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.30	-	-
A3	0.60	-	0.70
b	0.31	-	0.51
c	0.10	-	0.25
D	9.80	-	10.20
E	5.80	-	6.20
E1	3.80	-	4.20
e	1.27BSC		
L	0.40	-	1.27
L1	1.05REF		
θ	0	-	8°
h	0.25	-	0.50

Note: Dimensions are not to scale.

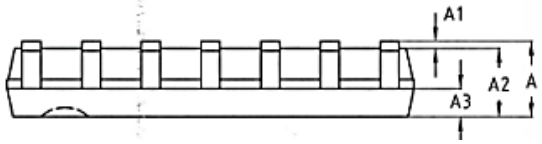
	TITLE	DRAWING NO.	REV
PUYA	PUYA SOP16 (150mil) POD	PY-POD-0001	1.0

6.4. SOP14 package information

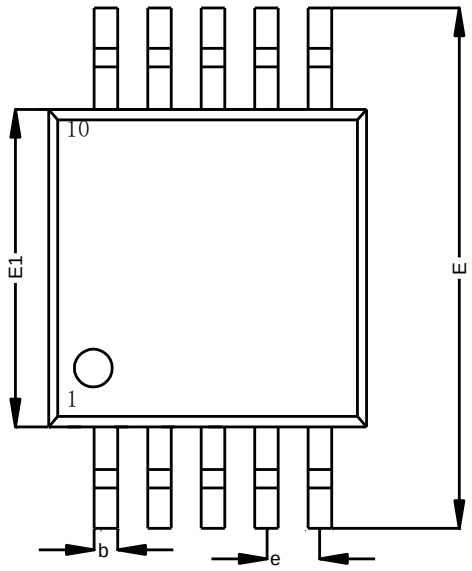


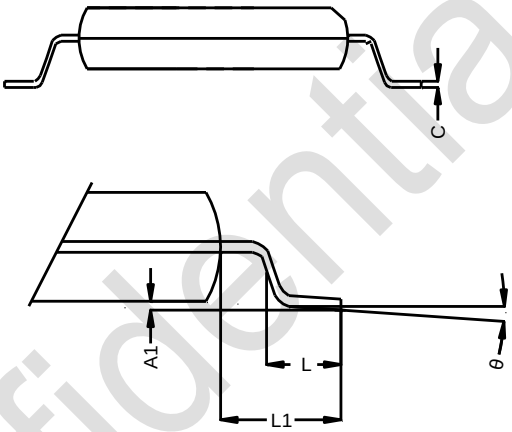


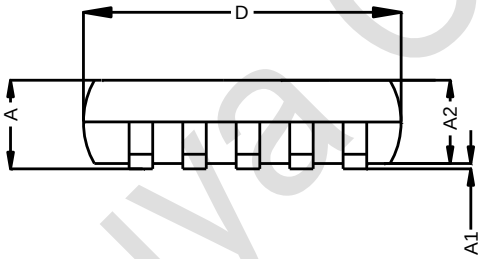
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.35	-	0.50
c	0.19	-	0.25
D	8.50	8.60	8.70
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	-	0.50
L	0.40	-	0.80
θ	0°	-	8°



6.5. MSOP10 package information







Common Dimensions

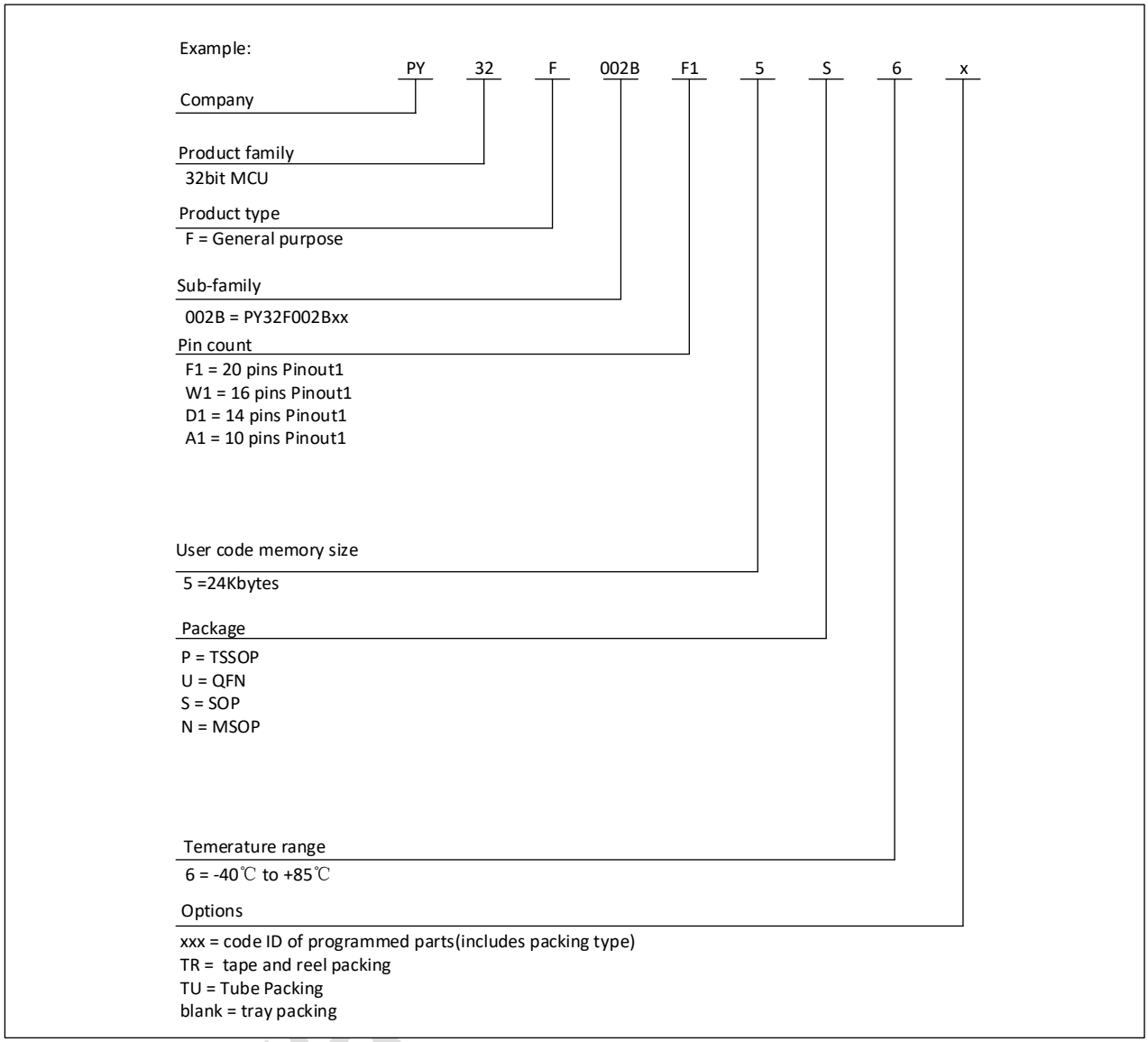
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.100
A1	0.050	-	0.150
A2	0.750	0.850	0.950
b	0.180	-	0.270
c	0.150	-	0.200
D	2.900	3.000	3.100
E	4.700	4.900	5.100
E1	2.900	3.000	3.100
e	-	0.500	-
L	0.400	-	0.700
L1	-	0.950	-
θ	0	-	8°

Note：1. Dimensions are not to scale

PUYA	TITLE Puya MSOP10 POD	DRAWING NO. QRPD-0049	REV 1.0

7. Ordering inforamation



8. Version history

Version	Date	Description
V0.1	2022.12.16	Initial version
V0.2	2023.05.06	Added cover
V0.3	2023.07.07	Updated Tables 3-1 and 5-8

Puya Semiconductor Co., Ltd.