1. Features

- Core
  - ARM® 32-bit Cortex®-M0+ CPU
  - Up to 72 MHz operating frequency
- Memories
  - Maximum 128K/96K/64K/32K bytes Flash memory
  - Maximum 32K/24K/16K/8K bytes SRAM
- Clock management
  - External 4 to 32 MHz high speed crystal oscillator (HSE)
  - External 32.768 kHz low-speed crystal oscillator (LSE)
  - Internal 4/8/16/22.12/24 MHz high speed clock (HSI)
  - Internal 32 kHz low speed clock (LSI)
  - PLL (supports 2/3 multiplication of HSI or HSE)
- Power management and reset
  - Operating voltage: 1.7 V to 5.5 V
  - Low power modes : Sleep and Stop
  - Power-on/power- down reset (POR/PDR)
  - Brown-out reset (BOR)
  - Programmable voltage detection (PVD)
- General-purpose input and output (I/O)
  - Up to 58 I/Os, all available as external interrupts
  - Drive current 8 mA
- 7-channel DMA controller
- One 12-bit ADC
  - Up to 16 external input channels
  - Input voltage conversion range: 0 to VCC
- One 12-bit DAC, supports 2 channels
- 3 analog comparators
- 3-channel operational amplifier
- Support 8*36/4*40 LCD
- 13 timers
  - One 16-bit advanced-control timer (TIM1)
  - One 32-bit general-purpose timer (TIM2)
  - Five 16-bit general-purpose timers (TIM3/14/15/16/17)
  - Two basic timers (TIM6/TIM7)
  - A low power timer (LPTIM)
  - A independent watchdog timer (IWDT)
  - A window watchdog timer (WWDT)
  - A SysTick timer
- RTC
- Communication interfaces
  - Two serial peripheral interfaces (SPI) with I2S function
  - Four universal synchronous/asynchronous Transceivers (USARTs) , support auto baud rate detection, two of USARTs support ISO7816, LIN and IrDA
  - Two I2C interfaces supporting standard mode (100 kHz), Fast mode (400 kHz), 7-bit/10-bit addressing mode and SMBus
  - USB 2.0 full-speed interface
  - CAN 2.0B standard communication interface
- Hardware CRC-32 module
- Hardware 32-bit divider
- Unique UID
- Serial wire debug (SWD)
- Working temperature: -40 to 85℃
- Package: LQFP64, LQFP48, QFN32, LQFP32

Content

2. Introduction

PY32F072 series microcontrollers are MCUs with high-performance ARM® 32-bit Cortex®-M0+ core, wide range of operating voltage. It has embedded up to 128 Kbytes flash and 32 Kbytes SRAM memory, the maximum operating frequency is 72 MHz, and contains various products in different package types. The chip integrates multi-channel I2C, SPI, USART and other communication peripherals, one 12-bit ADC, one DAC, 13 timers, one USB2.0, one CAN, three comparators, five operational amplifiers, and one LCD driver.

The devices operate within ambient temperatures from -40 to 85°C and with supply voltages from 1.7 V to 3.6 V. The chip provides sleep and stop low-power operating modes, which can meet different low-power applications.

The devices are suitable for various application scenarios, such as controllers, portable devices, PC peripherals, gaming and GPS platforms, industrial applications.

Table 2-1 PY32F072 series device features and peripheral counts

Peripheral		**PY32F072Cx(64pin)**				**PY32F072Rx(48pin)**				**PY32F072Kx(32pin)**			
Flash memory (Kbyte)		32	64	96	128	32	64	96	128	32	64	96	128
SRAM (Kbyte)		8	16	24	32	8	16	24	32	8	16	24	32
Timers	Advanced control	1 (16-bit)											
	General purpose	5 (16-bit) 1(32-bit)											
	Basic	2											
	Low-power	1											
	SysTick	1											
	Watchdog	2											
Comm. intefaces	SPI[I2S]	2[2]											
	I2C	2											
	USART	4											
	CAN	1											
	USB	1											
DMA		7ch											
RTC		Yes											

GPIOs	58(64-6pg)	42(48-6pg)	28(32-4pg)
12-bit ADC channels (external + internal)	1 (16 ext. + 5 int.)	1 (13 ext. + 5 int.)	1 (10 ext. + 5 int.)
12-bit DAC (number of channels)	1 (2)		
Analog Comparator	3		
Operational Amplifiers	3		
LCD Controller	1		
Max. CPU frequency	72 MHz		
Operating voltage	1.7 to 5.5 V		
Operating temperature	Ambient: -40 to 85 °C / Junction: -40 to 105 °C		
Packages	LQFP64	LQFP48	QFN32，LQFP32

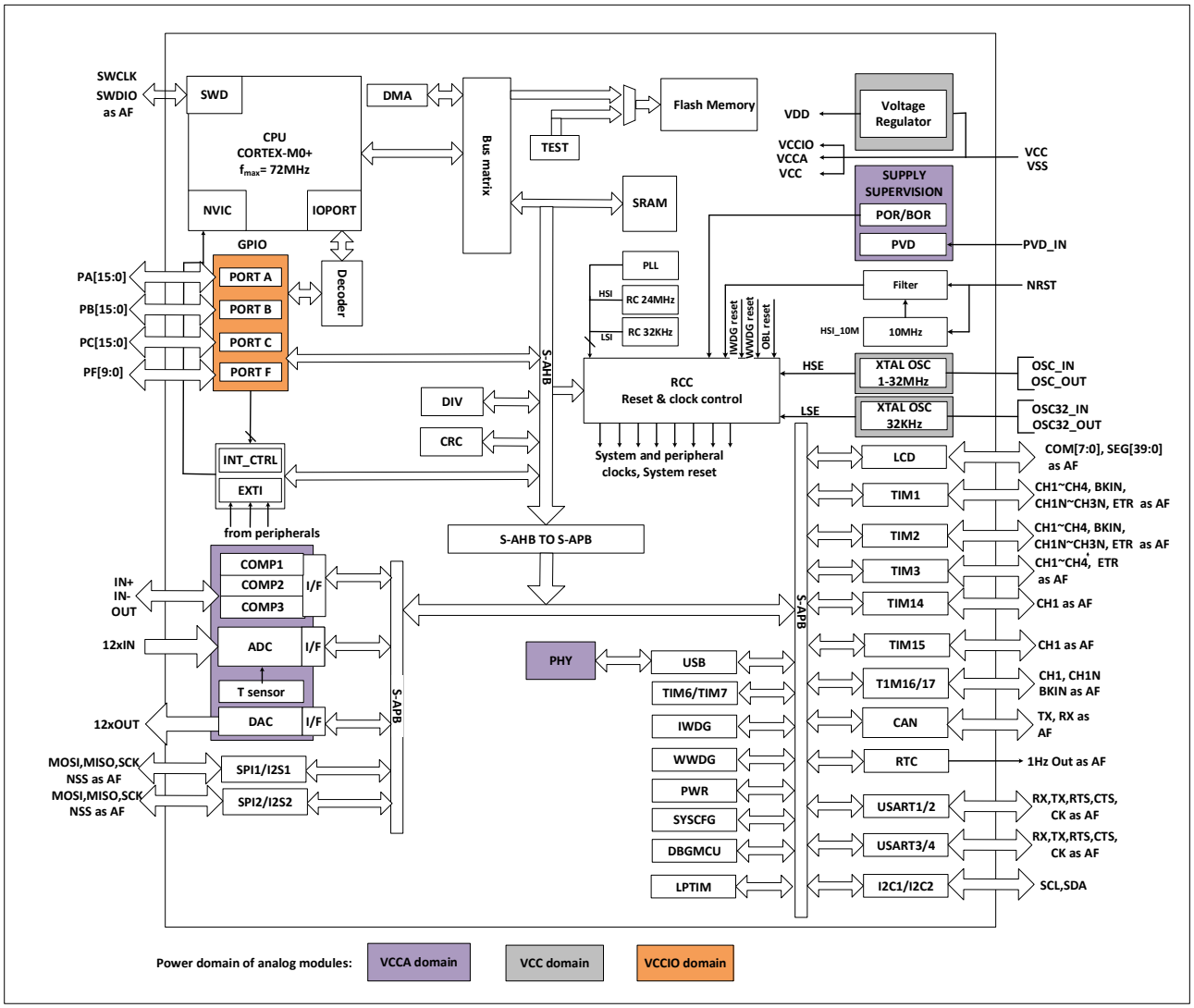


Figure 2-1 System block diagram

3. Functional overview

3.1. Arm®-Cortex®-M0+ core

The Arm® Cortex® -M0+ is an entry-level Arm 32-bit Cortex processor designed for a wide range of embedded applications. It provides developers with significant benefits, including:

- Simple structure, easy to learn and program
- Ultra-low power consumption, energy-saving operation
- Reduced code density and more

Cortex-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. The processor offers high-end processing hardware, including single-cycle multipliers, through a streamlined but powerful instruction set and an extensively optimized design. Moreover, it delivers the superior performance expected from a 32-bit architecture computer, with a higher coding density than other 8 and 16-bit microcontrollers.

The Cortex-M0+ is tightly coupled with a Nested Vectored Interrupt Controller (NVIC).

3.2. Memories

The on-chip integrated SRAM is accessed by bytes (8 bits), half-word (16bits) or word (32bits).

The on-chip integrated Flash consists of two different physical areas:

- Main flash area contains application and user data
- Information area has 12 kbytes, and it includes the following parts:
  - Option bytes
  - UID bytes
  - System memory

The protection of Flash main memory includes the following mechanisms:

- Read protection (RDP) prevents outside access.
- Wrtie protection (WRP) prevents unwanted writes (confuse by program memory pointer from PC). The minimum protection unit for write protection is 8 Kbytes .
- Option byte write protection is a special design for unlock.

3.3. Boot modes

At startup, the BOOT0 pin and boot selector option bit nBOOT are used to select one of the three boot options in the following table:

Table 3-1Boot configuration

Boot mode configuration		Mode
nBOOT1 bit	BOOT0 pin	
X	0	Main Flash as the boot area
1	1	System memory as the boot area
0	1	SRAM as the boot area

The Boot loader is located in the System memory and is used to download the Flash program through the USART interface.

3.4. Clock system

At startup, the default system clock frequency is HSI 8 MHz, and after the program is operating the system clock frequency and system clock source can be reconfigured. The high frequency clocks that can be selected are:

- A 4/8/16/22.12/24 MHz configurable internal high precision HSI clock
- A 32 kHz configurable internal LSI clock
- A 4 to 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. Simultaneously, CPU NMI interrupt is generated.
- A 32.768 kHz LSE clock.
- PLL clock has HSI and HSE sources. If the HSE source is selected, when CSS is enabled and CSS fails, the PLL and HSE will be turned off, and the hardware selects the system clock source as HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. AHB and APB clock frequencies up to 72 MHz.

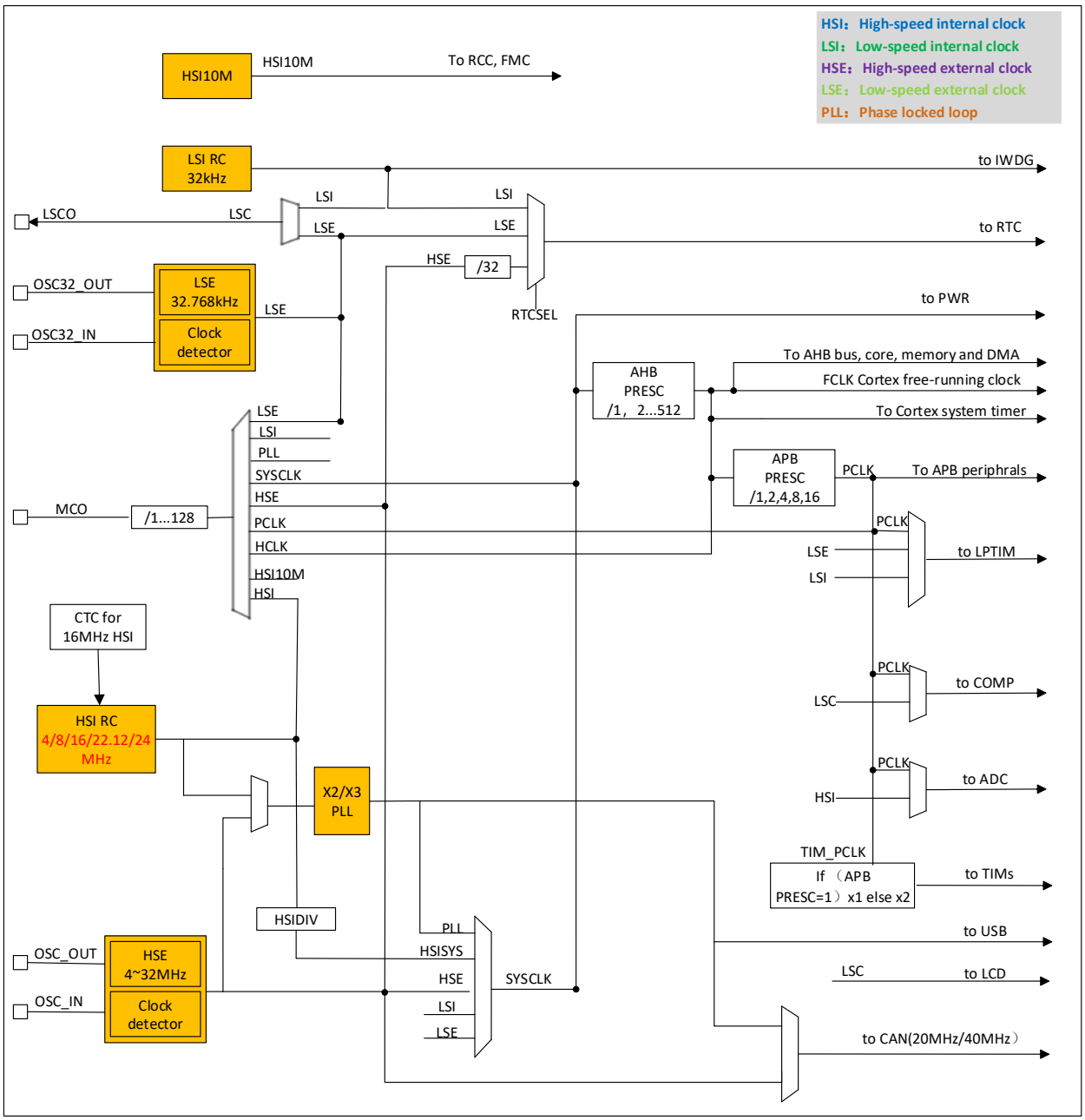


Figure 3-1 System Clock Structure Diagram

3.5. Power management

3.5.1. Power block diagram

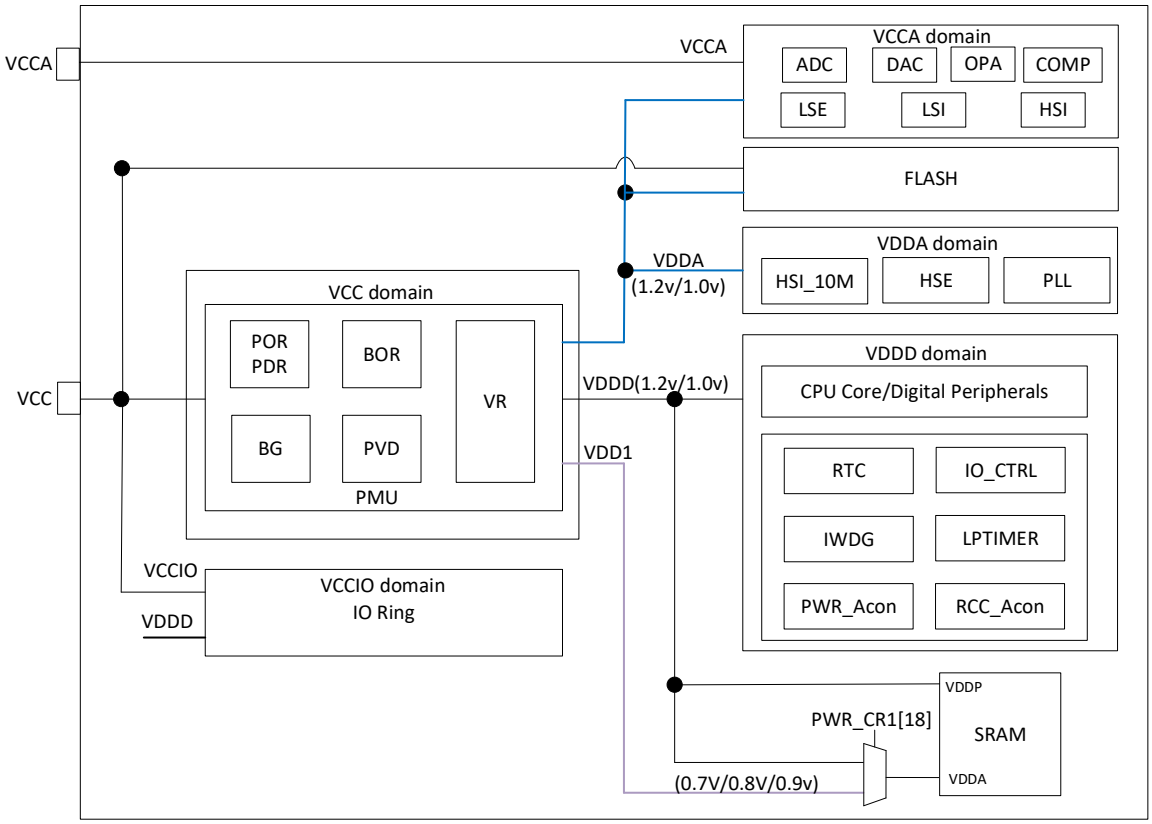


Figure 3-2 Power block diagram

Table 3-2 Power Block Diagram

Num-bering	Power supply	Power value	Describe
1	VCC	1.7 to 5.5 V	The chip is supplied power through the power pins.
2	VDDD	1.2/1.0 V ± 10 %	VR supplies power to the main logic circuits and SRAM inside the chip. When the MR is powered, it outputs 1.2 V. According to the software configuration, when entering the stop mode it powered by MR or LPR, and the LPR output is determined to be 1.2 V or 1.0 V.
3	VCCA	1.7 to 5.5 V	The chip is supplied analog power through the power pins.

3.5.2. Power monitoring

3.5.2.1. Power on reset (POR/PDR)

The power-on reset (POR) and power-down reset (PDR) module is designed in the chip to provide power-on and power-off reset for the chip. The module keeps working in all modes.

3.5.2.2. Brown-out reset (BOR)

In addition to POR/ PDR, BOR (brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte .

When the BOR is turned on, the BOR threshold can be selected by the Option byte, and both the rising and falling detection points can be configured individually.

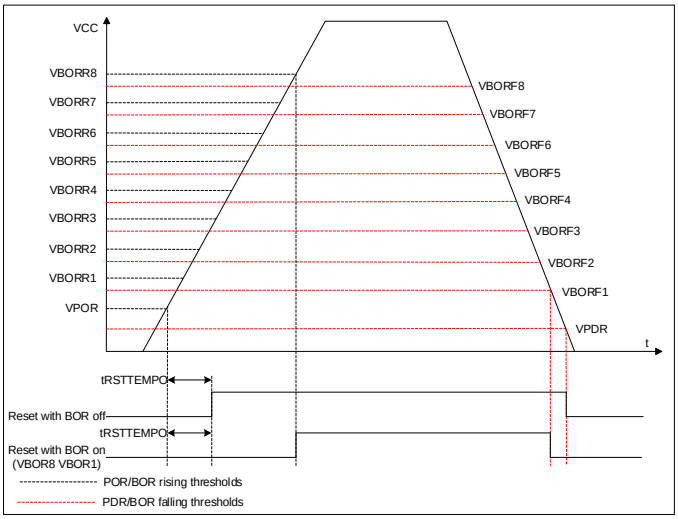


Figure 3-3 POR/PDR/BOR threshold

3.5.2.3. Programmable voltage detection (PVD)

Programmable voltage detector (PVD) module can be used to detect the VCC power supply and the voltage of the PB7 pin, and the detection point is configured through the register. When VCC is higher or lower than the detection point of PVD , the corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI , depending on the rising/falling edge configuration of EXTI line 16, when VCC rises above the detection point of PVD, or VCC falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

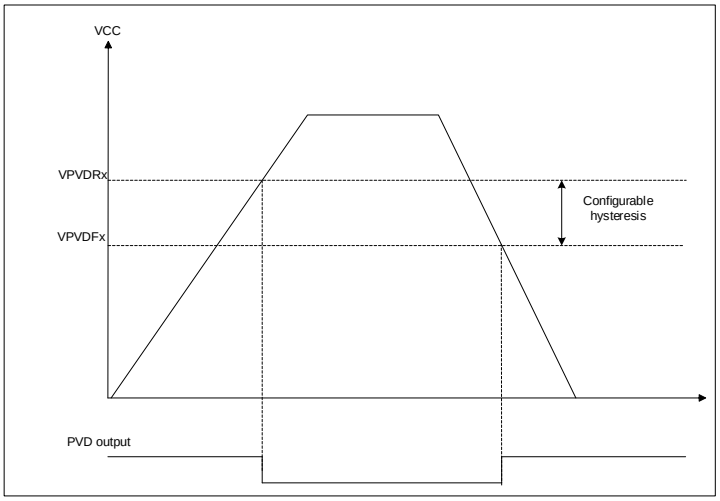


Figure 3-4 PVD threshold

3.5.3. Voltage regulator

The regulator has two operating modes:

- Main regulator (MR) is used in normal operating mode.
- Low power regulator (LPR) can be used in Stop mode where the power demand is reduced.

3.5.4. Low-power mode

In addition to the normal operating mode, the chip has 2 low-power modes:

- Sleep mode: Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.
- Stop mode: In this mode, the contents of SRAM and registers are maintained, HSI and HSE are turned off, and most modules of clocks in the VDD domain are stopped. GPIO, PVD, COMP output, RTC and LPTIM can wake up stop mode.

3.6. Reset

Two resets are designed in the chip: power reset and system reset.

3.6.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out Reset (BOR)

3.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load reset (OBL)
- Power reset (POR/PDR, BOR)

3.7. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function, locking mechanism will freeze I/Os configuration function .

3.8. Hardware divider (DIV)

Hardware divider is a 32-bit signed/unsigned integer hardware divider.

DIV feture:

- Configurable signed/unsigned integer division calculation
- 32-bit dividend, 32-bit divisor
- Output 32-bit quotient and 32-bit remainder
- Division zero warning flag, division end flag
- 8 clock cycles to complete a division operation
- Write the divisor register to trigger the division operation to start
- Automatically wait for the end of the calculation when reading the quotient register/remainder register

3.9. Direct memory access controller (DMA)

Direct Memory Access (DMA) provides high-speed data transfer between peripherals and memory or between memory and memory.

DMA controller has three channels, and each channel is responsible for managing memory access requests from one or more peripherals. The DMA controller includes an arbiter for handling DMA requests for each DMA request's priority..

DMA supports circular buffer management, eliminating the need for user code to intervene when the controller reaches the end of the buffer.

Each channel is directly connected to a dedicated hardware DMA request, and each channel also supports software triggering. These functions are configured through software.

DMA is available for peripherals: TIMERs, SPI, I2C, USART , ADC, DAC, CAN, USB GPIO DIV.

3.10. Interrupts and events

The PY32F072 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

3.10.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed

in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a high-priority interrupt event occurs and a low-priority interrupt event is just waiting to be serviced, the later-arriving high-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a high-priority ISR and then starting a pending low-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Supports one NMI interrupt
- Support 32 maskable external interrupts
- Supports 10 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

3.10.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from stop mode.

The EXTI controller has multiple channels, including a maximum of 16 GPIOs, 1 PVD output, 3 COMP outputs, RTC and LPTIM wake-up signals. GPIO, PVD and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.

Each EXTI line can be independently masked through registers.

The EXTI controller can capture pulses shorter than the internal clock period.

Registers in the EXTI controller latch each event. Even in stop mode, after the processor wakes up from stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

3.11. Analog-to-digital converter (ADC)

The chip has a 12-bit SARADC. The module has up to 18 channels to be measured, including 16 external channels and 5 internal channels. The reference voltage can be selected with precision voltage (1.5 V, 2.048 V or 2.5 V) or the power supply voltage.

The conversion mode of each channel can be set to single, continuous, sweep, discontinuous mode. Conversion results are stored in left or right-aligned 16-bit data registers.

An analogue watchdog allows the application to detect if the input voltage exceeds a user-defined high or low threshold.

The ADC has been implemented to operate at a low frequency, resulting in lower power consumption.

At the end of sampling, conversion, and continuous conversion, an interrupt request is generated when the conversion voltage exceeds the threshold when simulating the watchdog.

3.12. Digital-to-analog converter (DAC)

The two 12-bit 1MSPS DAC capable of digital-to-analog conversion.

3.13. Comparators (COMP)

Three general purpose comparators are integrated in the chip, namely COMP1/2/3. These two or three modules can be used as separate modules or combined with timer.

Comparators can be used as follows:

- Triggered by analog signal to generate low-power mode wake-up function
- Analog signal conditioning
- Cycle by cycle current control loop when connected with PWM output from timer

3.14. Operational amplifier (OPA)

The OPA1/2/3 modules can be flexibly configured for simple filter and buffer applications.

3.15. Liquid crystal display (LCD) controller

LCD controller is a digital controller/driver for monochrome passive liquid crystal displays with up to 8 common terminals (COM) and 40 segment terminals (SEG) to drive 160 (4x40) or 288 (8x36) LCD picture elements. The exact number of terminals depends on the device pinout as described in the datasheet.

3.16. Timer

The characteristics of different timers of PY32F072 series are shown in the following table:

Table 3-3 Timer features comparsion

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA	Capture /compare channels	Comple-mentary outputs
Advanced control	TIM1	16-bit	Up, down, center aligned	Integer from 1 to 65536	Support	4	3
General purpose	TIM2	32-bits	Up, down, center	Integer from 1 to 65536	Support	4	-

			aligned				
General purpose	TIM3	16-bit	Up, down, center aligned	Integer from 1 to 65536	Support	4	-
	TIM14	16-bit	Up	Integer from 1 to 65536	-	1	-
	TIM15, TIM16, TIM17	16-bit	Up	Integer from 1 to 65536	Support	1	1
Basic	TIM6, TIM7	16-bit	Up	Integer from 1 to 65536	Support	-	-

3.16.1. Advanced-control timer (TIM1)

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

TIM1 includes 4 independent channels:

- Input capture
- Output comparison
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If TIM1 is configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

TIM1 supports the DMA function.

3.16.2. General-purpose timers

3.16.2.1. TIM2/TIM3

The general-purpose timers TIM2/TIM3 are consist of 32/16-bit auto-reload counters and a 32/16-bit prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.

They can work with the TIM1 by the Timer Link.

TIM2/TIM3 supports DMA function.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

The counter can be frozen in debug mode.

3.16.2.2. TIM14

The general-purpose timer (TIM14) is consist of a 16-bit auto-reload counter driven by a programmable prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

The counter can be frozen in debug mode.

3.16.2.3. TIM15/TIM16/TIM17

The general-purpose timer (TIM15, TIM16 and TIM17) is consist of a 16-bit auto-reload counter driven by a programmable prescaler.

TIM15/TIM16/TIM17 features one single channel for input capture/output compare, PWM or one-pulse mode output..

TIM15/TIM16/TIM17 have complementary outputs with dead time.

TIM15/TIM16/TIM17 supports DMA function.

The counter can be frozen in debug mode.

3.16.3. Basic timers (TIM6/TIM7)

The basic timer (TIM6/TIM7) is consist of a 16-bit auto-reload upcounter driven by their programmable prescaler respectively.

Synchronization circuit to trigger DAC.

Generate interrupt/DMA request on update event (counter overflow).

3.16.4. Low power timer (LPTIM)

LPTIM is a 16 -bit upcounter with a 3-bit prescaler and only support a single count.

LPTIM can be configured as a stop mode wake-up source.

The counter can be frozen in debug mode.

3.16.5. Independent watchdog (IWDG)

Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.

IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.

Controlling of option byte can enable IWDG hardware mode.

IWDG is the wake-up source of stop mode, which wakes up stop mode by reset.

The counter can be frozen in debug mode.

3.16.6. System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

3.16.7. SysTick timer

SysTick timer is dedicated to real-time operating systems, but could also be used as a standard downcounter.

SysTick Features:

- 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

3.17. Real-time clock (RTC)

The real-time clock is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

RTC is a 32-bit programmable counter with a prescale factor of up to 2^{20} bits.

The RTC counter clock source can be LSE/LSI and the stop wake-up source.

RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).

RTC supports clock calibration.

RTC can be frozen in debug mode.

3.18. Inter-integrated circuit interface (I2C)

I2C (inter-integrated circuit) bus interface connects the microcontroller and the serial I2C bus. It provides multi-master capability and controls all I2C bus specific sequences, protocols, arbitration and timing. Standard mode (Sm) and fast mode (Fm) are supported.

I2C Features:

- Two I2C Interface, support slave and master mode
- Multi-host function : can be master or slave
- Support different communication speeds
  - Standard Mode (Sm): Up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz
- As master
  - Generate Clock
  - Generation of Start and Stop
- As slave
  - Programmable I2C address detection
  - Discovery of the Stop bit
- 7-bit/10-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I2C busy flag bit
- Error flag
  - Master a rbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Single-byte buffer with DMA capability
- Software reset
- Analog noise filter function
- Support SMBus

3.19. Universal synchronous/asynchronous receiver transmitter (USART)

PY32F072 contains 4 USARTs, supports ISO7816, LIN, IrDA.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the

industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baudrate generator to provide a wide range of baudrate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baudrate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USARTs features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baudrate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baudrate detection
- Programmable data length of 8 or 9 bits
- Configurable stop bits (1 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Detection flag
  - Receive full buffer
  - Send empty buffer
  - End of transmission
- Parity control
  - Send check digit
  - Check the received data
- Flagged interrupt sources
  - CTS change
  - Send empty register
  - Send completed
  - Receive full data register
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Error detection
- Multiprocessor communication

  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

3.20. Serial peripheral interface (SPI)

PY32F072 contains two SPIs. SPIs allow the chip to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in master mode and provides the communication clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- 8 master mode baud rate prescale factors (max fPCLK/4)
- Slave mode frequency (max fPCLK/4)
- Both master and slave modes can be managed by software or hardware NSS: dynamic change of master/slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Interrupt-causing master mode faults, overloads
- Two 32-bit Rx and Tx FIFOs with DMA capability

3.21. USB2.0 full-speed module

PY32F072 contains one USB 2.0 full-speed module.

- Compliant with the technical specifications of USB2.0 full-speed devices
- Configurable from 1 to 8 USB endpoints
- Cyclic Redundancy Check (CRC) generation/checking, non- eturn-to-zero reverse (NRZI) encoding/decoding and bit stuffing
- Support isochronous transmission
- supporting bulk/isochronous endpoints
- Supports USB suspend/resume operations
- Frame lock clock pulse generation

3.22. CAN

PY32F072 contains one CAN communication interface module.

- Fully supports the CAN2.0A/CAN2.0B and CAN FD protocols specified by ISO11898-1.
- CAN2.0 supports the highest communication baudrate of 1 Mbit/s
- Support 1 to 1/256 baudrate prescaler, flexible baudrate configuration.
- Eight receive buffers
- One high priority main transmit buffer PTB
- Three sub transmit buffers STB
- 16 independent filters
- Support silent mode
- Support loopback mode
- Supports capturing the error type of transmission and locating the location of arbitration failure
- Programmable error warning value
- Support ISO11898-4 specified time trigger CAN and receive timestamp

3.23. Serial wire debug (SWD)

The ARM SWD interface allows serial debugging tools to be connected to the PY32F072.

4. Pin configuration

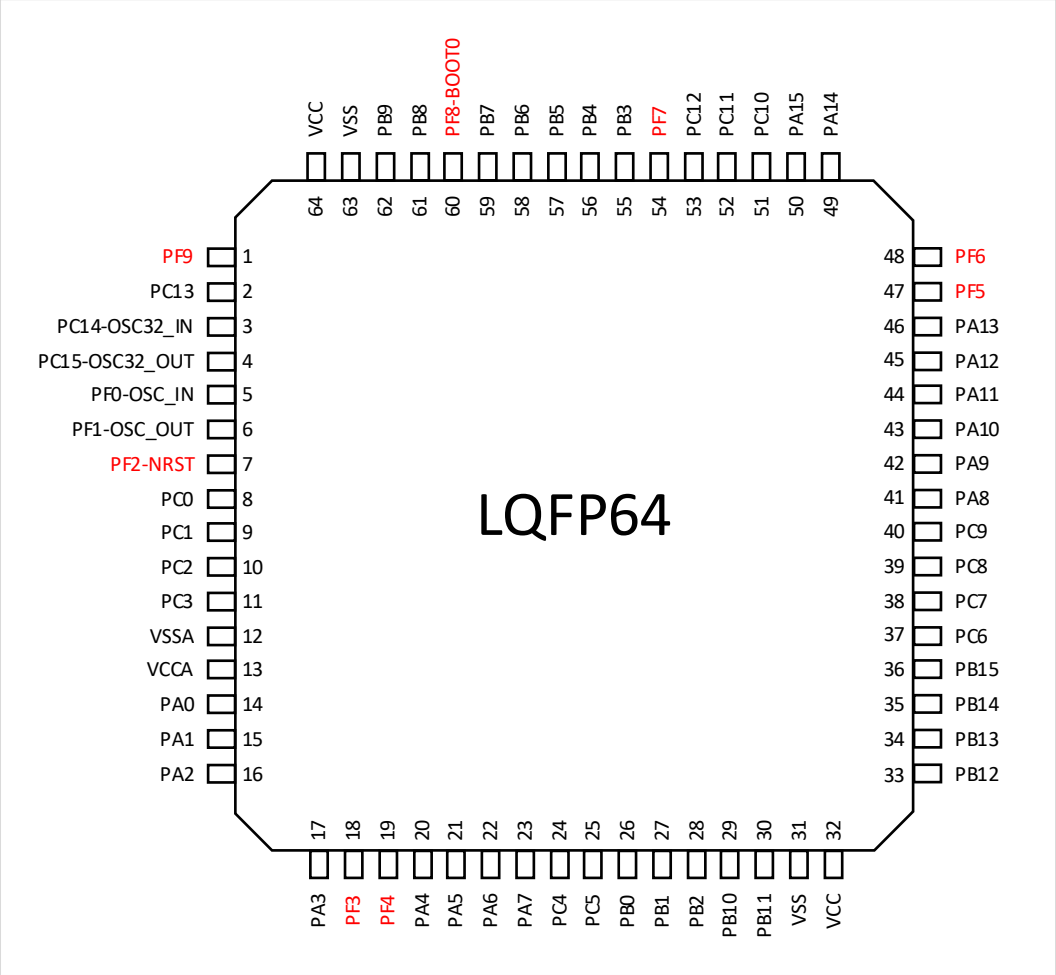


Figure 4-1LQFP64

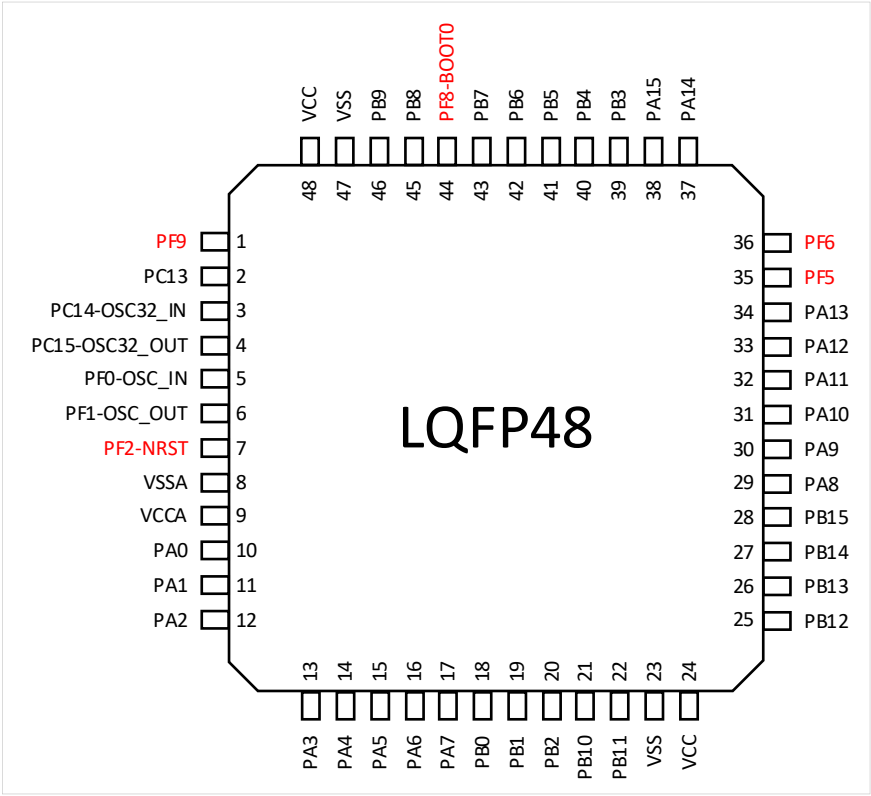


Figure 4-2LQFP48

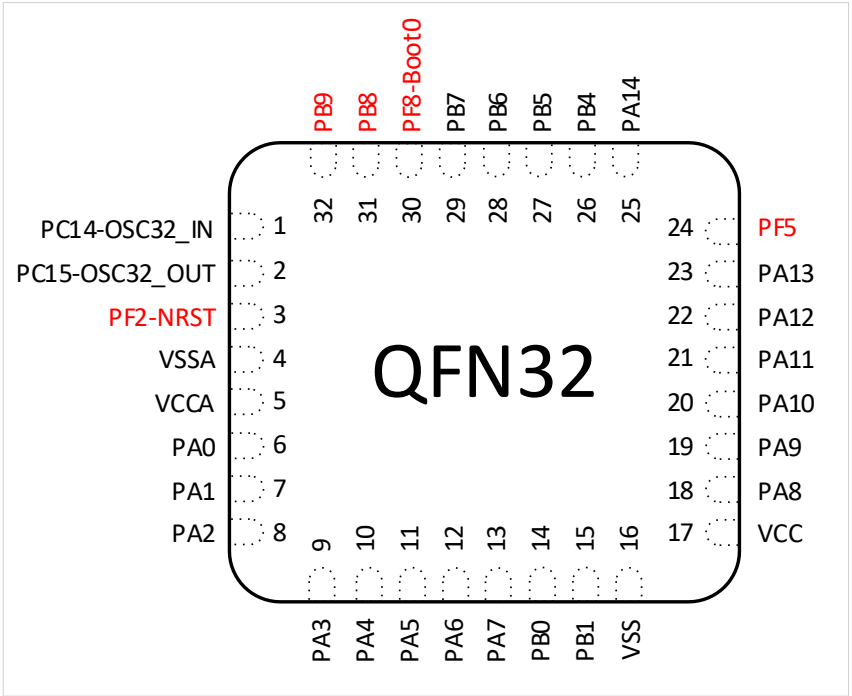


Figure 4-3 QFN32

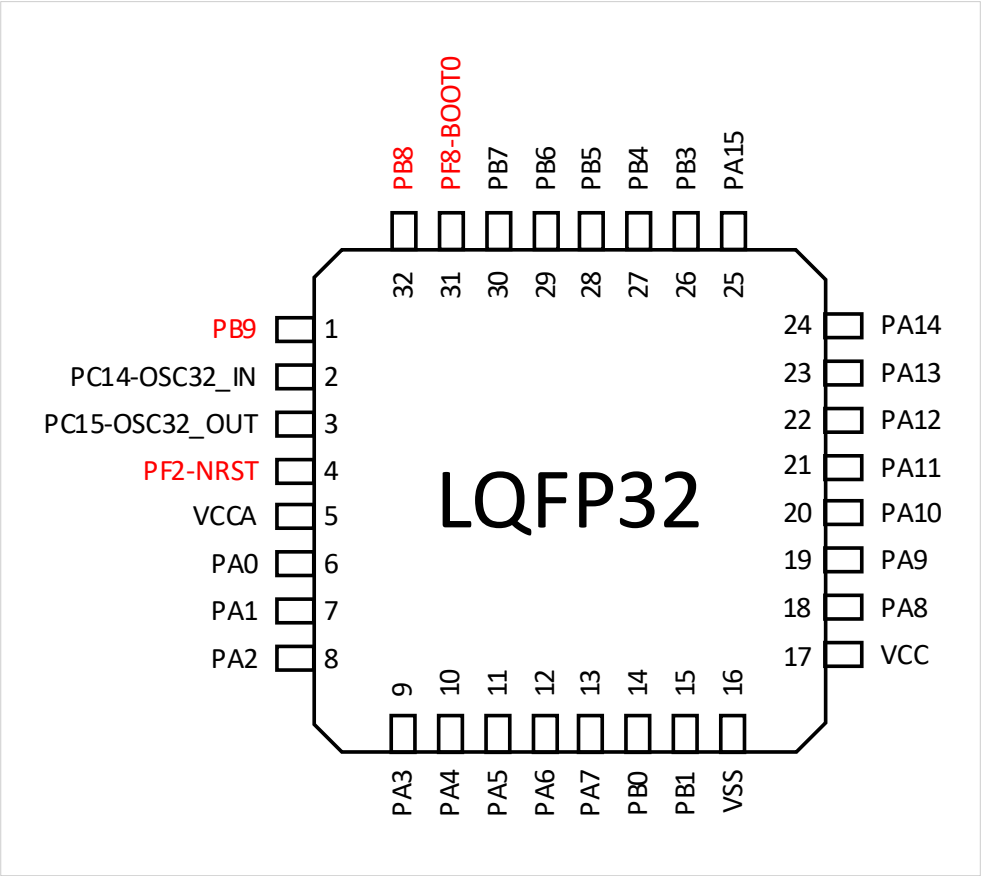


Figure 4-4 LQFP32

Table 4-1 Pin Definition Terminology and Symbols

Name		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I	Input-only pin
		I/O	Input/output pin
I/O structure		COM	Normal 5V I/O with analog input and output function
		RST	Reset pin, with internal weak pull-up resistor, without analog input and output function
		COM F	I/O, I2C Fm+ capable with analog input and output function
		COM U	GPIO 5V tolerant with USB PHY function
Notes			Unless otherwise specified, all ports are used as floating inputs between and after reset
Pin function	Alternate functions		Function selected by GPIOx_AFR register
	Additional functions		Directly selected or enabled through peripheral registers

Table 4-2LQFP64/LQFP48/QFN32/LQFP32 pin definition

Pin type				Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	QFN32	LQFP32					Alternate functions	Additional functions
	1			PF9	I/O	COM			
	2			PC13	I/O	COM			RTC_OUT
3	3	1	2	PC14	I/O	COM			OSC32_IN
4	4	2	3	PC15	I/O	COM			OSC32_OUT
5	5			PF0-OSC_IN	I/O	COM			OSC_IN
6	6			PF1-OSC_OUT	I/O	COM			OSC_OUT
7	7	3	4	PF2-NRST	I/O	RST			
8				PC0	I/O	COM			ADC_IN10, COMP1_INP0, COMP2_INN0 SEG27
9				PC1	I/O	COM			ADC_IN11, COMP1_INP1, COMP2_INN1 SEG26
10				PC2	I/O	COM			ADC_IN12, COMP1_INP2, COMP2_INN2 SEG25
11				PC3	I/O	COM			ADC_IN13, COMP1_INP3, COMP2_INN3

									SEG24
12	8	4		VSSA	I/O			Ground	
13	9	5	5	VCCA	I/O			Digital power supply	
14	10	6	6	PA0	I/O	COM			ADC_IN0, COMP1_INP4, COMP1_INN0, COMP2_INP0, COMP2_INN4 SEG23
15	11	7	7	PA1	I/O	COM			ADC_IN1, COMP1_INP5, COMP1_INN1, COMP2_INP1, COMP2_INN5 SEG22
16	12	8	8	PA2	I/O				ADC_IN2, COMP1_INP6, COMP1_INN2, COMP2_INP2 SEG21
17	13	9	9	PA3	I/O				ADC_IN3, COMP1_INP7, COMP1_INN3, COMP2_INP3 SEG20
18				PF3	I/O				SEG21
19				PF4	I/O				SEG22
20	14	10	10	PA4	I/O	COM_F			ADC_IN4, DAC_OUT1, COMP1_INP8, COMP1_INN4, COMP2_INP4 SEG19
21	15	11	11	PA5	I/O	COM_F			ADC_IN5,

									DAC_OUT2, COMP1_INP9, COMP1_INN5, COMP2_INP5, COMP3_INP0, COMP3_INN0 SEG18
22	16	12	12	PA6	I/O	COM_F			ADC_IN6, COMP1_INP10, COMP1_INN6 SEG17
23	17	13	13	PA7	I/O	COM			ADC_IN7, COMP1_INP11, COMP1_INN7 SEG16
24				PC4	I/O	COM			ADC_IN14, COMP1_INN8 SEG15
25				PC5	I/O	COM			ADC_IN15, COMP1_INN9 SEG14
26	18	14	14	PB0	I/O	COM			ADC_IN8, COMP2_INN6, SEG13
27	19	15	15	PB1	I/O	COM			ADC_IN9, COMP2_INP6, COMP2_INN7, COMP3_INP1, COMP3_INN1 SEG12
28	20			PB2	I/O	COM			ADC_IN10, COMP2_INP7, COMP2_INN8 OPA3_INN SEG11
29	21			PB10	I/O	COM_F			ADC_IN11,

									COMP2_INP8 OPA3_INP SEG10
30	22			PB11	I/O	COM_F			ADC_IN15, COMP3_INP8, COMP3_INN4 OPA3_OUT SEG9
31	23	16	16	VSS	I/O			Ground	
32	24	17	17	VCC	I/O			Digital power supply	
33	25			PB12	S				COMP2_INP9 OPA2_INN SEG8
34	26			PB13	S				COMP1_INP10 OPA2_INP SEG7
35	27			PB14					COMP2_INP11, COMP3_INP9, COMP3_INN5 OPA2_OUT SEG6
36	28			PB15					OPA1_INN SEG5
37				PC6					OPA1_INP SEG4
38				PC7					COMP3_INP13, COMP3_INN8 OPA1_OUT SEG3
39				PC8					SEG2
40				PC9					SEG1
41	29	18	18	PA8					SEG0

42	30	19	19	PA9					COM0
43	31	20	20	PA10					COM1
44	32	21	21	PA11		COM_U			USB_DM COM2
45	33	22	22	PA12		COM_U			USB_DP COM3
46	34	23	23	PA13					
47	35	24		PF5					
48	36			PF6					
49	37	25	24	PA14					
50	38		25	PA15					
51				PC10					COM4/SEG39
52				PC11					COM5/SEG38
53				PC12					COM6/SEG37
54				PF7					COM7/SEG36
55	39		26	PB3					COMP2_INN9 SEG35/VLCDH
56	40	26	27	PB4					COMP1_INP12 OPA3_OUT SEG34/VLCD3
57	41	27	28	PB5					COMP1_INP13 SEG33/VLCD2
58	42	28	29	PB6					COMP1_INP14, COMP2_INP14 SEG32/VLCD1
59	43	29	30	PB7					PVD_IN, COMP2_INP15

									SEG31
60	44	30	31	PF8/BOOT					SEG30
61	45	31	32	PB8					SEG29
62	46	32	1	PB9					SEG28
63	47			VSS				Ground	
64	48			VCC				Digital power supply	

(1) Configure by option bytes to choose PF2 or NRST is

(2) After reset, PA13 and PA14 are configured as SWDIO and SWCLK AF functions, the former has an internal pull-up resistor and the latter has an internal pull-down resistor activated.

(3) BOOT0 defaults to digital input mode and pull-down is enabled.

4.1. PortA alternate function mapping

Table 4-3 PortA alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART2_CTS	TIM2_CH1_ETR		USART4_TX			COMP1_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI2_SCK						SEG23	
PA1	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	EVENTOUT	USART2_RTS	TIM2_CH2		USART4_RX	TIM15_CH1N	I2C1_SMBA	
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI1_SCK/I2S1_CK	SPI2_MOSI					SEG22	
PA2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM15_CH1	USART2_TX	TIM2_CH3					COM2_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI1_MOSI/I2S1_SD	SPI2_MISO					SEG21	
PA3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM15_CH2	USART2_RX	TIM2_CH4					EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI2_MSIO	SPI2_CS					SEG20	
PA4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_NSS/I2S1_WS	USART2_CK			TIM14_CH1			EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI2_MOSI	USART2_TXD			PVD_OUT		SEG19	
PA5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK/I2S1_CK		TIM2_CH1_ETR					EVENTOUT

	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
			USART3_TX				SEG18	
PA6	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN		USART3_CTS	TIM16_CH1	EVENTOUT	COMP1_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
							SEG17	
PA7	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM1_CH1N		TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
							SEG16	
PA8	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CTC_SYNC			
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SPI2_NSS						SEG0	
PA9	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	TIM15_BKIN	USART1_TX	TIM1_CH2				I2C1_SCL	EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SPI2_MISO	MCO					COM0	
PA10	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	TIM17_BKIN	USART1_RX	TIM1_CH3				I2C1_SDA	EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SPI2_MOSI						COM1	
PA11	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	EVENTOUT	USART1_CTS	TIM1_CH4		CAN_RX		I2C2_SCL	COMP1_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SPI2_MOSI/I2S1_MCK			TIM1_BKIN2			COM2	
PA12	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	EVENTOUT	USART1_RTS	TIM1_ETR		CAN_TX		I2C2_SDA	COMP2_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SPI1_MOSI/I2S1_SD	I2S1_CKIN					COM3	
PA13	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SWDIO	IROUT						EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		USART1_RXD		COMP3_OUT	PVD_OUT			
PA14	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SWCLK	USART2_TX						EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		USART1_TXD			PVD_OUT			
PA15	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_NSS/I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	USART4_RTS			EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
			USART3_RTS_DE_CK					

4.2. PortB alternate function mapping

Table 4-4 Port B alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N		USART3_CK			COMP1_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SPI1_NSS/I2S1_WS		USART3_RX				SEG13	
PB1	AF0	AF1						
	TIM14_CH1	TIM3_CH4	TIM1_CH3N		USART3_RTS			EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
				COMP3_OUT			SEG12	
PB2	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
								EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SPI2_MISO		USART3_TX				SEG11	
PB3	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB4	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB5	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB6	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB7	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB8	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB9	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB10	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		I2C2_SCL	TIM2_CH3		USART3_TX	SPI2_SCK/I2S2_CK		COMP1_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15

		USART2_RTS					SEG10	
PB11	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	EVENTOUT	I2C2_SDA	TIM2_CH4		USART3_RX			COMP2_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI2_MOSI	USART2_CTS					SEG9	
PB12	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_NSS/I2S2_WS	EVENTOUT	TIM1_BKIN		USART3_CK	TIM15_BKIN		
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	I2C2_SMBA						SEG8	
PB13	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_SCK/I2S2_CK		TIM1_CH1N		USART3_CTS	I2C2_SCL		EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
		MCO		TIM15_CH1N			SEG7	
PB14	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_MISO/I2S2_MCK	TIM15_CH1	TIM1_CH2N		USART3_RTS	I2C2_SDA		EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
				TIM15_CH1			SEG6	
PB15	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_MOSI/I2S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N				EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
							SEG5	

4.3. PortC alternate function mapping

Table 4-5 PortC alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT							
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI1_MISO/I2S1_MCK	USART2_CTS	USART3_RTS				SEG27	
PC1	**AF0**	**AF1**						
	EVENTOUT							
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI1_MOSI/I2S1_SD	USART2_RTS	USART3_CTS	TIM15_CH1			SEG26	
PC2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	EVENTOUT	SPI2_MISO/I2S2_MCK						
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
		USART3_TXD	USART3_RXD	TIM15_CH2			SEG25	
PC3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	EVENTOUT	SPI2_MOSI/I2S2_SD						
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
		USART3_RXD	USART3_TXD				SEG24	
PC4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**

	EVENTOUT	USART3_TX						COMP3_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI1_NSS/I2S1_WS	USART1_TX		TIM2_CH1_ETR	IR_OUT		SEG14	
PC5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
		SUART3_RX						
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI1_MOSI/I2S1_SD	USART1_RX		TIM2_CH2			SEG14	
PC6	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM3_CH1							
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPi2_SCK/I2S2_CK		USART4_RXD	TIM2_CH3			SEG4	
PC7	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM3_CH2							
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI2_MISO/I2S2_MCK		SUART4_TXD	TIM2_CH4			SEG3	
PC8	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM3_CH3							
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI2_MOSI/I2S2_SD		USART4_CTS	TIM1_CH1			SEG2	
PC9	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM3_CH4							
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	SPI2_NSS/I2S2_WS	I2S1_CKIN	USART4_RTS	TIM1_CH2			SEG1	
PC10	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART4_TX	USART3_TX						
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
				TIM1_CH3			COM4/SEG39	
PC11	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART4_RX	USART3_RX						
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
				TIM1_CH4			COM5/SEG38	
PC12	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART4_CK	USART3_CK						
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
				TIM14_CH1			COM6/SEG37	
PC13	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
PC14	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
				TIM1_BKIN2				

PC15	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
				TIM15_BKIN				

4.4. PortF alternate function mapping

Table 4-7 PortF alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	CTC_SYNC							
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
				TIM14_CH1				
PF1	**AF0**	**AF1**						
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
				TIM15_CH1N				
PF2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	EVENTOUT							
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	MCO							
PF3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	EVENTOUT							
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
							SEG21	
PF4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
							SEG20	
PF5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
PF6	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM3_ETR	USART3_RTS						
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
				TIM1_CH1N			COM7/SEG36	
PF7	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
PF8	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
							SEG30	
PF9	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**

	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15

5. Memory map

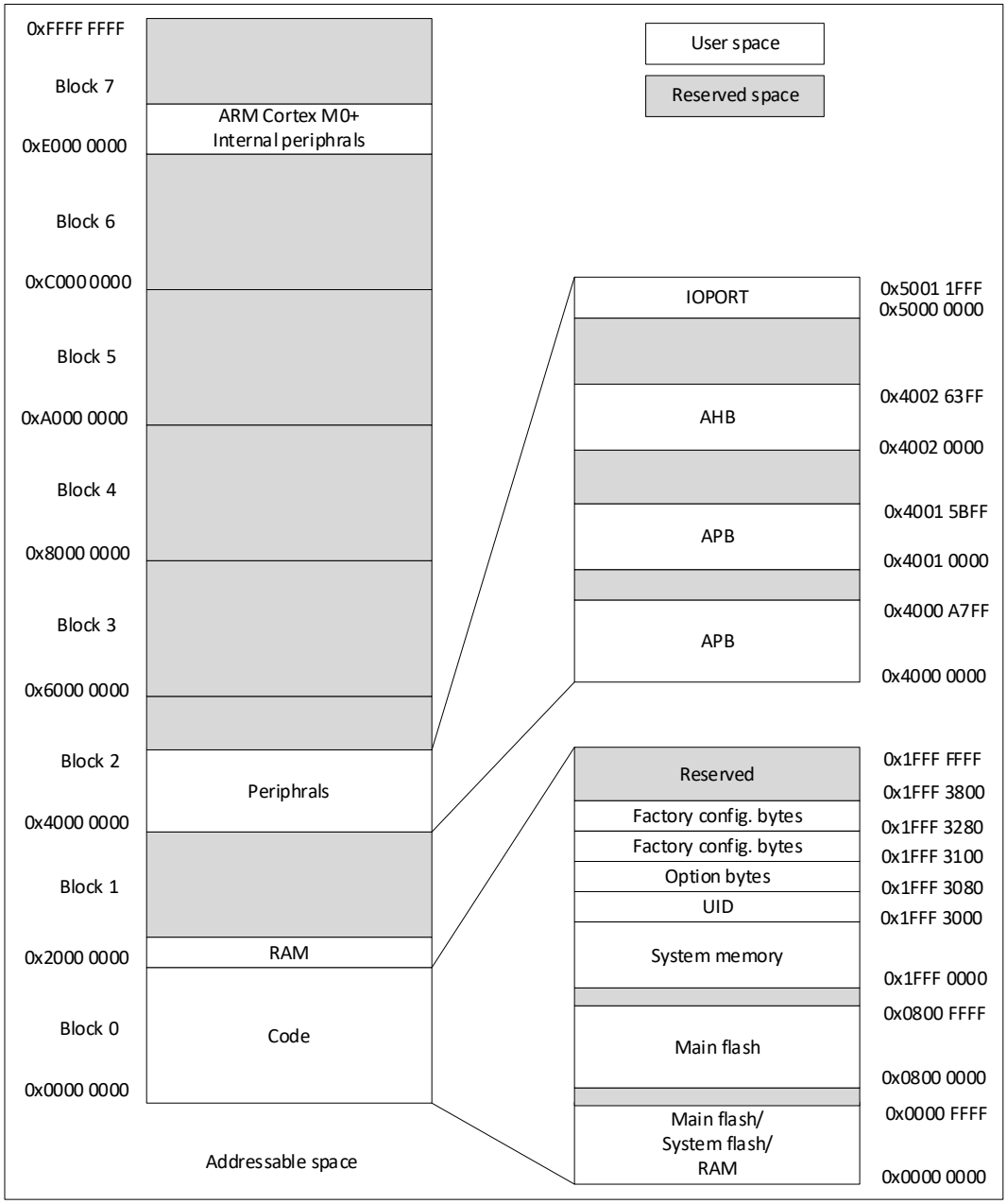


Figure 5-1 Memory map

Table 5-1 Memory boundary address

Type	Boundary Address	Size	Memory Area	Description
SRAM	0x2000 2000-0x3FFF FFFF	~512 Mbytes	Reserved	
	0x2000 0000-0x2000 3FFF	16 kbytes	SRAM	If the hardware is powered on to configure the SRAM to be 8kBytes, Then the SRAM address space is 0x2000 000-0x2000 1FFF
Information Block	0x1FFF 34 00-0x1FFF FFFF	4 kbytes	Reserved	
	0x1FFF 3380-0x1FFF 33FF	256 bytes	Factory config	High-Tempr TS Data
	0x1FFF 3300-0x1FFF 337F	256 bytes	Factory config	All trim data, NML-Tempr TS data
	0x1FFF 3280-0x1FFF 32FF	256 bytes	Factory config	Flash erasing time configuration parameters, CP pass ID
	0x1FFF 3200-0x1FFF 327F	256 bytes	Factory config	HIS Re-Trim data
	0x1FFF 3180-0x1FFF 31FF	256 bytes	Factory config	Flash/SRAM size configure, IP enable
	0x1FFF 3100-0x1FFF 317F	256 bytes	Factory config	GPIO infor, FT infor, pass ID
	0x1FFF 3080-0x1FFF 30FF	256 bytes	Option bytes	Chip software and hardware option bytes information
	0x1FFF 3000-0x1FFF 307F	256 bytes	UID bytes	Unique ID
	0x1FFF 0000-0x1FFF 2 FFF	12 kbytes	System memory	Store the boot loader
-	0x0801 0000-0x1FFF FFFF	~384 Mbytes	Reserved	
Main Block	0x0800 0000-0x0801 FFFF	128 kbytes	Main flash memory	
-	0x0001 0000-0x07FF FFFF	~8 Mbytes	Reserved	

-	0x0000 0000-0x0001 FFFF	128 kbytes	Choose according to the Boot configuration: 1) Main flash memory 2) System memory 3) SRAM	

(1) Except the above address, other is marked as reserved , which cannot be written , read as 0 , and a response error is generated .

Table 5-2 Peripheral register boundary address

Bus	Boundary Address	Size	PY*F072
	0xE000 000-0xE00F FFFF	1Mbytes	M0+
IOPORT	0x5000 1800 - 0x5FFF FFFF	~256 MB	Reserved
	0x5000 1400 - 0x5000 17FF	1 KB	GPIOF
	0x5000 1000 - 0x5000 13FF	1 KB	Reserved
	0x5000 0C00 - 0x5000 0FFF	1 KB	Reserved
	0x5000 0800 - 0x5000 0BFF	1 KB	GPIOC
	0x5000 0400 - 0x5000 07FF	1 KB	GPIOB
	0x5000 0000 - 0x5000 03FF	1 KB	GPIOA
AHB	0x4002 6400 - 0x4FFF FFFF	~256 MB	Reserved
	0x4002 3800 –0x4002 3BFF	1 KB	DIV
	0x4002 3400 - 0x4002 37FF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH
	0x4002 1C00 - 0x4002 1FFF	1 KB	Reserved
	0x4002 1800 - 0x4002 1BFF	1 KB	EXTI
	0x4002 1400 - 0x4002 17FF	1 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC 注 2
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
APB	0x4001 5C00 - 0x4001 FFFF	41 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBG
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved

	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0400 - 0x4001 23FF	8 KB	Reserved
	0x4001 0300 - 0x4001 03FF	1 KB	OPA
	0x4001 0200 - 0x4001 02FF		COMP
	0x4001 0000 - 0x4001 01FF		SYSCFG
	0x4000 8000- 0x4000 FFFF	32 KB	Reserved
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	Reserved
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR 注3
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6800 - 0x4000 6BFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	Reserved
	0x4000 6000 - 0x4000 63FF	1 KB	USB SRAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	Reserved
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC (include TAMP,BKP)
	0x4000 2400 - 0x4000 27FF	1 KB	LCD
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3

	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

(1) In the above table, the reserved address cannot be written, read back is 0, and a hardfault is generated

(2) Not only supports 32 bit word access, but also supports halfword and byte access.

(3) Not only supports 32 bit word access, but also supports halfword access.

6. Electrical Characteristics

6.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to VSS.

6.1.1. Minium and maximum values

Unless otherwise specified, the mimimum and maximum values are guaranteed in the worest condotions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A =25°C and T_A =$T_{A(max)}$ (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology charateristics are indicated in the table footnotes and are not tested in production. Based on charaterization, the minimum and maximum values refer to sample tests and represent the mean vaule plus or minus three times the standard deviation.

6.1.2. Typical values

Unless otherwise specified, typical data is based on T_A =25°C and VCC = 3.3V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by cgaracterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than equal to the value indicated.

6.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional opeartion of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6-1 Voltage characteristics (1)

Symbol	Ratings	Minimum value	Maximum value	Unit
VCC	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	VCC+0.3	V

（1） Power supply VCC and ground VSS pins must always be connected to the external power supply within the allowable range.

Table 6-2 Current characteristics

Symbol	Describe	Maximum value	Unit
I_{VCC}	Flowing into VCC pin (supply current)(1)	300	mA

I_{VSS}	Total current flowing out of VSS pin (outflow current)(1)	300	
$I_{IO(PIN)}$	Output sink current of COM IO(2)	20	
	Source current for all IOs	-20	

（1） Power supply VCC and ground VSS pins must always be connected to the external power supply within the allowable range.

（2） These I/O types refer to the terms and symbols defined by pins.

Table 6-3 Thermal characteristics

Symbol	Describe	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	℃
T_O	Range of working temperature	-40 to +85	℃

6.3. Operating conditions

6.3.1. General working conditions

Table 6-4 General working conditions

Symbol	Parameter	Condition	Minimum vaule	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK}	Internal APB Clock frequency	-	0	72	MHz
VCC	Standard operating voltage	-	1.7	5.5	V
VIN	I/O input voltage	-	-0.3	VCC+0.3	V
T_A	Ambient temperature	-	-40	85	℃
T_J	Junction temperature	-	-40	105	℃

6.3.2. Operating conditions at power-up / power-down

Table 6-5 Operating conditions at power-up / power-down

Symbol	Parameter	Condition	Minimum vaule	Maximum value	Unit
t_{VCC}	VCC rise time rate	-	0	∞	us/V
	VCC fall time rate	-	20	∞	

6.3.3. Embedded reset and LVD module features

Table 6-6 Embedded reset module features

Symbol	Parameter	Condition	Minimum vaule	Typical value	Maximum value	Unit
$t_{RSTTEMPO}$(1)	Reset time	-	-	4.0	7.5	ms
$V_{POR/PDR}$	POR/PDR reset threshold	Rising edge	1.50(2)	1.60	1.70	V
		Falling edge	1.45(1)	1.55	1.65(2)	V

V_{BOR1}	BOR threshold 1	Rising edge	1.70(2)	1.80	1.90	V
		Falling edge	1.60	1.70	1.80(2)	V
V_{BOR2}	BOR threshold 2	Rising edge	1.90(2)	2.00	2.10	V
		Falling edge	1.80	1.90	2.00(2)	V
V_{BOR3}	BOR threshold 3	Rising edge	2.10(2)	2.20	2.30	V
		Falling edge	2.00	2.10	2.20(2)	V
V_{BOR4}	BOR threshold 4	Rising edge	2.30(2)	2.40	2.50	V
		Falling edge	2.20	2.30	2.40(2)	V
V_{BOR5}	BOR threshold 5	Rising edge	2.50(2)	2.60	2.70	V
		Falling edge	2.40	2.50	2.60(2)	V
V_{BOR6}	BOR threshold 6	Rising edge	2.70(2)	2.80	2.90	V
		Falling edge	2.60	2.70	2.80(2)	V
V_{BOR7}	BOR threshold 7	Rising edge	2.90(2)	3.00	3.10	V
		Falling edge	2.80	2.90	3.00(2)	V
V_{BOR8}	BOR threshold 8	Rising edge	3.10(2)	3.20	3.30	V
		Falling edge	3.00	3.10	3.20(2)	V
V_{PVD0}	PVD threshold 0	Rising edge	1.70(2)	1.80	1.90	V
		Falling edge	1.60	1.70	1.80(2)	V
V_{PVD1}	PVD Threshold 1	Rising edge	1.90(2)	2.00	2.10	V
		Falling edge	1.80	1.90	2.00(2)	V
V_{PVD2}	PVD Threshold 2	Rising edge	2.10(2)	2.20	2.30	V
		Falling edge	2.00	2.10	2.20(2)	V
V_{PVD3}	PVD Threshold 3	Rising edge	2.30(2)	2.40	2.50	V
		Falling edge	2.20	2.30	2.40(2)	V
V_{PVD4}	PVD Threshold 4	Rising edge	2.50(2)	2.60	2.70	V
		Falling edge	2.40	2.50	2.60(2)	V
V_{PVD5}	PVD threshold 5	Rising edge	2.70(2)	2.80	2.90	V
		Falling edge	2.60	2.70	2.80(2)	V
V_{PVD6}	PVD threshold 6	Rising edge	2.90(2)	3.00	3.10	V
		Falling edge	2.80	2.90	3.00(2)	V
V_{PVD7}	PVD threshold 7	Rising edge	3.10(2)	3.20	3.30	V
		Falling edge	3.00	3.10	3.20(2)	V
$V_{POR\_PDR\_hyst}$(1)	POR / PDR hysteresis voltage	-		50		mV
$V_{PVD\_BOR\_hyst}$(1)	PVD hysteresis voltage			100		mV
$Idd_{(PVD)}$	PVD power consump-tion			0.6		uA
$Idd_{(BOR)}$	BOR power consump-tion			0.6		uA

（1） Guaranteed by design, not tested in production.

（2） Data is based on assessment results and is not tested in production.

6.3.4. Operating current characteristics

Table 6-7 Operating mode current

Symbol	Condition						Typical value(1)	Maximum value	Unit
	System clock	Frequency	Code	Run	Peripheral clock	FLASH sleep			
I_{DD}(run)	HSI	72 MHz	While(1)	Flash	ON	DISABLE			mA
					OFF	DISABLE			
		48 MHz			ON	DISABLE		-	
					OFF	DISABLE		-	
		24 MHz			ON	DISABLE		-	
					OFF	DISABLE		-	
		16 MHz			ON	DISABLE		-	
					OFF	DISABLE		-	
		8 MHz			ON	DISABLE		-	
					OFF	DISABLE		-	
		4 MHz			ON	DISABLE		-	
					OFF	DISABLE		-	
	LSI	32 kHz			ON	DISABLE		-	uA
					OFF	DISABLE		-	
	LSI	32.768 kHz			ON	ENABLE	25	-	uA
					OFF	ENABLE	24	-	

（1） Data is based on assessment results and is not tested in production.

Table 6-8Sleep mode current

Symbol	Condition				Typical value(1)	Maximum value	Unit
	System clock	Frequency	Peripheral clock	FLASH sleep			
I_{DD} (sleep)	HSI	72MHz	ON	DISABLE		-	mA
			OFF	DISABLE		-	mA
		48MHz	ON	DISABLE			
			OFF	DISABLE			
		24MHz	ON	DISABLE		-	mA
			OFF	DISABLE		-	mA
		16MHz	ON	DISABLE		-	mA
			OFF	DISABLE		-	mA
		8MHz	ON	DISABLE		-	mA
			OFF	DISABLE		-	mA
		4MHz	ON	DISABLE		-	mA
			OFF	DISABLE		-	mA
	LSI	32.768kHz	ON	DISABLE	170	-	uA
			OFF	DISABLE	170	-	uA
	LSI	32.768kHz	ON	ENABLE	95	-	uA
			OFF	ENABLE	96	-	uA

(1) Data is based on assessment results and is not tested in production.

Table 6-9Stop mode current

Symbol	Condition					Typical value(1)	Maximum value	unit
	VCC	VDD	MR/LPR	LSI	Peripheral clock			
I_{DD} (stop)	1.7 to 5.5V	1.2V	MR	-	-	30	-	uA
		1.2V	LPR	ON	RTC+IWDG+LPTIM	6	-	
					IWDG	6	-	
					LPTIM	6	-	
					RTC	6	-	
				OFF	No	6	-	
		1.0V		ON	RTC+IWDG+LPTIM	4.5	-	
					IWDG	4.5	-	
					LPTIM	4.5	-	
					RTC	4.5	-	
				OFF	No	3	-	

(1) Data is based on assessment results and is not tested in production.

6.3.5. Wake-up time for low power mode

Table 6-10 Low power mode wake-up time

Symbol	Parameters(1)		Condition		Typical value(2)	Maximum value	Unit
$T_{WUSLEEP}$	Wake-up from sleep mode		-		7		us
T_{WUSTOP}	Wake-up from stop mode	Powered by MR	Execute program in Flash, HSI (24 MHz) as system clock		3.5		us
		Powered by LPR	Execute program in Flash, HSI as system clock	VDD=1.2V	5		us
				VDD=1.0V	8		

（1） The wake-up time is measured from the wake-up time until the first instruction is read by the user program.

（2） Data is based on assessment results and is not tested in production.

6.3.6. External clock source characteristics

6.3.6.1. External high-speed clock

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the chip stops working, the corresponding I/O is used as a standard GPIO.

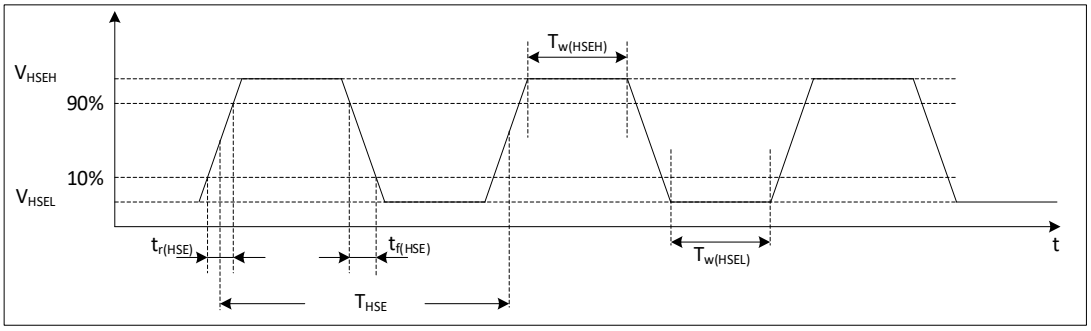


Figure 6-1 External high-speed clock timing diagram

Table 6-11 External high-speed clock features

Symbol	Parameters(1)	Minimum value	Typical value	Maximum value	Unit
f_{HSE_ext}	User external clock source frequency	0	8	32	MHz
V_{HSEH}	Input pin high level voltage	0.7VCC		VCC	V
V_{HSEL}	Input pin low level voltage	Vss		0.3VCC	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	Enter high or low time	15			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Enter the rise/fall time	-		20	ns

(1) Guaranteed by design, not tested in production.

6.3.6.2. External low-speed clock

In the bypass mode of LSE (the LSE BYP of RCC_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO.

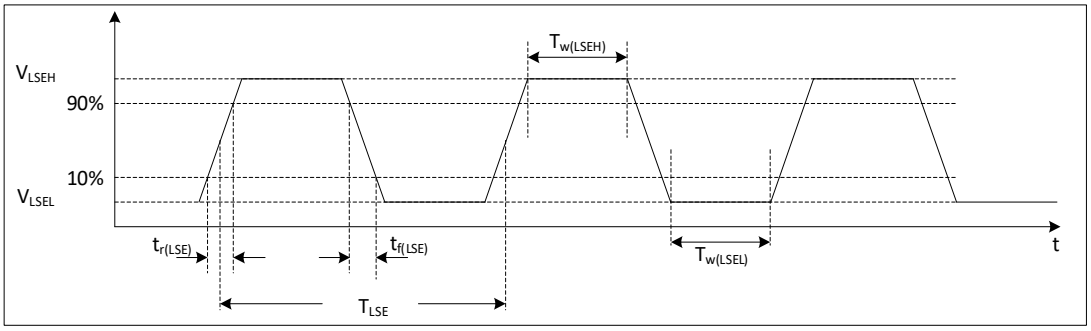


Figure 6-2 External low-speed clock timing diagram

Table 6-12 External low-speed clock characteristics

Symbol	Parameters(1)	Minimum value	Typical value	Maximum value	Unit
f_{LSE_ext}	User external clock frequency		32.768	1000	KHz
V_{LSEH}	Input pin high level voltage	0.7VCC			V
V_{LSEL}	Input pin low level voltage			0.3VCC	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	Enter high or low time	450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Enter the rise/fall time	-		50	ns

(1) Guaranteed by design, not tested in production .

6.3.6.3. External high-speed crystal

The high-speed external (HSE) clock can be supplied with a ~32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 6-13 External high-speed crystal characteristics

Symbol	Parameter	Condition(1)	Minimum value(2)	Typical value	Maximum value(2)	Unit
f_{OSC_IN}	Oscillation frequency	-	1		32	MHz
IDD(4)	HSE current consumption	During startup			5.5	mA
		VCC = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz		0.58		
		VCC = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz		0.59		
		VCC = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz		0.89		
		VCC = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz		1.14		
		VCC = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz		1.94		
$t_{SU(HSE)}$(3)(4)	Startup Time	f_{OSC_IN} = 32 MHz		2		ms
		f_{OSC_IN} = 4 MHz		2		ms

(1) Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.

(2) Guaranteed by design, not tested in production.

(3) $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state , measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another .

(4) Data is based on assessment results and is not tested in production.

6.3.6.4. External low speed crystal

The low-speed external (LSE) clock can be supplied with a 32.768 KHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 6-14 External low-speed crystal feature

Symbol	Parameter	Condition(1)	Minimum value(2)	Typical value	Maximum value(2)	Unit
IDD(4)	LSE current consumption	LSE_DRIVER [1:0] = 00		250		nA
		LSE_DRIVER [1:0] = 01		560		
		LSE_DRIVER [1:0] = 10		920		
		LSE_DRIVER[1:0] = 11		1260		
$t_{SU(LSE)}$(3)(4)	Startup Time			3		s

（1） Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.

（2） Guaranteed by design, not tested in production.

（3） $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable , measured for a standard crystal/resonator , which may vary greatly from crystal to resonator.

（4） Data is based on assessment results and is not tested in production.

6.3.7. Internal high frequency clock source HSI characteristics

Table 6-15 Internal high frequency clock source characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HSI}	HSI frequency		4.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
ΔTemp (HSI)	HSI frequency temperature drift	VCC = 1.7 to 5.5 V, TA = 25 C	-1(2)		1(2)	%
		VCC = 1.7 to 5.5 V, TA = 0 to 85 C	-2(2)		2(2)	%
		VCC = 1.7 to 5.5 V, TA = -40 to 85 C	-4(2)		2(2)	%
fTRIM (1)	HSI fine-tuning accuracy			0.1		%
$\Delta T_{emp(HSI)}$	HSI frequency temperature drift		45(1)		55(1)	%
tStab (HSI)	HSI stabilization time			2	4(1)	us
f_{TRIM}(1)	HSI fine-tuning accuracy	4 MHz		100		uA
		8 MHz		105		uA

		16 MHz		150		uA
		22.12 MHz, 24 MHz		180		uA

（1） Guaranteed by design, not tested in production.

（2） Data is based on assessment results and is not tested in production.

6.3.8. Internal low frequency clock source LSI characteristics

Table 6-17 Internal low frequency clock characteristics

Symbol	Parameter	Condition	Minimum vaule	Typical value	Maximum value	Unit
f_{LSI}	LSI frequency			32 kHz		
$\Delta T_{emp(LSI)}$	LSI frequency temperature drift	VCC = 3.3 V, T_A = 25 °C	-3		+3	%
		VCC = 1.6 to 5.5 V, T_A = 0 to 85 °C	-10(2)		10(2)	%
		VCC = 1.6 to 5.5 V, T_A = -40 to 85 °C	-20(2)		20(2)	%
f_{TRIM}(1)	LSI fine-tuning accuracy			0.2		%
$t_{Stab(LSI)}$(1)	LSI stabilization time			150		us
$I_{DD(LSI)}$(1)	LSI current consumption			210		nA

(1) Guaranteed by design, not tested in production.

(2) Data is based on assessment results and is not tested in production.

6.3.9. Phase locked loop (PLL) characteristics

Table 6-16 Phase locked loop characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{PLL_IN}	input frequency	T_A = 25 °C, VCC = 3.3 V	12(1)		24(1)	MHz
f_{PLL_OUT}	Output frequency	T_A = 25 °C, VCC = 3.3 V	24(1)		72	MHz
Jitter	Period jitter				0.3(1)	ns
t_{LOCK}	Latch time	f_{PLL_IN} = 24 MHz		15	40(1)	us

（1） Guaranteed by design, not tested in production.

6.3.10. Memory characteristics

Table 6-17 Memory characteristics

Symbol	Parameter	Condition	Typical value	Maximum value(1)	Unit
t_{prog}	Page program	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase	-	3.0	4.5	ms
I_{DD}	Page programe		2.1	2.9	mA
	Page/sector/mass erase		2.1	2.9	mA

(1) Guaranteed by design, not tested in production.

Table 6-18 Memory erase times and data retention

Symbol	Parameter	Condition	Minimum(1)	Unit
N_{END}	Erase and write times	T_A = -40 to 85 ℃	100	kcycle
t_{RET}	Data retention period	10 Kcycle T_A = 55 ℃	20	Year

(1) Data is based on assessment results and is not tested in production.

6.3.11. EFT characteristics

Symbol	Parameter	Condition	Grade	Typical value	Unit
EFT to IO		IEC61000-4-4	B	2	kV
EFT to Power		IEC61000-4-4	B	4	kV

6.3.12. ESD & LU characteristics

Table 6-19ESD & LU characteristics

Symbol	Parameter	Condition	Typical value	Unit
$V_{ESD(HBM)}$	Static discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	8	KV
$V_{ESD(CDM)}$	Static discharge voltage (charging equipment model)	ESDA/JEDEC JS-002-2018	1	KV
$V_{ESD(MM)}$	Static discharge voltage (machine model)	JESD22-A115C	200	V
LU	Static latch-up	JESD78E	200	mA

6.3.13. Port characteristics

Table 6-20IO static characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IH}	Input high level voltage	VCC = 1.7 to 5.5 V	0.7VCC			V
V_{IL}	Input low level voltage	VCC = 1.7 to 5.5 V			0.3VCC	V
V_{hys}(1)	Schmitt hysteresis voltage			200		mV
I_{lkg}	Input leakage current				1	uA
R_{PU}	Pull-up resistor		30	50	70	kΩ
R_{PD}	Pull-down resistor		30	50	70	kΩ
C_{IO}(1)	Pin capacitance			5		pF

(1) Guaranteed by design, not tested in production.

Table 6-21 Output voltage characteristics

Symbol	Parameters(1)	Condition	Minimum	Maximum	Unit
V_{OL}	COM IO output low level	I_{OL} = 8 mA, VCC ≥ 2.7 V	-	0.4	V
V_{OL}		I_{OL} = 4 mA, VCC = 1.8 V	-	0.5	V
V_{OL}(3)	Output low level voltage for an I/O pin	I_{OL} = 8 mA, VCC ≥ 2.7 V	-	0.4	V
V_{OL}(3)		I_{OL} = 4 mA, VCC = 1.8 V	-	0.4	V
V_{OH}	COM IO output high level	I_{OH} = 8 mA, VCC ≥ 2.7 V	VCC–0.4	-	V
V_{OH}		I_{OH} = 4 mA, VCC = 1.8 V	VCC–0.5	-	V
V_{OH}(3)	Output high level voltage for an I/O pin	I_{OL} = 8 mA, VCC ≥ 2.7 V	VCC–0.4		V
V_{OH}(3)		I_{OL} = 4 mA, VCC = 1.8 V	VCC–0.4		V

(1) IO types can refer to the terms and symbols defined by the pins.

(2) Data is based on assessment results and is not tested in production.

6.3.14. NRST pin characteristics

Table 6-22NRST pin characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IH}	Input high level voltage	VCC = 1.7 to 5.5 V	0.7VCC			V
VIL	Input low level voltage	VCC = 1.7 to 5.5 V			0.2VCC	V
V_{hys}(1)	Schmitt hysteresis voltage			300		mV
I_{lkg}	Input leakage current				1	uA
RPU(1)	Pull-up resistor		30	50	70	kΩ
RPD(1)	Pull-down resistor		30	50	70	kΩ
C_{IO} _	Pin capacitance			5		pF

(1) Guaranteed by design, not tested in production.

6.3.15. ADC characteristics

Table 6-23ADC characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
I_{DD}	Current consumption	@0.75MSPS		1.0		mA
C_{IN}(1)	Internal sample and hold capacitors			5		pF
F_{ADC}	Convert clock frequency	VCC = 1.7 to 2.3 V	1	4	8(2)	MHz
		VCC = 2.3 to 5.5 V	1	8	12(2)	MHz
T_{samp}(1)		VCC = 1.7 to 2.3 V	0.2			us
		VCC = 2.3 to 5.5 V	0.1			us
T_{conv}(1)				12*Tclk		
T_{eoc}(1)				0.5*Tclk		

DNL(2)	3-3.6V@RT				±1	LSB
INL(2)	3-3.6V@RT				±1.5	LSB
Offset(2)	3-3.6V@RT				±1.5	LSB
DNL	1.7~2.3V@RT				?	
DNL	2.3~5.5V@RT				?	

(1) Guaranteed by design, not tested in production.

(2) Data is based on assessment results and is not tested in production.

6.3.16. DAC features

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit	Comments
V_{DDA}	Analog supply voltage	1.7	-	5.5	V	-
$R_{LOAD(1)}$	Resistive load vs. VSSA with buffer ON	5	-	-	kΩ	
	Resistive load vs. VCCA with buffer ON	15	-	-	kΩ	
$R_{O(1)}$	Impedance output with buffer OFF	-	-	15	kΩ	The minimum resistive load between DAC_VOUT and VSS to have a 1% accuracy is 1.5 MΩ .
$C_{LOAD(1)}$	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	VDDA - 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V DDA – 10 mV	V	
$I_{DDA(1)}$	DAC DC current consumption in quiescent-mode (2)	-	-	600	μA	With no load, middle code (0x800) on the inputs
		-	-	700	μA	With no load, worst code (0xF1C) at VREF+ = 3.6 V in terms of DC consumption on the inputs
DNL(3)		-	-	±1	LSB	Given for the DAC in 10-bit configuration

	Differential linearity error	-	-	±3	LSB	Given for the DAC in 12-bit configuration
$INL_{(3)}$	Integral linearity error	-	-	±1	LSB	Given for the DAC in 10-bit configuration
				±4	LSB	Given for the DAC in 12-bit configuration
$Offset_{(3)}$	offset error	-	-	±3	LSB	Given for the DAC in 10-bit
		-	-	±12	LSB	Given for the DAC in 12-bit
Gain $error_{(3)}$	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING(3)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches finalvalue ±1LSB	-	3	4	µs	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the inputcode (from code i to i+1LSB)	-	-	1	MS/s	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ
$t_{WAKEUP(3)}$	Wakeup time from off state	-	6.5	10	µs	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ input code between lowest and highest possible ones.
$PSRR+_{(1)}$	Power supply rejection ratio (to V DDA) (static DC measurement	-	–67	–40	dB	No R_{LOAD} , C_{LOAD} = 50 pF

6.3.17. Comparator characteristics

Table 6-24 Comparator characteristics(1)

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
VIN	Input voltage range			0		VCC	V
VBG	Scale input voltage			VREFINT			V
VSC	Scaler offset voltage				±5	± 10	mV
IDD(SCALER)	Scaler static consumption				0.8	1	uA
tSTART_SCALER	Scaler startup time				100	200	us
tSTART	Startup time to reach propagation delay specification	High-speed mode				5	us
		Medium-speed mode				15	
tD	Propagation delay	200 mV step,	High-speed mode		40	70	ns

		100 mV overdrive	Medium-speed mode		0.9	2.3	us
		>200 mV step, 100 mV overdrive	High-speed mode			85	ns
			Medium-speed mode			3.4	us
Voffset	Offset error				±5		mV
Vhys	Hysteresis	No hysteresis			0		mV
		With hysteresis			20		
IDD	Consumption	Medium-speed mode, no de-glitcher	Static		5		uA
			With 50 KHz and ±100 mv overdrive square signal		6		uA
		Medium-speed mode, with de-glitcher	Static		7		uA
			With 50 KHz and ±100 mv overdrive square signal		8		uA
		High-speed mode, no de-glitcher	Static		250		uA
			With 50 KHz and ±100 mv overdrive square signal		250		uA

(1) Guaranteed by design, not tested in production.

6.3.18. Operational amplifier characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
Vi	Input voltage		0		AVCC	V
Vo	The output voltage		0.1		AVCC - 0.2	V
Io	Output current				2.2	mA
RL	load time		5K			Ω
Tstart	initialization time				20	us
Vio	Input offset voltage			±6		mV
PM	Phase margin			80		Deg
UGBW	unity gain width			10		MHz
SR	Slew rate			8		V/us

6.3.19. Temperature sensor characteristics

Table 6-25 Temperature sensor characteristics

Symbol	Parameter	Mini-mum value	Typical value	Maximum value	Unit
T_L(1)	VTS linearity with temperature		±1	±2	℃
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/℃
V_{30}	Voltage at 30 ℃ (±5 ℃)	0.742	0.76	0.785	V
t_{START}(1)	Start up time entering in continuous mode		70	120	us
t_{s_temp}(1)	ADC sampling time when reading the tempera-ture	9			us

(1) Guaranteed by design, not tested in production.

(2) Data is based on assessment results and is not tested in production.

6.3.20. Built-in reference voltage characteristics

Table 6-26 Built-in reference voltage characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
VREFINT	Internal reference voltage	1.17	1.2	1.23	V
$T_{start\_vrefint}$	Start time of internal reference voltage		10	15	us
T_{coeff}	Temperature coefficient			100(1)	ppm/°C
I_{vcc}	Current consumption from VCC		12	20	uA

(1) Guaranteed by design, not tested in production.

6.3.21. Built-in reference voltage

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REF25}	Internal 2.5V reference voltage	TA = 25°C, VCC = 3.3 V	2.465	2.5	2.525	V
V_{REF25}	Start time of internal reference voltage	TA = -40 to 85°C, VCC1 = 1.7 to 5.5 V	2.463	2.5	2.525	V(1)
				2.048		
V_{REF215}	Internal 2.5V reference voltage	TA = 25°C, VCC = 3.3V	1.485	1.5	1.515	V

V_{REF15}	Current consumption from VCC	TA = -40 to 85°C, VCC1 = 1.7 to 5.5 V	1.477	1.5	1.519	V(1)
T_{coeff}	Internal 2.5V/1.5V temperature coefficient	TA = -40 to -85°C			120	ppm/°C

6.3.22. Timer characteristics

Table 6-27 Timer characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution time	-	1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	20.833		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-		$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz		24	
R_{esTIM}	Timer resolution	TIM1/3/14/16/17		16	Bit
$t_{COUNTER}$	16-bit counter clock period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.020833	1365	us

Table 6-28LPTIM characteristics (clock selection LSI)

Prescaler	PRESC [2:0]	Minimum overflow value	Maximum overflow value	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table 6-29IWDG characteristics (clock selection LSI)

Prescaler	PR[2:0]	Minimum overflow value	Maximum overflow value	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 6-30 WWDG characteristics (Clock selection 4 8MHz PCLK)

Prescaler	WDGTB[1:0]	Minimum overflow value	Maximum overflow value	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	

4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

6.3.23. Communication port characteristics

6.3.23.1. I2C bus interface features

The I2C interface meets the timing requirements of the I2C-bus specification and user manual:

- Standard-mode (Sm): 100 kbit/s
- Fast-mode (Fm): 400 kbit/s

The I2C timings requirements is guaranteed by design, provided the I2C peripheral is properly configured and the I2C CLK frequency is greater than the minimum required in the table below.

Table 6-31 Minimum I2C CLK frequency

Symbol	Parameter	Condition	Minimum	Unit
$f_{I2CCLK(min)}$	Minimum I2CCLK frequency	Standard-mode	2	MHz
		Fast-mode	9	

I2C SDA and SCL pins have analogue filtering, see table below.

Table 6-32I2C filter characteristics

Symbol	Parameter	Minimum	Maximum	Unit
t_{AF}	Lmiting duration of spikes suppressed by the filter (spikers shorter than the limiting duration are suppressed)	50	260	ns

6.3.23.2. Serial peripheral interface (SPI) characteristics

Table 6-33SPI characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	12	MHz
		Slave mode	-	12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, fPCLK = 36 MHz, presc = 4	Tpclk*2 - 2	Tpclk*2 + 1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode, fPCLK = 48 MHz, presc = 4	Tpclk + 5(1)	-	ns
		Slave mode, fPCLK = 48 MHz, presc = 4	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	ns
$t_{h(SI)}$		Slave mode	Tpclk + 5	-	

$t_{a(SO)}$	Data output access time	Slave mode, presc = 4	0	3Tpclk	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	2Tpclk + 5	4Tpclk + 5	ns
$t_{v(SO)}$	Data output valid ime	Slave mode (after enable edge), presc = 4	0	1.5Tpclk(2)	ns
$t_{v(MO)}$	Data output valid ime	Master mode (after enable edge)	-	6	ns
$t_{h(SO)}$	Data output hold time	Slave mode, presc = 4	0(3)	-	ns
$t_{h(MO)}$		Master mode	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

(1) The Master generates a 1pclk receive control signal before the receive edge.

(2) Slave has a maximum of 1pclk based on the sending edge of SCK delay, considering IO delay, etc., define 1.5pclk.

(3) Between the receiving edge and the sending edge , the slave updates the data before the sending edge.

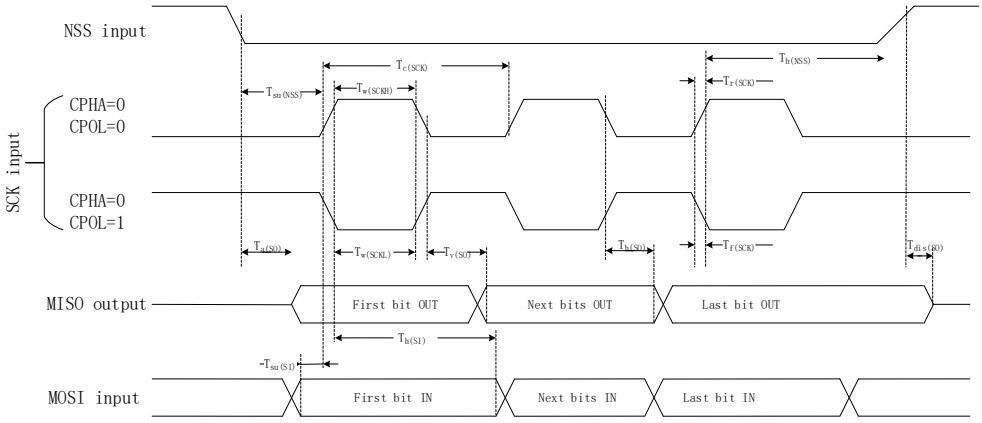


Figure 6-3SPI timing diagram – slave mode and CPHA=0

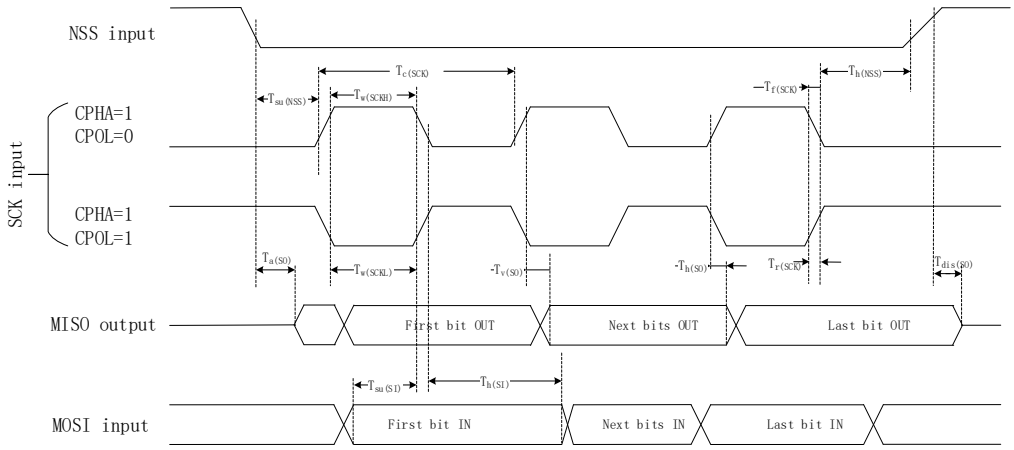


Figure 6-4SPI timing diagram – slave mode and CPHA=1

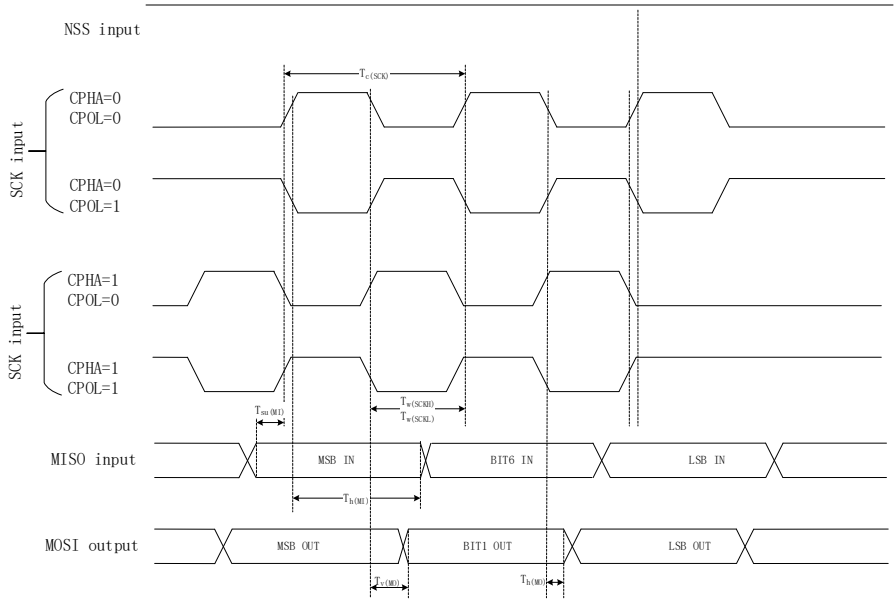
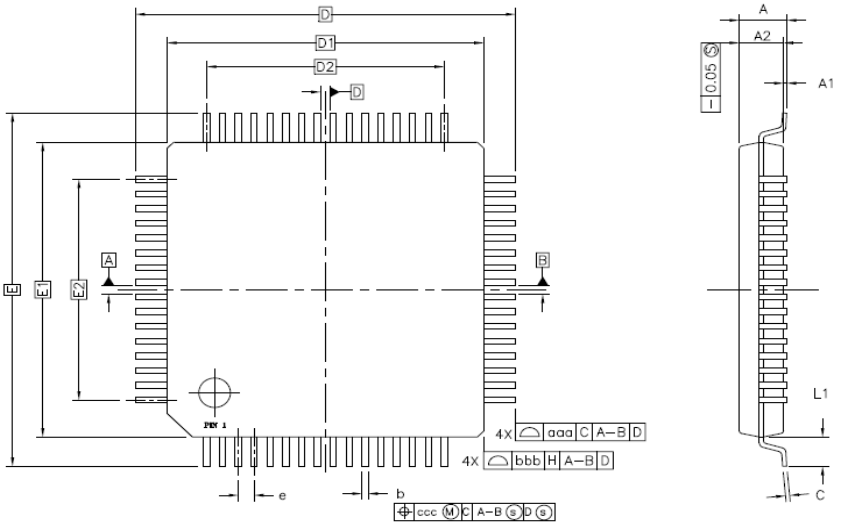
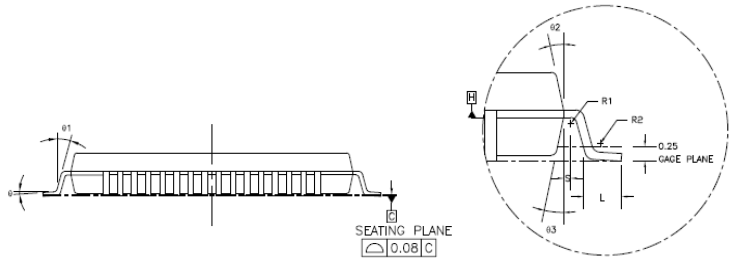


Figure 6-5SPI timing diagram – master mode

7. Package information

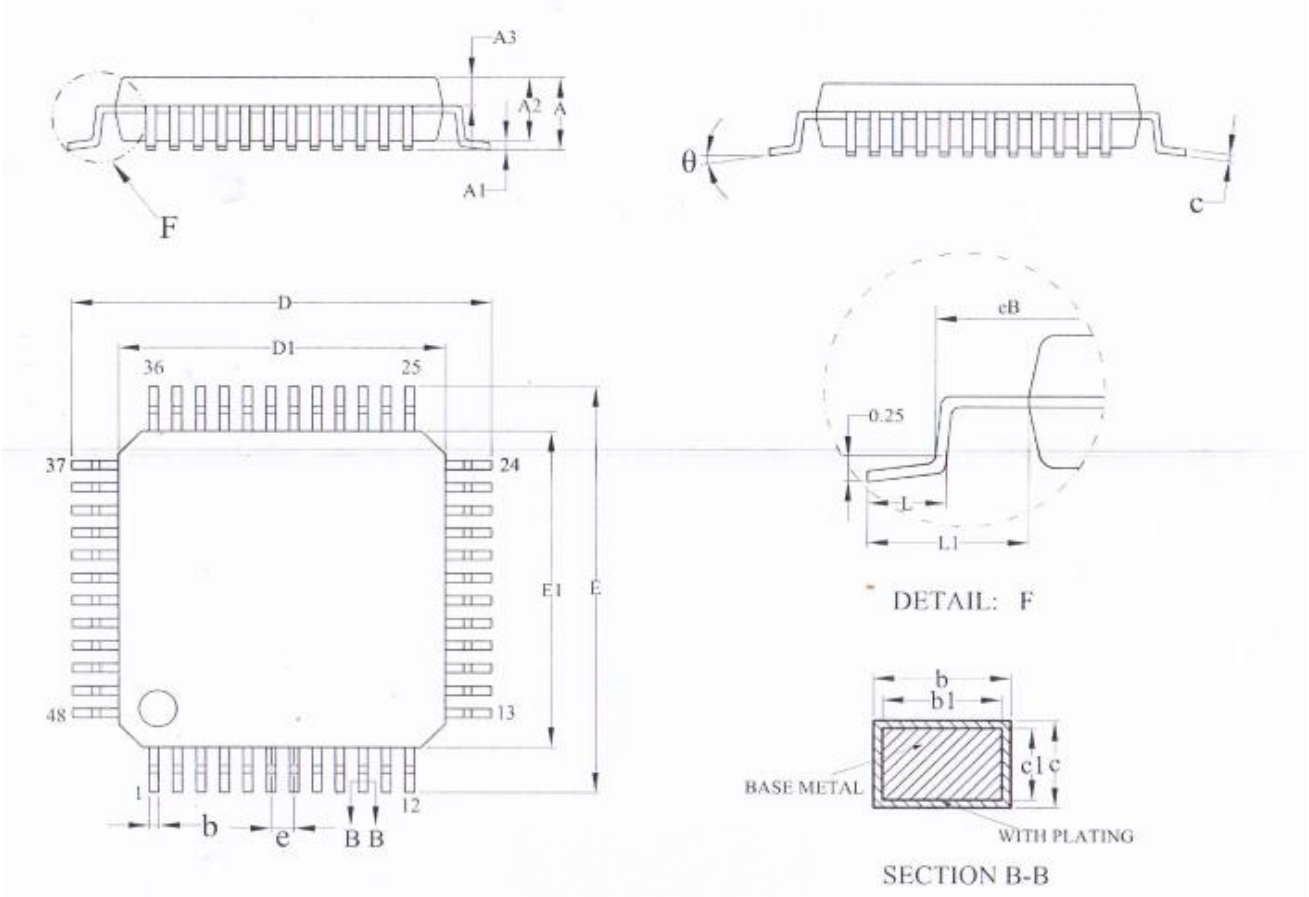
7.1. LQFP64 package size





Symbol	LQFP64		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	-	12.00	-
D1	-	10.00	-
E	-	12.00	-
E1	-	10.00	-
R1	0.08	-	-
R2	0.08	-	0.20
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	-	1.00	-
S	0.20	-	-
b	0.17	0.20	0.27
e	-	0.50	-
D2	-	7.50	-
E2	-	7.50	-
aaa	0.20		
bbb	0.20		
ccc	0.08		

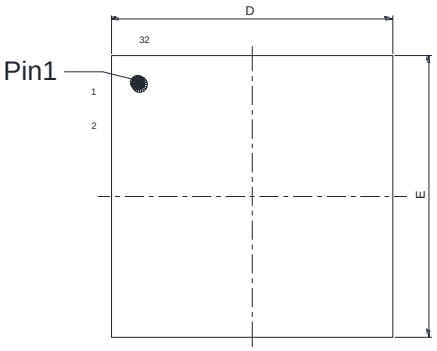
7.2. LQFP48 package size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7

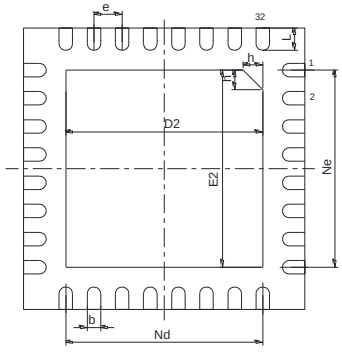
7.3. QFN32 package dimensions

TOP VIEW



SIDE VIEW

BOTTOM VIEW



BOTTOM VIEW

Common Dimensions

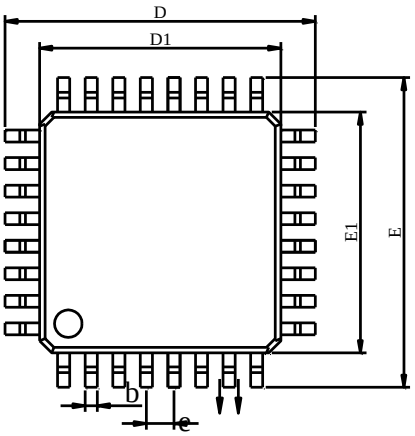
(Unit of Measure=millimeters)

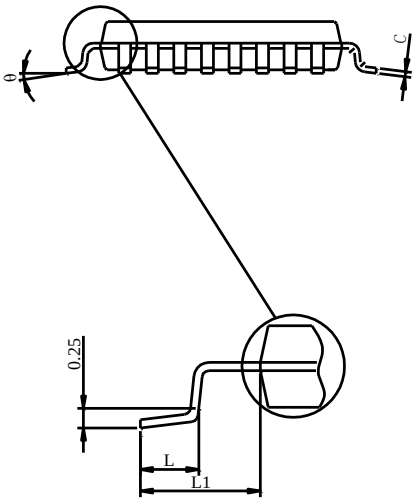
Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0	0.020	0.050
b	0.180	0.250	0.300
c	0.200REF		
D	4.900	5.000	5.100
D2	3.400	3.500	3.600
E	4.900	5.000	5.100
E1	3.400	3.500	3.600
e	0.500BSC		
Nd	3.500BSC		
L	0.350	0.400	0.450
h	0.300	0.350	0.400

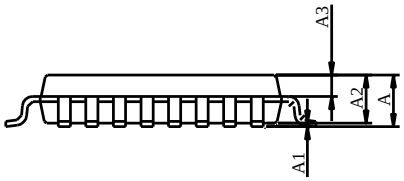
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	QFN32L(0505X0.75-0.5)	QFN-32	A

7.4. LQFP32 package dimensions







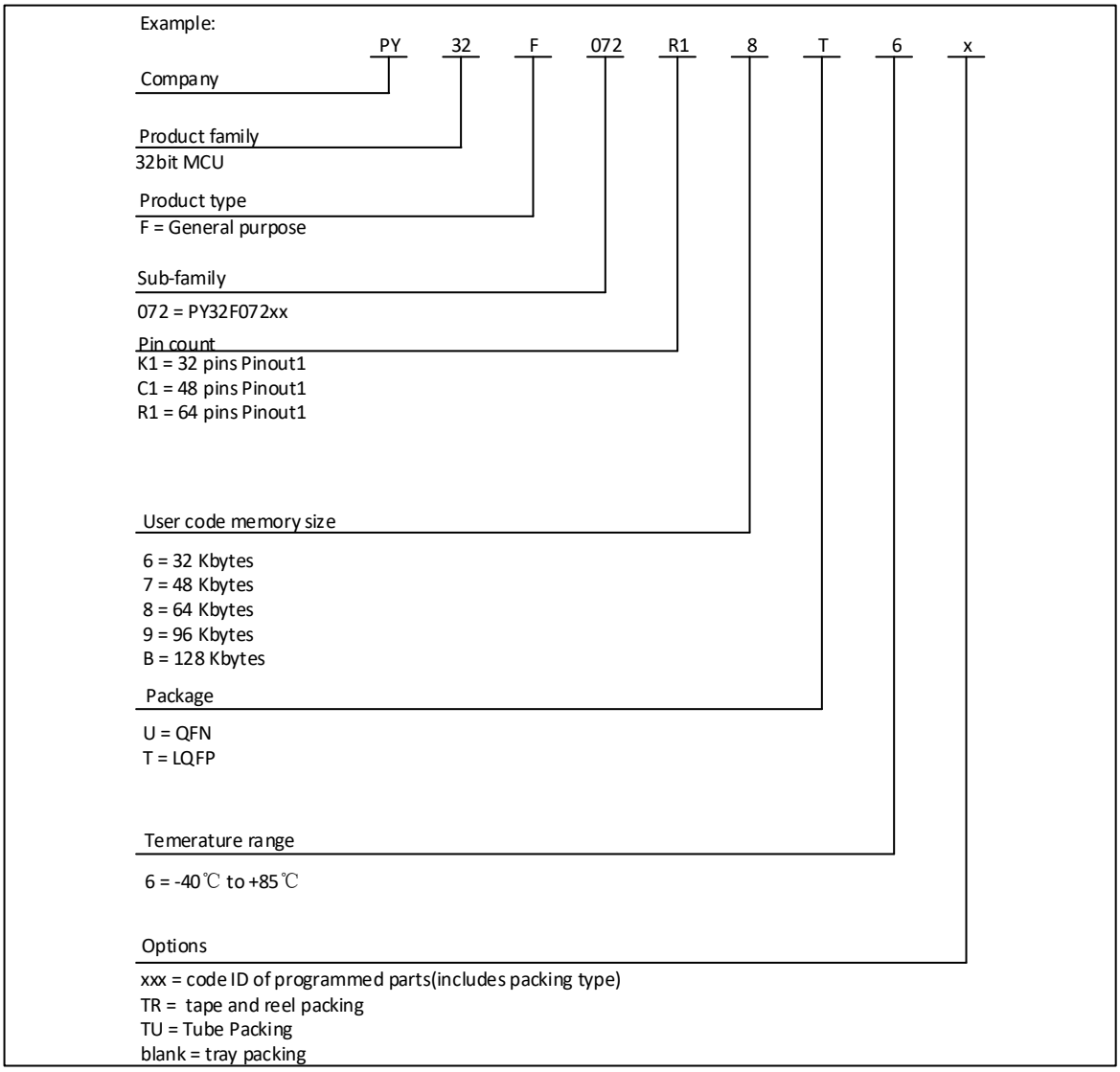
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
A3	0.590	0.640	0.690
b	0.330	-	0.410
c	0.130	-	0.170
D	8.800	9.000	9.200
D1	6.900	7.000	7.100
E	8.800	9.000	9.200
E1	6.900	7.000	7.100
e		0.800BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	LQFP32L(0707X1.4-0.8)	LQFP-32	B

8. Ordering Information



9. Version history

Version	Date	Update record
V0.1	2022.06.16	Pre-release version