MBI6033 Application Note

Foreword

The MBI6033 is a constant current LED driver for LED strips applications. The stability of data transmission has been improved through clock reverse and A-Token™ topology. This article mainly addresses five chapters:

1. The strip design, LED and current setting…etc.
2. The controller signal design, including notice for controller, CKI frequency notice… etc.
3. The production and setup, including the effect of hot swap, the design to reduce the surge voltage…etc.
4. The method of system testing.
5. Other applications notice, such as long distance transmission and logic level issue.

Chapter 1. Strips Design

Figure 1 shows the application circuit.

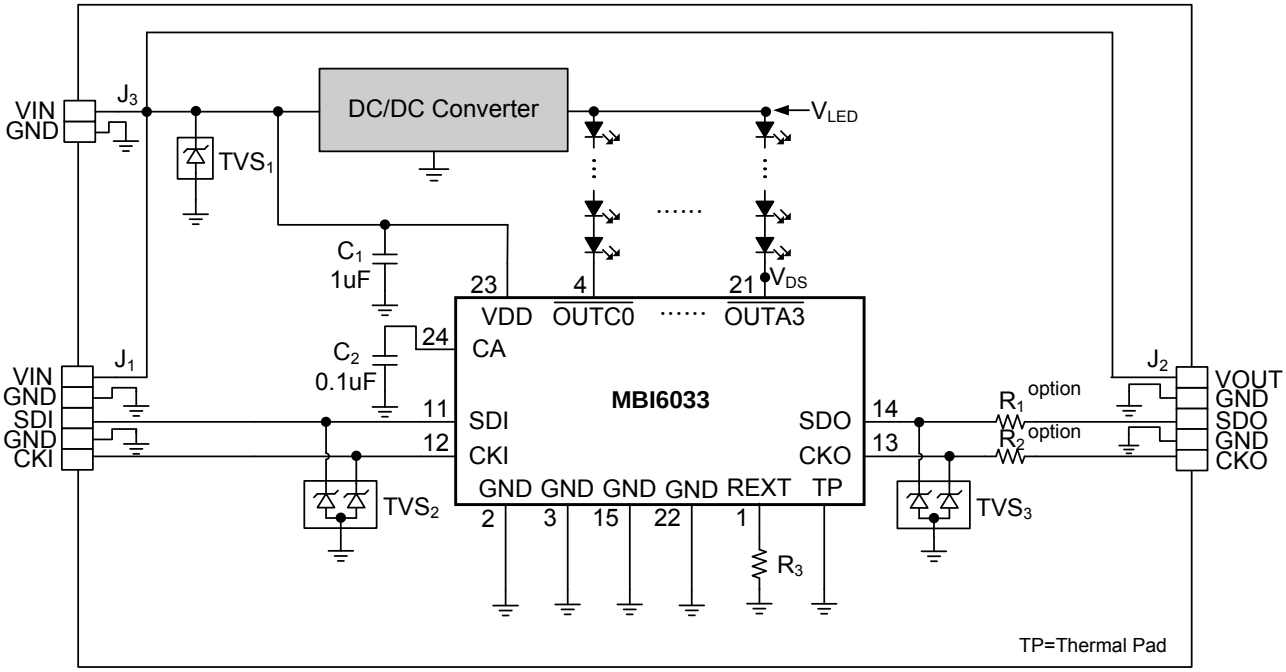

Figure 1. Application circuit

1. Notice about LED

The higher V_{LED} may result in high voltage drop on MBI6033's output port while adopting LEDs with large variation of forward voltage and then cause overheat. Therefore, LED forward voltage (V_F) sorting is necessary.

2. Setting Current Notice

MBI6033 allows users to set the three LED current (I_{OUT}) by an external resistor, R_3. MBI6033 current gain (CG) can be adjusted from 0 to127. No matter the output current is set by R_3 or current gain, the resulted current should be controlled in the output current range of MBI6033. After users decide the LED current, users can get a suitable R_3 by the following equation.

$$R_3 = (0.61V / I_{OUT}) \times 23 \times (CG/127) \quad \text{..... (1)}$$

R_3 must be placed close to MBI6033 in order to prevent R_3 from being disturbed. Moreover, the 1% tolerance resistor, is recommended in order to obtain the accurate output current.

To keep the MBI6033 constant current, a sufficient voltage at $\overline{OUTC0}$~$\overline{OUTA3}$ of MBI6033 (V_{DS}) is needed. Figure 2 and figure 3 show the I-V curves of MBI6033 when V_{CA} are 5V and 3.3V respectively. Users can refer to the figures and get a suitable V_{DS}. In general, the V_{DS} is slightly greater than the knee voltage. (Recommendation: $V_{DS} = V_{knee}+0.2V$)

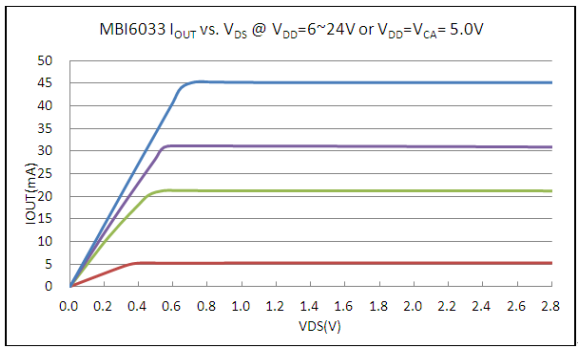

Figure 2. the relationship between I_{OUT} and V_{DS} of VDD=6~24V or VDD=VCA=5V

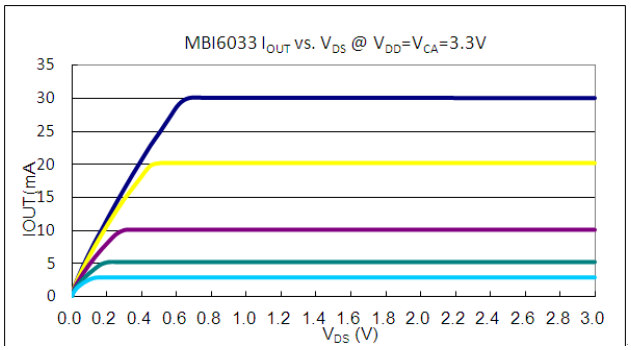

Figure 3. the relationship between I_{OUT} and V_{DS} of VDD=VCA=3.3V

When PCB layout, please keep the layout traces of output ports away from the SDI/CKI/SDO/CKO to avoid the interference of crosstalk. Or it is recommended to use the ground plane to separate these wires shown in figure 4.

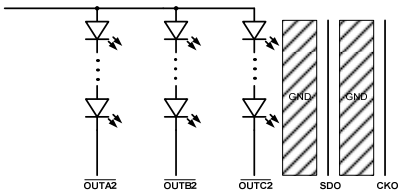

Figure 4. Use the ground plane to isolate SDI/CKI/SDO/CKO and $\overline{OUTC0}$~$\overline{OUTA3}$

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3. Setting LED Power

The minimum V_{LED} can be determined by the following equation

$$V_{LED,\ MIN.} = (V_{F,\ MAX.} \times n) + V_{DS} \quad \text{..... (2)}$$

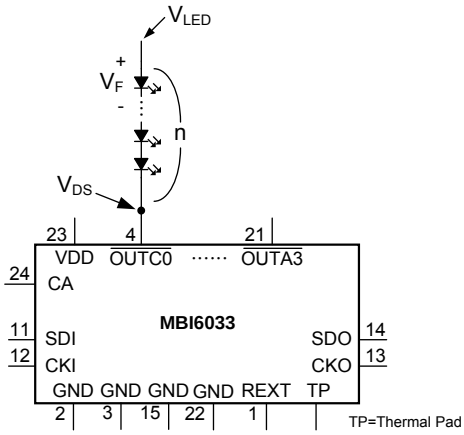

Figure 5. The sketch of minimum V_{LED} voltage

where $V_{F,MAX}$ represents the maximum forward voltage of LED, and n is the number of cascaded LEDs. The maximum sustaining voltage of $\overline{OUTC0}$~$\overline{OUTA3}$ is 28V.

4. Power Configuration

Because of the impedance of power lines, the voltage of each strip might be different in the multi- strip cascaded application as shown in figure 6. Figure 7 and figure 8 show the poor waveform of power. Users have to calculate the dropout voltage caused by the impedance of power line.

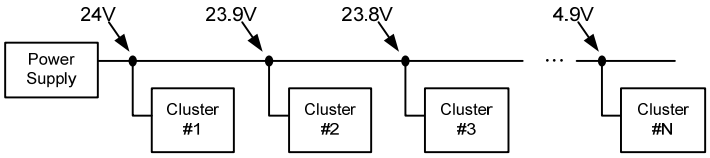

Figure 6. The sketch of dropout voltage in multi- strip cascaded application

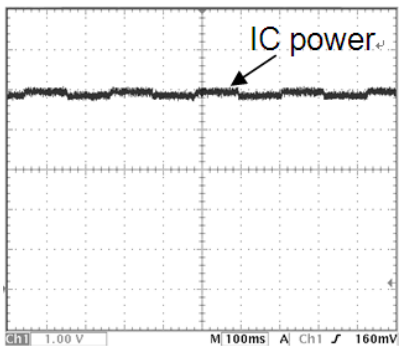

Figure 7. The poor waveform of power

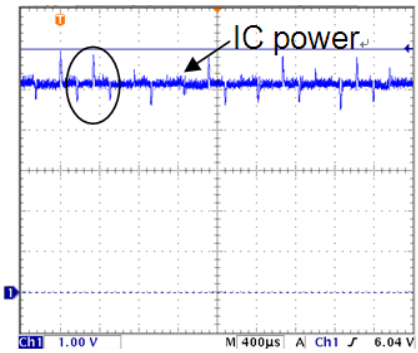

Figure 8. The poor waveform of power

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Figure 9 and figure 10 show the proposed method of the power and power distribution of strips respectively.

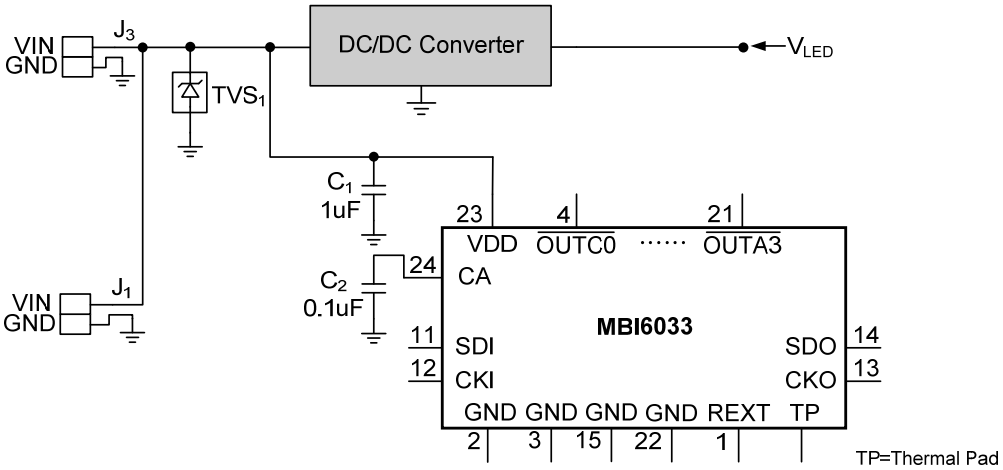

Figure 9. The proposed method of the power

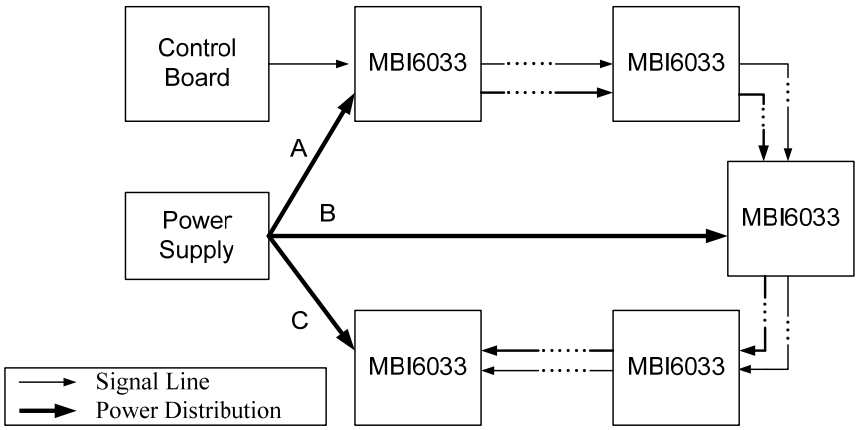

Figure 10. The power distribution of strips

For example, the maximum conductor impedance of AWG26 is 152Ω/km. It means that 1km transmission line is equal to 150Ω. If transmission line is 50cm and current is 20mA, there will be 1.52mV voltage drop. If the voltage is lower than that of DC/DC converter supply voltage, users should use a new power line.

Table 1. The specification of transmission line

UL 1007 CSA TR-64	Range		Conductor		Insulation		Tolerance mm	Maximum Conductor Resistance Ω/km	Permitable Current A	Minimum Insulation Resistance MΩ/km	(VAC/min) Insulation Potential Strength
	Temp ℃	Voltage V	AWG	NO./MM	Thickness mm	O.D. mm					
Stranded	UL 80℃ CSA 90℃	300V	32	7/0.080	0.38	1.00	±0.10	703	1.6	15	2000
			30	7/0.100	0.38	1.10	±0.10	397	2.0		
			28	7/0.127	0.38	1.20	±0.10	248	2.5		
			26	7/0.160	0.38	1.30	±0.10	152	3.5		
			24	11/0.160	0.38	1.45	±0.10	88.6	5.0		
			22	17/0.160	0.38	1.60	±0.10	62.5	7.0		
			20	21/0.180	0.38	1.85	±0.10	39.5	9.0		
			18	34/0.180	0.38	2.10	±0.10	24.4	13.0		
			16	26/0.254	0.38	2.40	±0.10	15.6	17.0		
Top-Coated(ATC)			30	7/0.100	0.38	1.10	±0.10	397	2.0		
			28	7/0.127	0.38	1.20	±0.10	248.0	2.5		
			26	7/0.160	0.38	1.30	±0.10	152.0	4.0		
			24	7/0.200	0.38	1.45	±0.10	88.6	5.3		
			22	7/0.254	0.38	1.60	±0.10	62.5	7.2		
Solid(TA)			26	1/0.404	0.38	1.25	±0.10	155	3.8		
			24	1/0.511	0.38	1.40	±0.10	92.4	5.3		
			22	1/0.643	0.38	1.55	±0.10	60.1	7.2		
			20	1/0.813	0.38	1.70	±0.10	37.0	9.4		
			18	1/1.020	0.38	1.96	±0.10	23.6	13.0		

5. Signal Quality

Good waveform quality should be no crosstalk , no overshoot/undershoot and the amplitude of the voltage is higher than V_{IH}. Figure 11 describes the signal waveform with good quality.

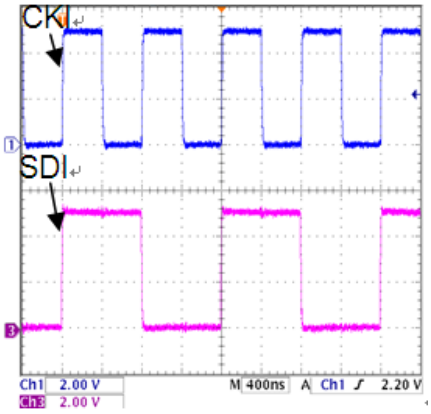

Figure 11. Good quality signal waveform

5.1 Cross-talk

When two signal lines are juxtaposed together, a phenomenon will happen on these two signals, as shown in figure 12. In order to suppress the cross-talk, a GND line to separate these two signals is necessary, as shown in figure 13. A twist pair cable is easy to suffer cross-talk. Therefore, it is not suggested to adopt the twin wires in this application.

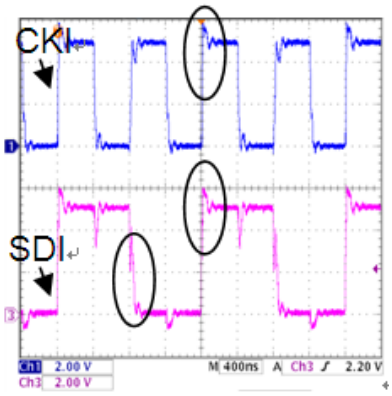

Figure 12. The waveform of cross-talk

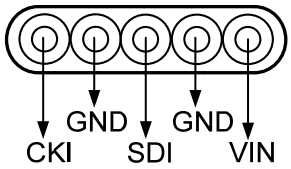

Figure 13. The arrangement of transmission line

In order to reduce the noise interference, the cable wire with shield is recommended to be the transmission line; also, the drain wire of braid shield and mylar foil must connect to ground.

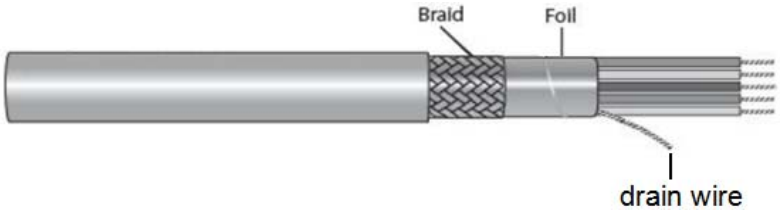

Figure 14. The cable wire with shield

5.2 Overshoot / Undershoot Voltage

Figure 15 shows the overshoot and undershoot voltage on SDI and CKI signals. In order to improve the signal quality, it is recommend to reserve the PCB positions of R_1 and R_2 in figure 16. The resistance of R_1 and R_2 will affect the rising and falling time of SDO/CKO. The larger resistance results in slower rising/falling time and reduce the effect of over/undershoot voltage. However, the large resistance might cause abnormal transmission.

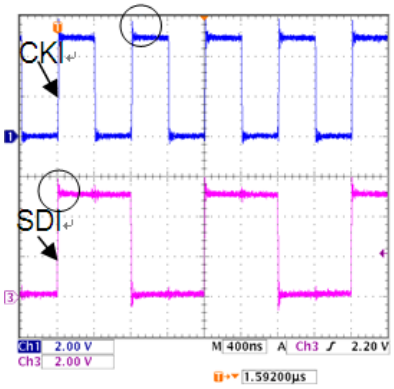

Figure 15. The poor waveform of overshoot or undershoot voltage

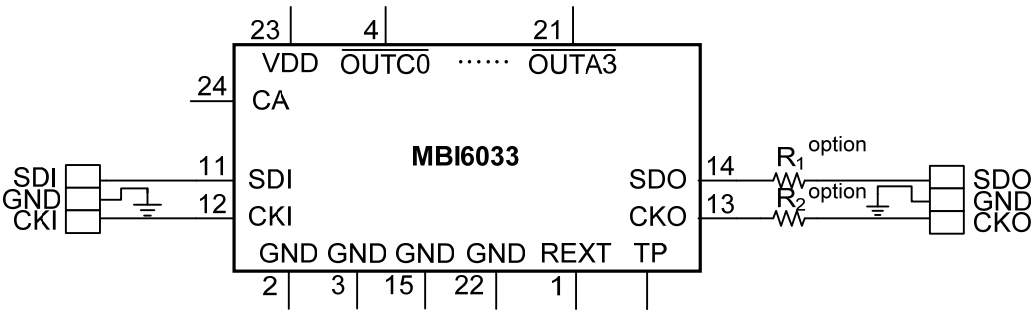

Figure 16. The sketch of how to improve the poor waveform

Figure 17 shows the waveform of CKI with TVS and the CKI frequency is 270kHz, users can increase the capacitor or increase frequency to alleviate the glitch.

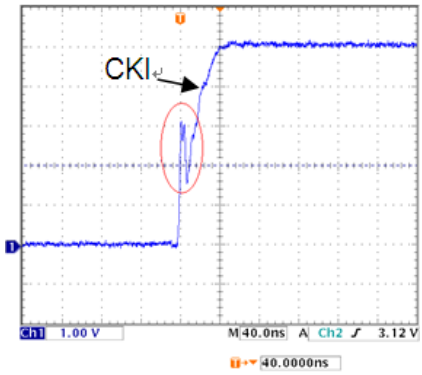

Figure 17. The poor waveform of overshoot voltage

5.3 Amplitude

The factors that affect amplitude include equivalent capacitance of wire, equivalent capacitance of TVS, voltage of CA and resistance of SDO/CKO. User can choose shorter wire to reduce the equivalent capacitance and smaller equivalent capacitance of TVS and adjust resistance of SDO/CKO.

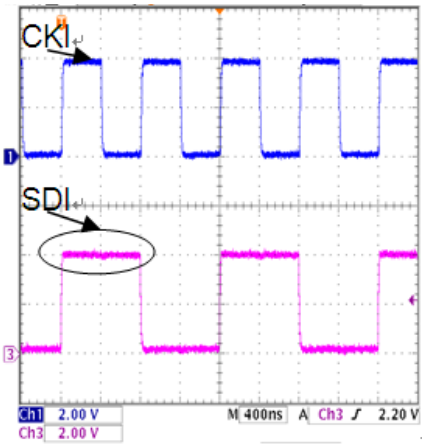

Figure 18. The poor waveform of insufficient amplitude

6. Notice about CA

In order to stabilize the internal digital circuit, CA should not connect to any other device. A ceramic capacitor with 0.1uF is recommended to connect to CA pin.

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Chapter 2. Control Signal Design

1. Notice for Controller

To enhance the validity of control signal, the control signal should be outputted after the power supplies of controller and module are stable, as figure 19 shows. The transmission lines of SDI and CKI from controller to first strip should be separated by a ground line and add a GND on connector to be the common ground.

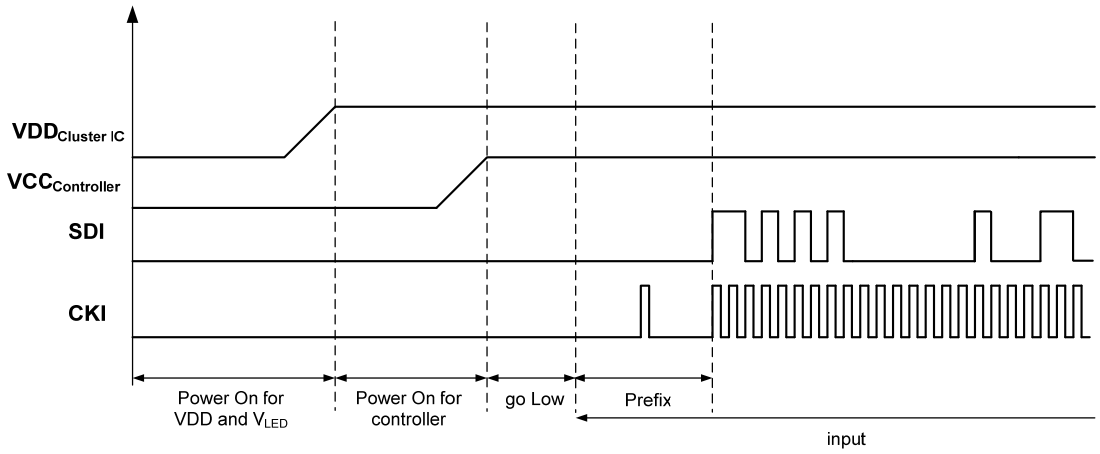

Figure 19. Power sequence

2. CKI Frequency Notice

The minimum CKI frequency of MBI6033 is 200kHz. Users should use fixed CKI frequency to improve system stability.

3. CKI Stop Time

The time-out protection of MBI6033 is to check the validity of data counter by counting the duration of CKI stop through the internal counter. If two events of CKI stops exceeds 20us happened continuously, MBI6033 will ignore the present input data and keep the previous data until the correct data is inputted.

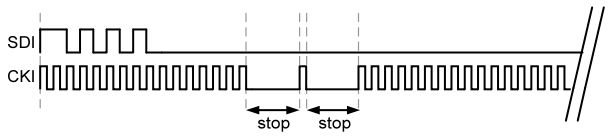

Figure 20. Diagram of CKI stop time

4. Input Signal

The output signal of controller should allow the falling edge of CKI in the middle of SDI data. The recommended CKI is 50% of the duty, as shown in figure 21.

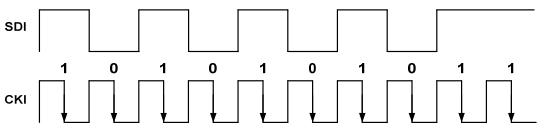

Figure 21. The falling edge of CKI in the middle of SDI data

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The correct input signal format should consist of Prefix, Header and Data.

Prefix	Header	Data

4.1 Prefix

The prefix is the event of CKI continuous stops two times and the stop time exceeds 21us. In order to make MBI6033 realize the new gray scale and meet the image refresh time (T_{frame}), the following equations can be used to calculate the prefix.

$$T_{prefix} \leqq T_{frame} - T_{Data} \quad \text{..... (3)}$$

$$T_1, T_2 > 21us \quad \text{..... (4)}$$

where T_{Data} represents the time of transmission, T_{Data} of Non-current gain mode is $T_{Data}= T_{CKI}$ x (48 + (48 x 4) x N) and Current gain mode is $T_{Data}= T_{CKI}$ x (48 + (24 + 48 x 4) x N), N is the amount of cascaded IC and T_{CKI} is the CKI period, as shown in figure 22.

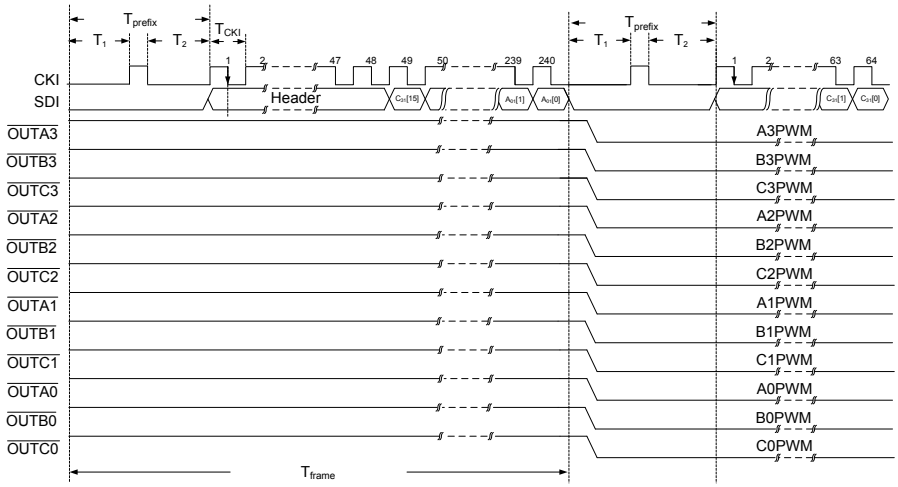

Figure 22. Non-current gain mode of prefix

Example

Number of MBI6033 in cascade: 64 pcs

Gray scale data:16-bit

Period of CKI (T_{CKI}): 1us (1/1MHz),

Refresh time of a frame: 16.67ms (1/60Hz).

From equation (3), T_{prefix} = 16.67ms –1us x (48 + (48 x 4) x 64) = 4.33ms. T_1, T_2=(4.33ms – 1us)/2=2165.25us. The time is larger than the time of 21us. The data stream can be recognized, as shown in figure 23.

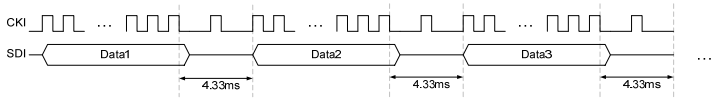

Figure 23. The Diagram of prefix is 4.33ms

4.2 Header

The correct Header must be transmitted before the data to make sure each MBI6033 can catch the data with correct address. The header includes H (Command Header), S (Sync), L (Length), CF (Configuration) and X1 (or SV).

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4.2.1 Command Header

MBI6033 has three types of command headers, as shown in table 2. According to the definition of each header, the consequent data will be written to current data.

Table 2. Three kinds of command

Command H[7:0]	Data Type
8'b11010101	Current gain mode
8'b11110011	Non-current gain mode
8'b11000001	Software reset

4.2.2 Sync and Length

The length data will minus 1 whenever the data chain pass to the next IC, and the Most Significant Bit (MSB) will be exported first to length the next IC. When the data of length is the zero, the data will be latched to register. ***The L (Length) of MBI6033 is the amount of cascaded ICs minus one*****.** For example, if there are three MBI6033 in cascaded, the L (Length) will be 2 (14'b00000000000010), and ***the initial S (Sync) is 0 (14b'00000000000000)*****.**

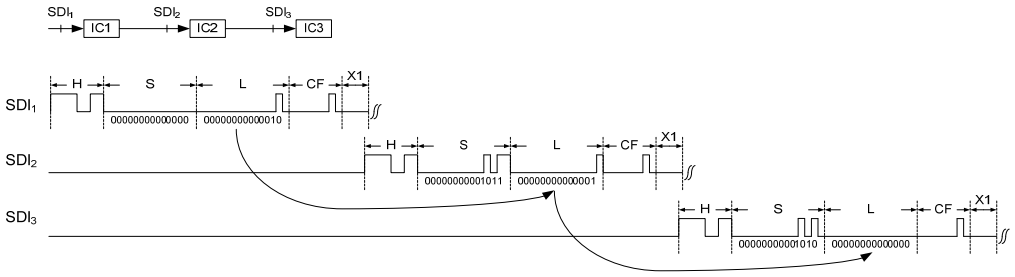

Figure 24. Diagram of Length

4.2.3 CF

CF[6:4] is used to set up the GCLK divider. The width of PWM can be determined by the following equation

The width of PWM =GCLK x1024 ..... (5)

Table 3. GCLK divider

CF[6:4]	GCLK	CF[6:4]	GCLK
000	GCLK= internal oscillator (F_{osc})	100	GCLK=internal oscillator (F_{osc})/16
001	GCLK= internal oscillator (F_{osc})/2	101	GCLK= internal oscillator (F_{osc})/64
010	GCLK= internal oscillator (F_{osc})/4	110	GCLK= internal oscillator (F_{osc})/128
011	GCLK=internal oscillator (F_{osc})/8	111	GCLK= internal oscillator (F_{osc})/256

CF[1] is used to control the output ports; when CF[1]=1, all the output ports will be turned on, and vice versa.

4.2.4 X1

The code name of Header[3:0] is X1, and the recommended value is 4'b0000.

Following shows the example of two MBI6033 in cascade with different commands

Current Gain Mode

There are 2x(24+4x48) bits data behind the X1. Since the maximum current (CG) of MBI6033 is 127, the recommended value of CG[7] is 0.

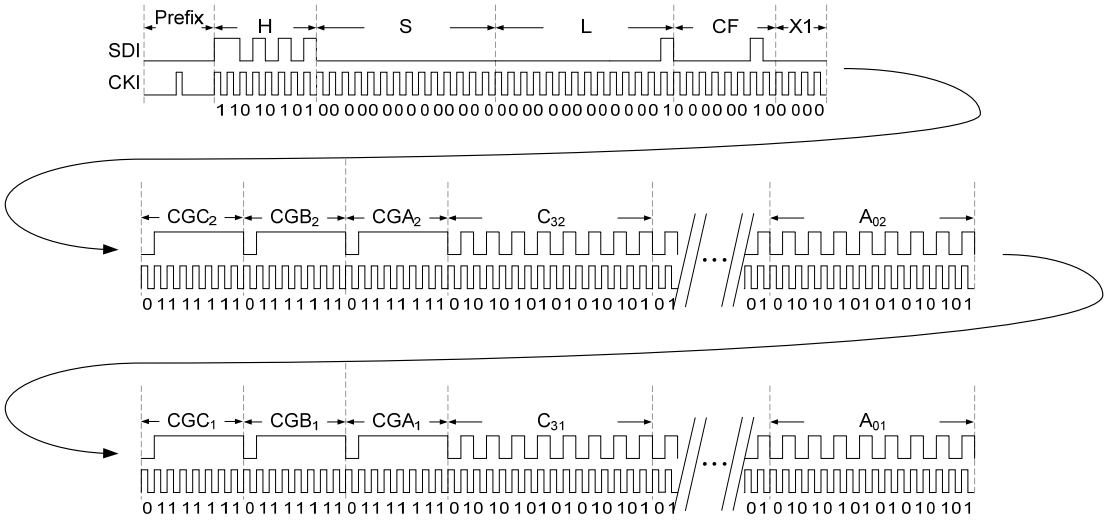

Figure 25. Current gain mode

Non-Current Gain Mode

There are 2x4x48 bits data behind the X1. In non-current gain mode, the maximum current gain (CG) of MBI6033 is 127.

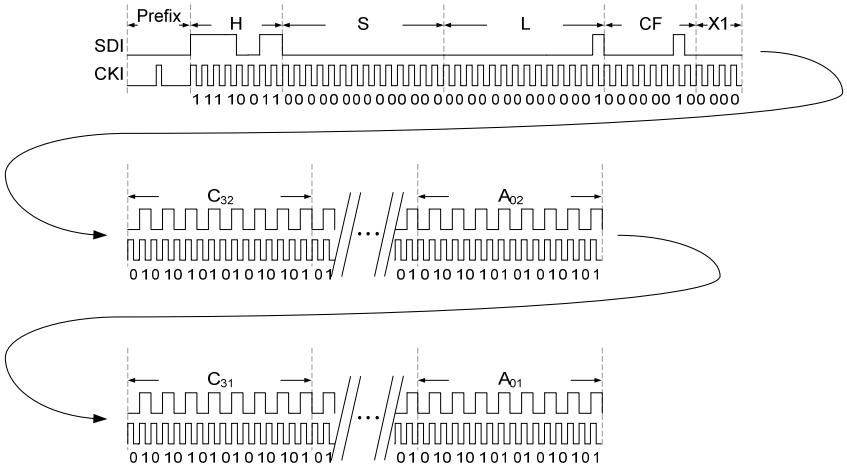

Figure 26. Non-current gain mode

Software Reset

There are 2x4x48 bits data behind the X1, and IC will be reset to the initial state after executed the software reset command.

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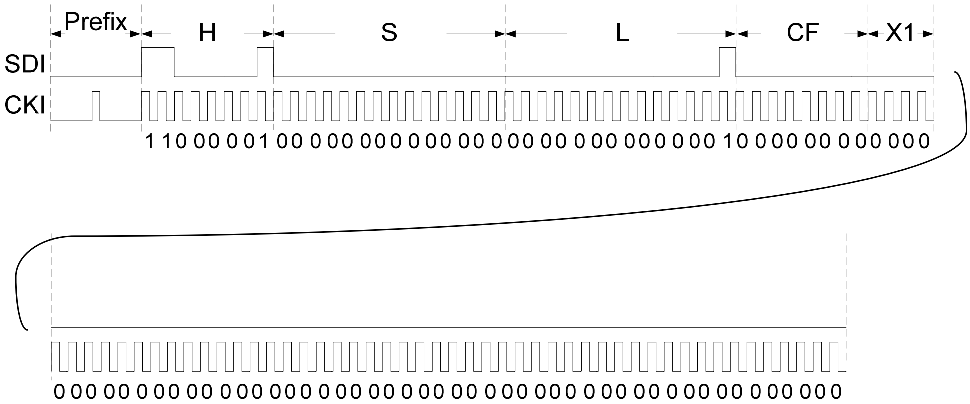

Figure 27. Software reset

Chapter 3. Production and Setup

1. The Effect of Hot Swap

Hot swapping means the action of connecting or disconnecting the pin of VDD/SDI/CKI/SDO/CKO of MBI6033. It will induce the heavy instantaneous current and high voltage, and then damage the IC. Besides increasing the EOS protection component as mentioned, users also may add the longer ground terminal in connectors, and operate the correct procedures to avoid hot swap.

2. Design to Reduce Strike Voltage

2.1 Resistance

Cascade a resistor at SDO and CKO can reduce the probability of IC been damaged by hot swap. The larger resistance results the lower probability of damage problem, and the lower speed of transmission. The recommended resistances of R_2 and R_3, which are shown in figure 16, are 10Ω.

2.2 Connector

When setting up or removing the connecter of strip instantly, in order to reduce the unexpected spike voltage and to avoid IC been burned out, users need to turn off the power, and then set up or remove the strip. It is better to connect GND first. Users can design the longer GND terminal in connector pin than in VDD terminal in connector to reduce the unexpected strike voltage, as shown in figure 32.

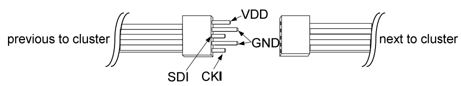

Figure 32. The safety design of longer terminal ground

2.3 Transient Voltage Suppressor

All Macroblock products have passed the standard of ESD protection. But to enhance the capacity of Electrical Over Stress (EOS) protection, an external device, Transient Voltage Suppressor (TVS), is necessary. Figure 33 shows the positions of TVS_1~TVS_3, and followings are the guidelines for TVS selection.

Select TVS_1

a. The maximum Reverse Stand-Off Voltage (V_{RWM}) should be equal to module's input voltage.

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b. The maximum clamping voltage (V_C) should be higher than module's input voltage.

c. The maximum Peak Pulsed Power (P_{PPM}) is the product of maximum clamping voltage and peak pulse current.

d. TVS diode should be placed to the pins that need to protect as close as possible to prevent the EOS.

Select TVS_2 and TVS_3

a. The maximum Reverse Stand-Off Voltage (V_{RWM}) should be equal to 5V.

b. The maximum clamping voltage (V_C) should be equal to 7V.

c. The maximum Peak Pulsed Power (P_{PPM}) is the product of maximum clamping voltage and peak pulse current, and it should be determined by the measured surge amplitude.

d. TVS diode should be placed to the pins that need to protect as close as possible to prevent the EOS.

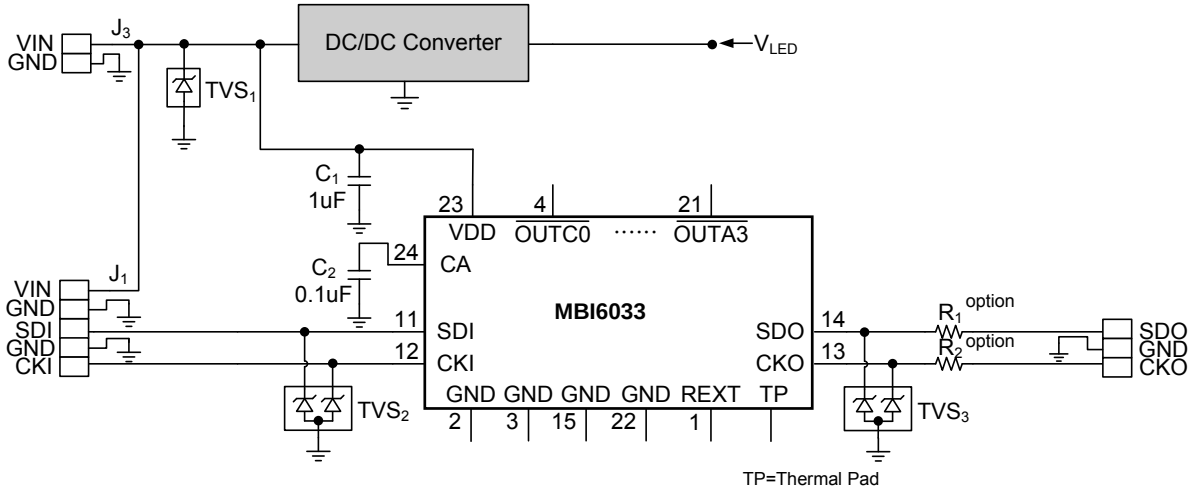

Figure 33. Apply the electrical overstress protection

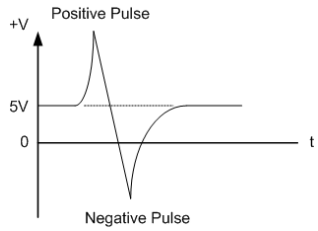

Figure 34. Without use EOS component

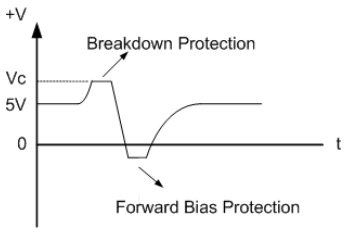

Figure 35. With use EOS component

3. Production and Setup Procedures

The following procedures should be observed in producing and installing the modules. In order to avoid the controller from providing a valid power to the IC and cause the EOS through the ESD protection circuit. Modules in the production and installation should carefully follow the correct procedures:

Step 1: Before install the module, please turn all the power off.

Step 2: The procedure of electrostatic discharge should be taken before connecting the cluster.

Step 3: Make sure the grounding system has been properly grounded.

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Step 4: Make sure all the conducting wires of power supply and controller have completed and correctly contacted with connector.

Step 5: After the above procedures have been executed, then start the system power supply.

Step 6: After the system power is stable, then start the controller power supply.

Step 7: Before the procedures of cluster removing or repairing welding, users have to turn off the controller power first and then the system power. After the residual charge has been completely discharged, then the rework procedures can be executed.

4. Printed Circuit Board Notice

1. Users should avoid empty solder, cold solder, and split solder in manufacturing process of Printed Circuit Board (PCB).
2. Device layout should avoid approaching the board edge of PCB.
3. To design the longer size of PCB, it is suggested to select the thick slab value of PCB to avoid soldering issues due to board bending.

Chapter 4. The Method of System Testing

The CKI frequency is 1MHz, RGB gray scale data is 16'b0101010101010101, and the LED turns on sequence is R→G→B→R→G…. If the LED works normally, the CKI frequency can be increased to 500kHz until LED works abnormally. If the LED can't work normally, then the CKI frequency should be decreased. The lowest CKI frequency is 200kHz. If LED still can't work under this frequency, please check if the signals of SDI and CKI have been distorted.

Chapter 5. Other Application Notice

1. Using the Long Power Line on the PCB

If users have to use the long power line on the PCB, the distributed capacitors, which figure 36 shows, are recommended. The value of C_d depends on the distance between each power line.

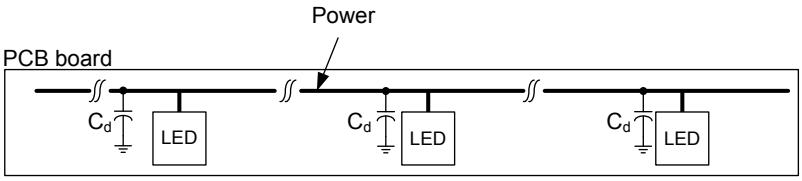

Figure 36. The sketch of distributed capacitance

2. Logic Level Issue

Because of the impedance of power lines, the VDD voltage of each strip might be less 6V, which will cause voltage drop on CA and affect the logic level of MBI6033 in the multi- strip cascaded application, as shown in figure 37. When CA is 5V, the V_{IH}/V_{IL} level will be 3.65V/1.4V respectively. And if the CA of another cluster is 4V, the logic level will be 2.92V/1.12V. The different logic level will cause a different trigger time and then impact the signal transmission. Please refer to the section of "Power Configuration" for the suggested method.

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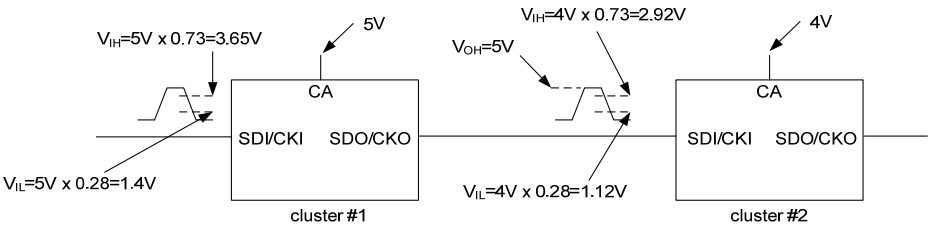

Figure 37. The diagram of different CA

Summary

In the application of multiple strips cascaded, the following notices must be taken

1. The transmission line with small parasitic inductance is required to enhance the signal quality.
2. To prevent the insufficient V_{LED}, which is caused by the conductor resistance in transmission line, results the problem of strip brightness unbalance, please refer figure 3 to design the power source.
3. Please refer to chapter 3, “Production and Installation”, to protect IC being damaged from hot-plug in. Please take a note, even the processes in chapter 3 have been executed, it only can reduce the probability of burn-out when hot-plug in, can’t totally solve the problem.

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