Data Sheet

MM32SPIN05x

32-bit Microcontroller Based on Arm®Cortex®-M0

版本：**1.24**

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1 General Introduction

1.1 Introduction

This product incorporates a high performance 32 bit microcontroller with the core of Arm® Cortex®M0. The highest operating frequency is up to 72MHz, with builtin high-speed memory, a rich set of I/O ports and peripherals connected to the external bus. This product contains one 12 bit ADC, one comparator, one 16bit generalpurpose timer, one 32bit generalpurpose timer, three 16bit basic timers, one 16bit advanced timer, and standard communication interfaces, including one I2C, two SPI and two UART interfaces.

The device works between 2.0V to 5.5V range. The regular temperature for the device is 40◦C to +85◦C and 40◦C to +105◦C extended temperature range are also available. A comprehensive set of powersaving mode allows the design of lowpower applications。

The abundant peripherals make this microcontroller suitable for a variety of applications:

- Motor drive and application control
- Medical and handhled devices
- PC gaming peripherals and GPS platform
- ndustrial applications: programmable controllers (PLCs), inverters, printers and scan-ners
- Alarm system, video intercom, heating, ventilation and air conditioning

The devices are available in 5 different packages: LQFP48, LQFP32, QFN32, QFN20 and TSSOP20.

1.2 Product Characteristics

- Core and system
  - 32bit Arm® Cortex®M0 processor as the core
  - Maximum operating frequency is up to 72MHz
  - Single cycle 32bit hardware multiplier
  - Hardware divider(32bit)
- Memory
  - 32K bytes of Flash memory
  - 4K bytes of SRAM
  - Boot loader supports Chip Flash and ISP (InSystem Programming)
- Clock, reset and power management
  - 2.0V to 5.5V power supply
  - Poweron/Powerdown reset (POR/PDR), Programmable voltage detector (PVD)
  - External 4 ~ 24MHz high speed crystal oscillator
  - Embedded factorytuned 48/72MHz high speed oscillator
- Low-power
  - Sleep, Stop and Standby modes
- One 12bit ADC and 1μS of conversion time (up to 13 channels)
  - Conversion range: 0 to V_{DDA}
  - Support sampling time and resolution configuration

  - Onchip temperature sensor
  - Onchip voltage sensor
- One comparator
- One 5-channel DMA controller
  - Supported peripherals: Timer, UART, I2C, SPI and ADC
- Up to 39 fast I/Os:
  - All I/O ports can be mapped to 16 external interrupts
  - All ports are capable of inputting and outputting 5V signals
- Up to 9 timers
  - One 16bit 4channel advancedcontrol timer with 4channel PWM output, dead-time generation and emergency stop
  - One 16bit timer and one 32bit timer, with up to 4 IC/OC, usable for IR control decoding
  - Two 16bit timer, with one IC/OC, one OCN, deadtime generation and emergency stop and modulator gate for IR control
  - One 16bit timer, with one IC/OC
  - Two watchdog timers (independent and window type)
  - One SysTick timer: 24bit downcounter
- Debug mode
  - Serial wire debug (SWD)
- Up to 5 Communication interfaces
  - Two UARTs
  - One I2C
  - Two SPIs
- 96bit unique ID (UID)
- Packages LQFP48, LQFP32, QFN32, QFN20 and TSSOP20

2 Specification

2.1 Model List

2.1.1 Ordering Information

Table 1 Ordering Information

Model / Peripheral Interface		MM32SPIN05PF	MM32SPIN05PT	MM32SPIN05NT	MM32SPIN05NW/TW
CPU frequency		72MHz			
Flash memory KB		32	32	32	32
SRAM KB		4	4	4	4
Timer	General-purpose (16 bit)	4	4	4	4
	General-purpose (32 bit)	1	1	1	1
	Advanced control	1	1	1	1
Communication interface	UART	2	2	2	2
	I2C	1	1	1	1
	SPI / I2S	2	1	1	1
Number of GPIO		39	25	27	16
12-bit ADC	Number	1	1	1	1
	Number of channels	13	13	13	9
Comparator		1	1	1	1
Working voltage		2.0V~5.5V			
Working temperature		-40℃~105℃			
Package		LQFP48	LQFP32	QFN32	QFN20/TSSOP20

2.1.2 Marking Information

Marking
QFN marking:

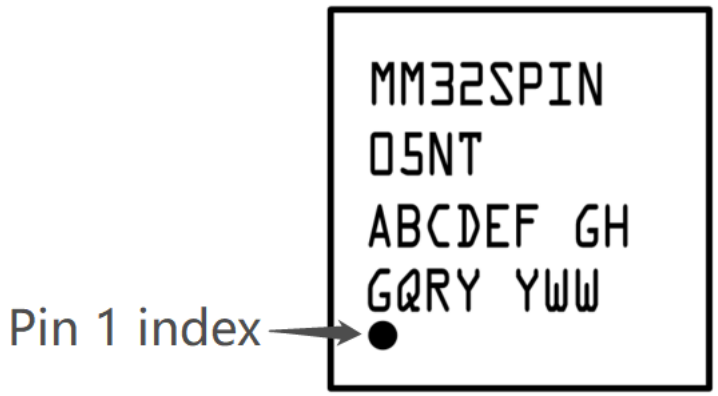

Figure 1 QFN32 package marking

QFN32 package has the following topside marking:

- 1st line：MM32SPIN
  - First part of product name
- 2nd line：05NT
  - Second part of product name
- 3rd line：ABCDEF -Trace code
  GH-Revision code
- 4th line：GQRY YWW
  - “GQRY”，other information；“YWW”,Date code，“Y” means year and “ww” means week in date code

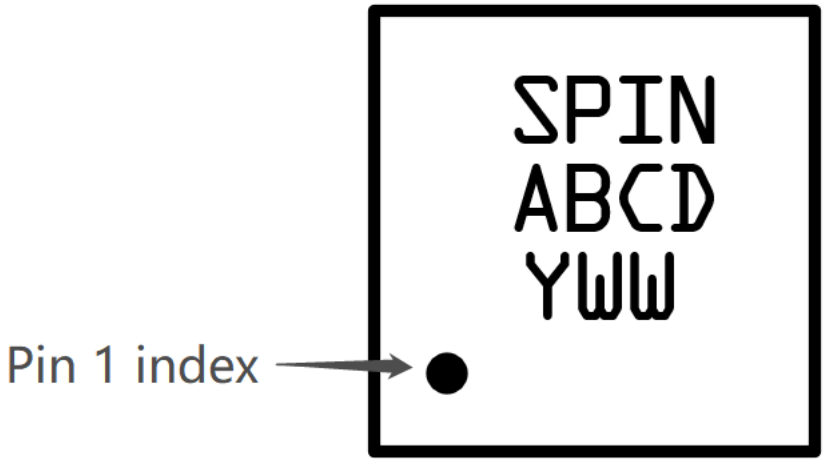

Figure 2 QFN20 package marking

QFN20 3x3 package has the following topside marking:

- 1st line：SPIN
  - Motor product
- 2nd line：ABCD
  - Trace code
- 3rd line：YWW
  - Date code，“Y” means year and “ww” means week in date code

Marking

LQFP marking:

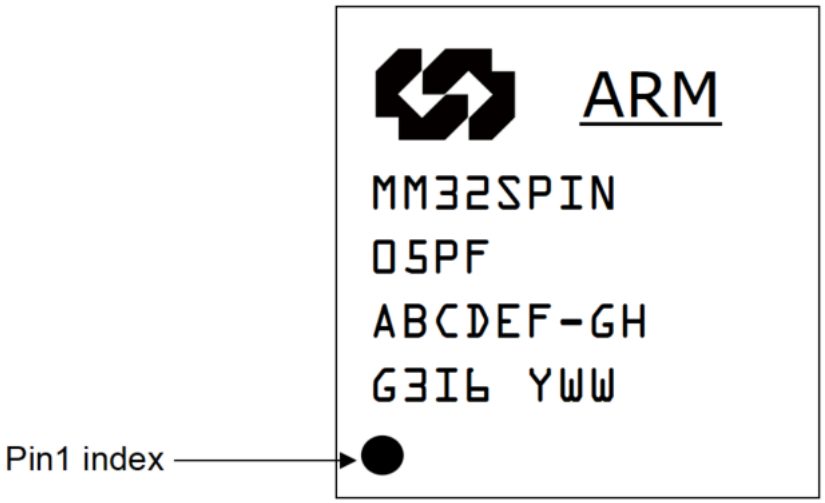

Figure 3 LQFP package marking

LQFP package has the following topside marking:

- 1st line：
  - Company logo+ARM
- 2nd line：MM32SPIN
  - First part of product name
- 3rd line：05PF/05PT
  - Second part of product name
- 4th line：ABCDEF -Trace code
  GH-Revision code

- 5th line：GQRY YWW
  - “GQRY”，other information；“YWW”,Date code，“Y” means year and “ww” means week in date code

Marking

TSSOP marking:

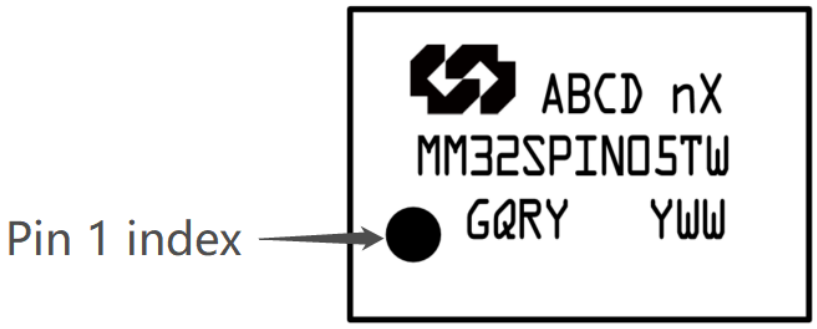

Figure 4 TSSOP package marking

TSSOP20 package has the following topside marking

- 1st line：
  - Company logo
  - ABCD means Trace code
  - nX means Revision code
- 2nd line：MM32SPIN05TW
  - Product name
- 3rd line：GQRY YWW
  - “GQRY”，other information；“YWW”,Date code，“Y” means year and “ww” means week in date code

2.1.3 Block Diagram

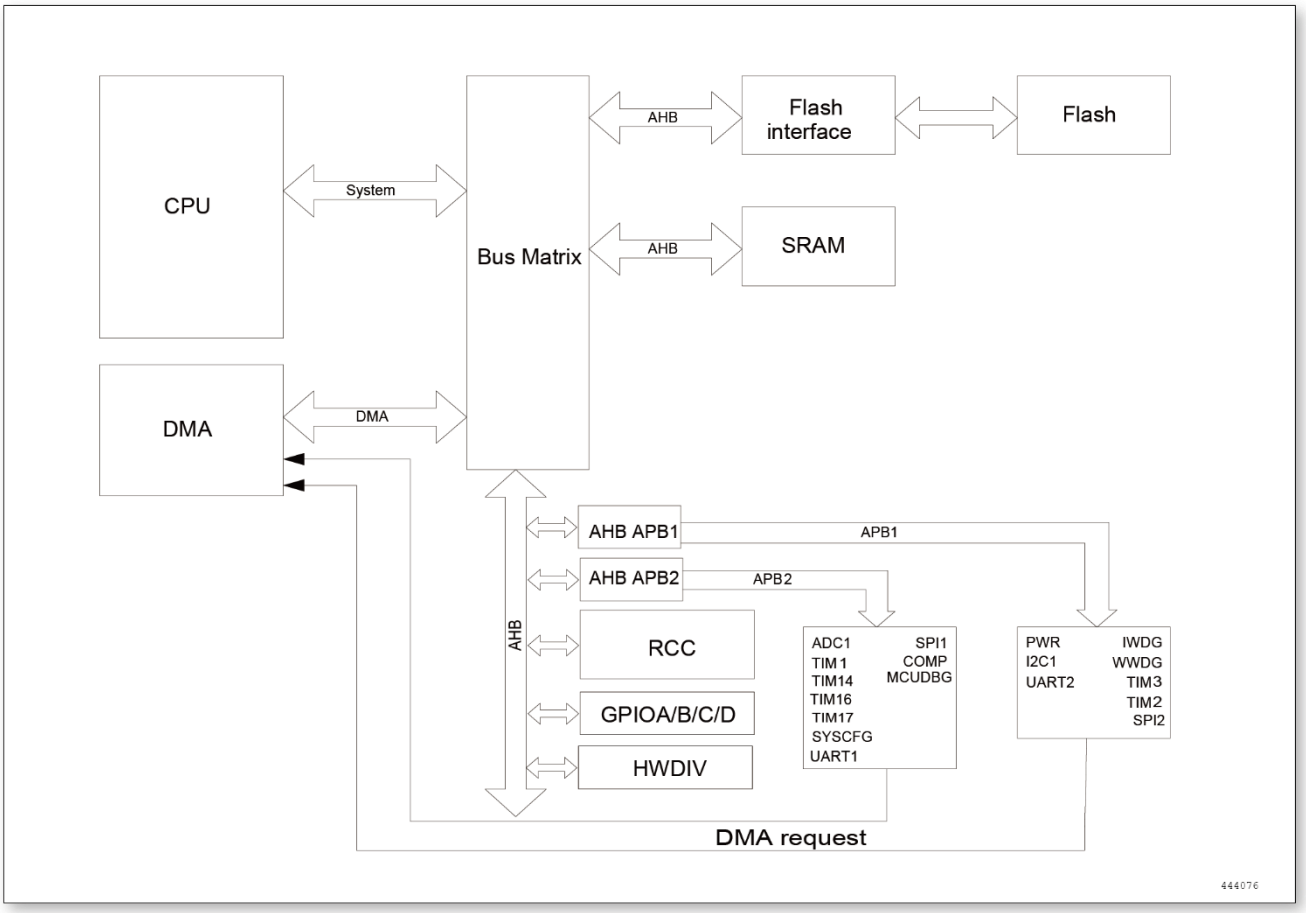

Figure 5 Block diagram

2.2 Functional Description

2.2.1 Arm® Cortex®M0 with embedded flash memory and SRAM

The Arm® Cortex®M0 processor is configurable and has multilevel pipeline 32 bit reduced instruction set processor, and characterized by high performance and low power consumption.

2.2.2 Embedded flash memory

The embedded flash memory is up to 32K bytes, usable for storing programs and data.

2.2.3 Memory mapping

Table 2 Memory mapping

Bus	Boundary address	Size	Peripheral
FLASH	0x0000 0000 0x0000 7FFF	32 KB	Main flash memory, system memory, or SRAM, depends on the configuration of BOOT
	0x0000 8000 0x07FF FFFF	~ 128 MB	Reserved
	0x0800 0000 0x0800 7FFF	32 KB	Main Flash memory
	0x0800 8000 0x1FFD FFFF	~256 MB	Reserved
	0x1FFE 0000 0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200 0x1FFE 0FFF	3 KB	Reserved
	0x1FFE 1000 0x1FFE 1BFF	3 KB	Reserved
	0x1FFE 1C00 0x1FFF F3FF	~256 MB	Reserved
	0x1FFF F400 0x1FFF F7FF	1 KB	System memory
	0x1FFF F800 0x1FFF F80F	16 B	Option bytes
	0x1FFF F810 0x1FFF FFFF	~2 KB	Reserved
SRAM	0x2000 0000 0x2000 0FFF	4 KB	SRAM
	0x2000 1000 0x2FFF FFFF	~ 512 MB	Reserved
APB1	0x4000 0000 0x4000 03FF	1 KB	TIM2
	0x4000 0400 0x4000 07FF	1 KB	TIM3
	0x4000 0800 0x4000 27FF	8 KB	Reserved
	0x4000 2800 0x4000 2BFF	1 KB	Reserved
	0x4000 2C00 0x4000 2FFF	1 KB	WWDG
	0x4000 3000 0x4000 33FF	1 KB	IWDG
	0x4000 3400 0x4000 37FF	1 KB	Reserved
	0x4000 3800 0x4000 3BFF	1 KB	SPI2
	0x4000 4000 0x4000 43FF	1 KB	Reserved
	0x4000 4400 0x4000 47FF	1 KB	UART2
	0x4000 4800 0x4000 4BFF	3 KB	Reserved
	0x4000 5400 0x4000 57FF	1 KB	I2C1
	0x4000 5800 0x4000 5BFF	1 KB	Reserved
	0x4000 5C00 0x4000 5FFF	1 KB	Reserved
	0x4000 6000 0x4000 63FF	1 KB	Reserved
	0x4000 6400 0x4000 67FF	1 KB	Reserved
	0x4000 6800 0x4000 6BFF	1 KB	Reserved

Bus	Boundary address	Size	Peripheral
	0x4000 6C00 0x4000 6FFF	1 KB	Reserved
	0x4000 7000 0x4000 73FF	1 KB	PWR
	0x4000 7400 0x4000 FFFF	1 KB	Reserved
APB2	0x4001 0000 0x4001 03FF	1 KB	SYSCFG
	0x4001 0400 0x4001 07FF	1 KB	EXTI
	0x4001 0800 0x4001 23FF	7 KB	Reserved
	0x4001 2400 0x4001 27FF	1 KB	ADC1
	0x4001 2800 0x4001 2BFF	1 KB	Reserved
	0x4001 2C00 0x4001 2FFF	1 KB	TIM1
	0x4001 3000 0x4001 33FF	1 KB	SPI1
	0x4001 3400 0x4001 37FF	1 KB	DBGMCU
	0x4001 3800 0x4001 3BFF	1 KB	Reserved
	0x4001 3C00 0x4001 3FFF	1 KB	COMP
	0x4001 4000 0x4001 43FF	1 KB	TIM14
	0x4001 4400 0x4001 47FF	1 KB	TIM16
	0x4001 4800 0x4001 4BFF	1 KB	TIM17
	0x4001 4C00 0x4001 7FFF	13 KB	Reserved
AHB	0x4002 0000 0x4002 03FF	1 KB	DMA
	0x4002 0400 0x4002 0FFF	3 KB	Reserved
	0x4002 1000 0x4002 13FF	1 KB	RCC
	0x4002 1400 0x4002 1FFF	3 KB	Reserved
	0x4002 2000 0x4002 23FF	1 KB	Flash 接口
	0x4002 2400 0x4002 5FFF	15 KB	Reserved
	0x4002 6000 0x4002 63FF	1 KB	Reserved
	0x4002 6400 0x4002 FFFF	39 KB	Reserved
	0x4003 0000 0x4003 03FF	1 KB	HDIV
	0x4003 0400 0x47FF FFFF	~ 128 MB	Reserved
	0x4800 0000 0x4800 03FF	1 KB	GPIOA
	0x4800 0400 0x4800 07FF	1 KB	GPIOB
	0x4800 0800 0x4800 0BFF	1 KB	GPIOC
	0x4800 0C00 0x4800 0FFF	1 KB	GPIOD
	0x4800 1000 0x5FFF FFFF	~ 384 MB	Reserved

2.2.4 Embedded SRAM

4K Bytes of embedded SRAM.

2.2.5 Nested vectored interrupt controller (NVIC)

This product embeds a nested vectored interrupt controller, which can handle multiple maskable interrupting channels (excluding 16 Cortex® M0 interrupt lines) with 16 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry address directly enters into the core
- Tightly coupled NVIC interfaces
- Allow early processing of interrupts
- Handle higher priority interrupts that arrive late

- Support tailchaining of interrupts
- Automatically saves the processor state
- Offer automatic recovery when the interrupt returns with no instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.2.6 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of multiple edge detectors used to generate interrupt/event requests. Each interrupt line can be independently configured to select the trigger event (rising edge, falling edge or both) and can be masked independently. A pending register maintains the status of all interrupt requests. The EXTI can detect a signal with a pulse width shorter than the internal AHB clock period. All GPIOs can be connected to the 16 external interrupt lines.

2.2.7 Clocks and startup

System clock selection is performed on startup, however the internal 48 MHz oscillator is selected as default CPU clock on reset. Then an external 2~24 MHz clock with failure monitoring function can be selected. If an external clock failure is detected, the clock will be isolated. The system automatically switches back to the internal oscillator. If an interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure AHB frequency and highspeed APB (APB2 and APB1) domain. The maximum frequency of AHB and highspeed APB is 72MHz. Please refer to the clock drive diagram in figure 6.

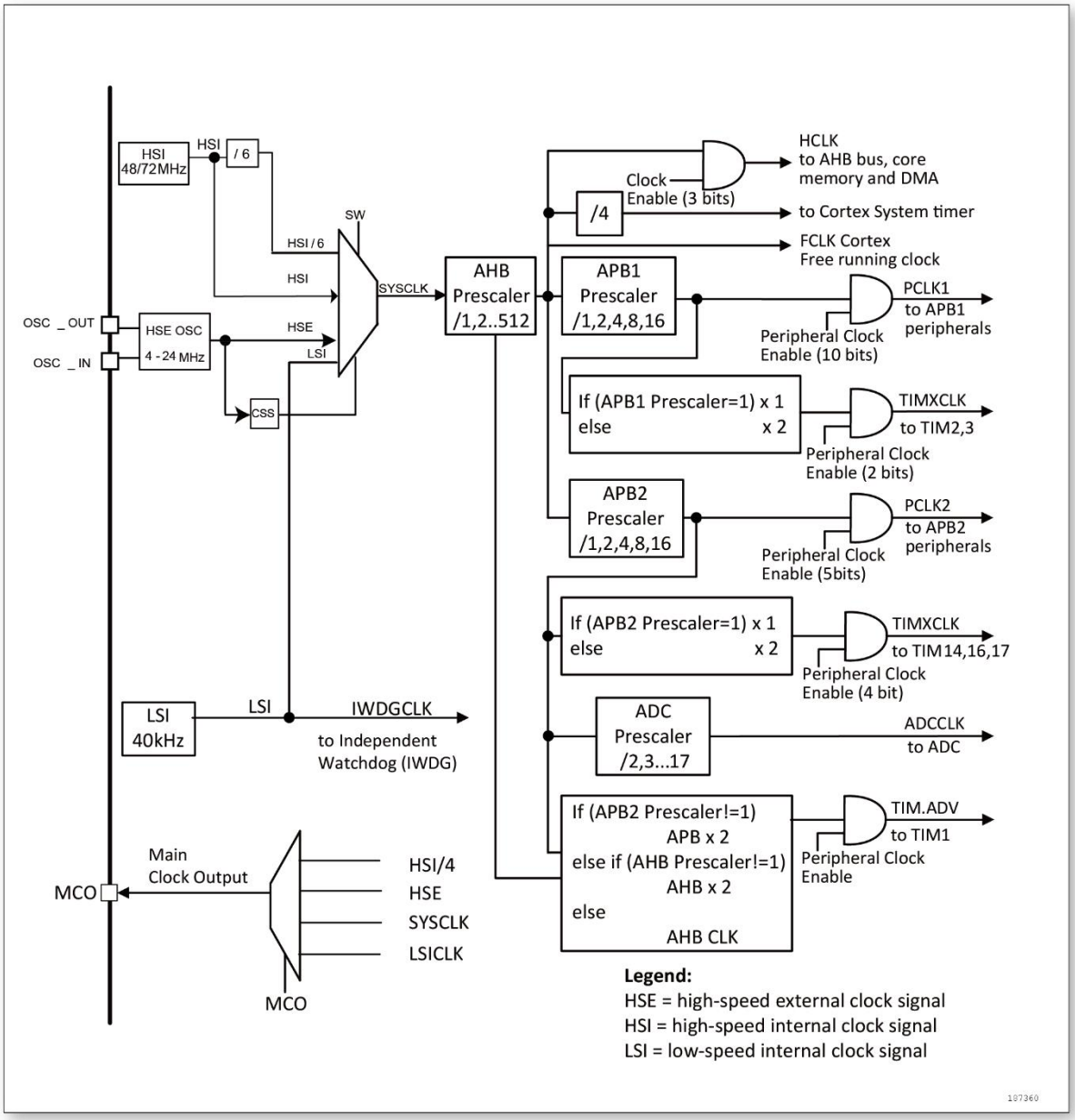

Figure 6 Clock tree

2.2.8 Boot Modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options：

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is stored in the system memory, and can reprogram the flash by UART1

2.2.9 Power Supply Schemes

- V_{DD} = 2.0V ~ 5.5V: external power supply for I/Os and the internal regulator through V_{DD} pins.
- V_{SSA}, V_{DDA}= 2.0V ~ 5.5V： external power supply for reset modules and oscillators. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.

2.2.10 Power Supply Supervisors

This product has integrated poweron reset (POR)/powerdown reset (PDR) circuit. The circuit remains in the working state and ensures proper operation above a threshold of 2.0V. When V_{DD} is below a specified threshold ($V_{POR/PDR}$), the device will be placed in the reset state, without the need for an external reset circuit.

Additionally, the device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, an interrupt can be generated. The interrupt handler will send a warning message or switch the microcontroller to the safe mode. The PVD function should be enabled by a program.

2.2.11 Voltage Regulator

The voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.12 Low Power Mode

The product support low power mode to achieve the best compromise between low power consumption, short startup time and multiple wake up events.

Table 3 Low power mode list

Mode	Entry	Wakeup	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator	Influence on data and registers	Preautions
Sleep Mode	WFI(WaitforInterrupt)	Any arbitrary interrupt	CPU clock off, no influence	Off	On		The peripheral

Mode	Entry	Wakeup	Influence on 1.5V area clock	Influence on V_{DD} area clock	Voltage regulator	Influence on data and registers	Preautions
	WFE(Waitfor Event)	Wake-up event	on other clock and ADC clock				clock still remains and the contents of register and SRAM are kept
Stop Mode	LPDS bit; SLEEPDEEP bit; WFI or WFE;	Any arbitrary interrupt (set in the external interrupt register), IWDG reset wake-up	All 1.5V area clocks are off	HSI and HSE oscillator off	On	The contents of register and SRAM are kept and all peripheral clocks are disabled	GPIOs that are not used before entering low power should set analog input state
Standby Mode	PDDS bit; SLEEPDEEP bit; WFI or WFE;	WKUP pin, NRST pin external reset, IWDG reset			Off	The contents of register and SRAM are kept and all peripheral clocks are disabled. Here, wake-up is equivalent to chip reset	

Sleep mode

In the Sleep mode, only the CPU stops working. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs

Stop mode

The Stop mode minimizes the power consumption while retaining the content of SRAM and registers. The HSI oscillator and HSE crystal oscillator are also shut down in the Stop mode. The microcontroller can be woken up from the Stop mode by any of the EXTI signals. The EXTI signal can be a wake up signal from one of the 16 external I/O ports and the output of the PVD

Standby mode

The Standby mode can minimize the power consumption of the system. In the Standby mode, the voltage regulator turns off when the CPU is in the deep sleep mode. The entire 1.5V power supply domain is disconnected. HSI and HSE oscillators are also turned off. They can be woken up by the rising edge of WKUP

pin, external reset of NRST pin and IWDG reset. They also can be woken up by the watchdog timer without reset. The contents of SRAM and registers will be lost.

2.2.13 HWDIV

The hardware division unit consists of four 32bit data registers, which are dividend, divisor, quotient and remainder, and can be done with signed or unsigned 32bit division. The hardware division control register USIGN can choose whether to have signed division or unsigned division.

Each time the divisor register is written, the division operation is automatically triggered. After the operation is completed, the result is written to the quotient and remainder registers. If the reader register, remainder register, or status register is read before the end, the read operation is suspended until the end of the operation.

If the divisor is zero, an overflow interrupt flag will be generated.

2.2.14 Direct memory access controller (DMA)

The flexible 5 way universal DMA can manage memory to memory, peripheral to memory and memory to peripheral transfers. The DMA controller supports the management of the ring buffer, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, with support for software trigger on each channel. The length, the source address and the destination address of the transfer can be set separately by the software.

The DMA can be used with major peripherals: UART, I2C, SPI, ADC and general-purpose, basic, advanced control timer TIMx.

2.2.15 Timers and watchdogs

The product includes one advanced timer, two generalpurpose timers, three basic timers, two watchdog timers and one SysTick timer.The following table compares the functions of advanced control timer, generalpurpose timer and basic timer:

Table 4 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complem - entary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Interger from 1 ~ 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, down, up/down	Interger from 1 ~ 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Interger from 1 ~ 65536	Yes	4	No

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complem - entary outputs
Basic	TIM14	16-bit	Up	Interger from 1 ~ 65536	Yes	1	No
	TIM16/TIM17	16-bit	Up	Interger from 1 ~ 65536	Yes	1	Yes

Advancedcontrol timer (TIM1)

The advanced control timer is composed of one 16bit counter, four capture/compare channels and one threephase complementary PWM generator. It has complementary PWM outputs with dead time insertion and can be used as a complete generalpurpose timer. Four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center alignment mode)
- Single pulse output

If configured as a 16-bit generalpurpose timer, it has the same features as a TIM2 timer. If configured as a 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In the debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these outputs.

Many features are shared with those of general-purpose TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

Generalpurpose timers (TIMx)

Two synchronizable generalpurpose timers (TIM2, TIM3) are built into the product. The generalpurpose timer has one 16/32-bit autoload up/ down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single pulse mode output.

Generalpurpose timers 32-bit

The generalpurpose timer has one 32-bit autoload up/ down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single pulse mode output

Generalpurpose timers 16-bit

The generalpurpose timer has one 16-bit autoload up/down counter, one 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single pulse mode output.

The generalpurpose timers can work together with the advanced control timer via the Timer Link feature for synchronization or event chaining. Their counters can be

frozen in the debug mode. Any of the generalpurpose timer can be used to produce PWM outputs. Each timer has independent DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1～ 4 Hall sensors. Each timer can produce PWM outputs or be seen as a simple time reference.

Basic timer

TIM14

This timer is based on a 16-bit autoreload upcounter and a 16-bit prescaler. TIM14 features one single channel for input capture/output compare, PWM or one pulse mode output. Its counter can be frozen in debug mode

TIM16/TIM17

Every timer is based on a 16-bit autoreload upcounter and a 16-bit prescaler. They each have a single channel for input capture/output compare, PWM or onepulse mode output. TIM16 and TIM17 have a complementary output with dead time generation and independent DMA request generation. Their counters can be frozen in debug mode.

Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter. It is clocked from an independent 40 KHz internal oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability, and the counter can be frozen in debug mode.

Systick

This timer is dedicated to realtime operating systems，but could also be used as a standard downcounter. It features：

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.16 GPIO

Each GPIO pin can be configured by software as an output (pushpull or opendrain), an input (with or without pull up/pull down), or alternate peripheral function. Most GPIO pins are shared with digital or analog alternate peripherals.

2.2.17 Universal asynchronous receiver/transmitter (UART)

UART provides hardware management of the CTS, RTS. Compatible with ISO7816

smart card mode. The UART interface supports output data lengths of 5 bits, 6 bits, 7 bits, 8 bits, and 9 bits. All UART interface can be served by the DMA controller.

2.2.18 I2C interface

The I2C interface can operate in multimaster or slave modes. It can support Standard mode，and Fast Mode.

It supports 7bit or 10bit addressing modes.

2.2.19 Serial peripheral interface (SPI)

The SPI interface, in slave or master mode, can be configured to 1 ～ 32 bits per frame. The maximum rate is 24M for master mode and 12M for slave mode.

All SPI interfaces can be served by the DMA controller.

2.2.20 Analogtodigital converter (ADC)

The product is embedded with one 12-bit analogtodigital converter (ADC) which has up to 13 external channels and is available for singleshot, onecycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs.

All ADC can be served by the DMA controller.

The analog watchdog function allows to monitor one or all selected channels precisely. An interrupt will occur when the monitored signal exceeds a preset threshold.

Events generated by generalpurpose timers (TIMx) and the advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can synchronize the ADC conversion with the clock.

2.2.21 Hardware Dvision

The hardware division unit consists of four 32bit data registers, which are dividend, divisor, quotient and remainder, and can be done with signed or unsigned 32bit division. The hardware division control register USIGN can choose whether to have signed division or unsigned division.

Each time the divisor register is written, the division operation is automatically triggered. After the operation is completed, the result is written to the quotient and remainder registers. If the reader register, remainder register, or status register is read before the end, the read operation is suspended until the end of the operation.

If the divisor is zero, an overflow interrupt flag will be generated.

2.2.22 Comparator (COMP)

The product has one builtin comparator which can be used independently (suitable for I/Os on all terminals) or in combination with the timer. It can also be used for a variety of functions, including:

- Trigger wake up events in the lowpower mode by analog signals
- Adjust the analog signal
- Combine with PWM outputs from timers to form a cyclebycycle current control loop

- Railtorail comparator
- Each comparator has an optional threshold
  - Alternate I/O pins
  - The internal comparison voltage CRV can be AVDD or the partial voltage value of the internal reference voltage
- Programmable hysteresis voltage
- Programmable rate and power consumption
- The output terminal can be redirected to an I/O port or multiple timer input terminals to trigger the following events:
  - Capture event
  - OCref_clr event (cyclebycycle current control)
  - Brake event to shut off PWM rapidly

2.2.23 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel to convert the sensor output to a digital value.

2.2.24 Serial wire debug port (SWDP)

Two-wire serial debug port (SWDP) is embedded in the Arm.

An Arm SWDP allows to be connected to a singlechip microcomputer through serial wire debugging tools.

3 Pin Definition and Alternate Function

3.1 Pinout Diagram

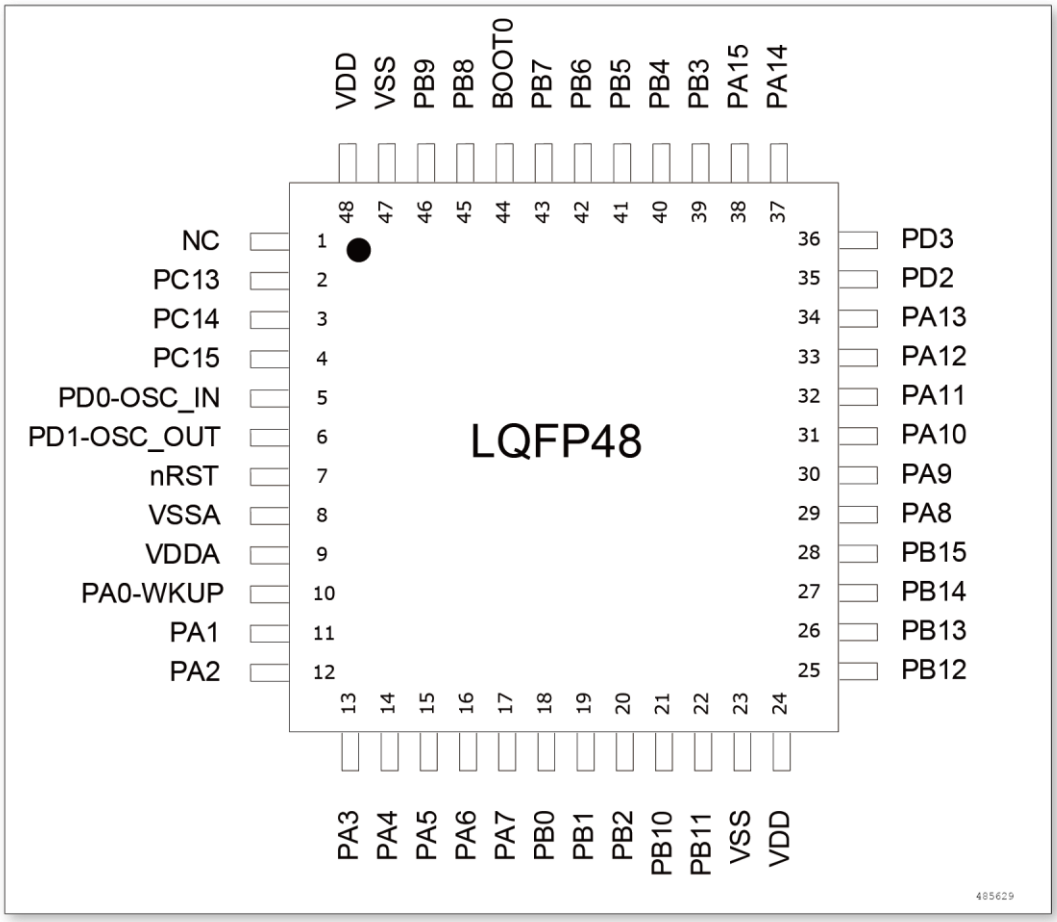

Figure7 LQFP48 pinout diagram

Pin definition and Alternate Function

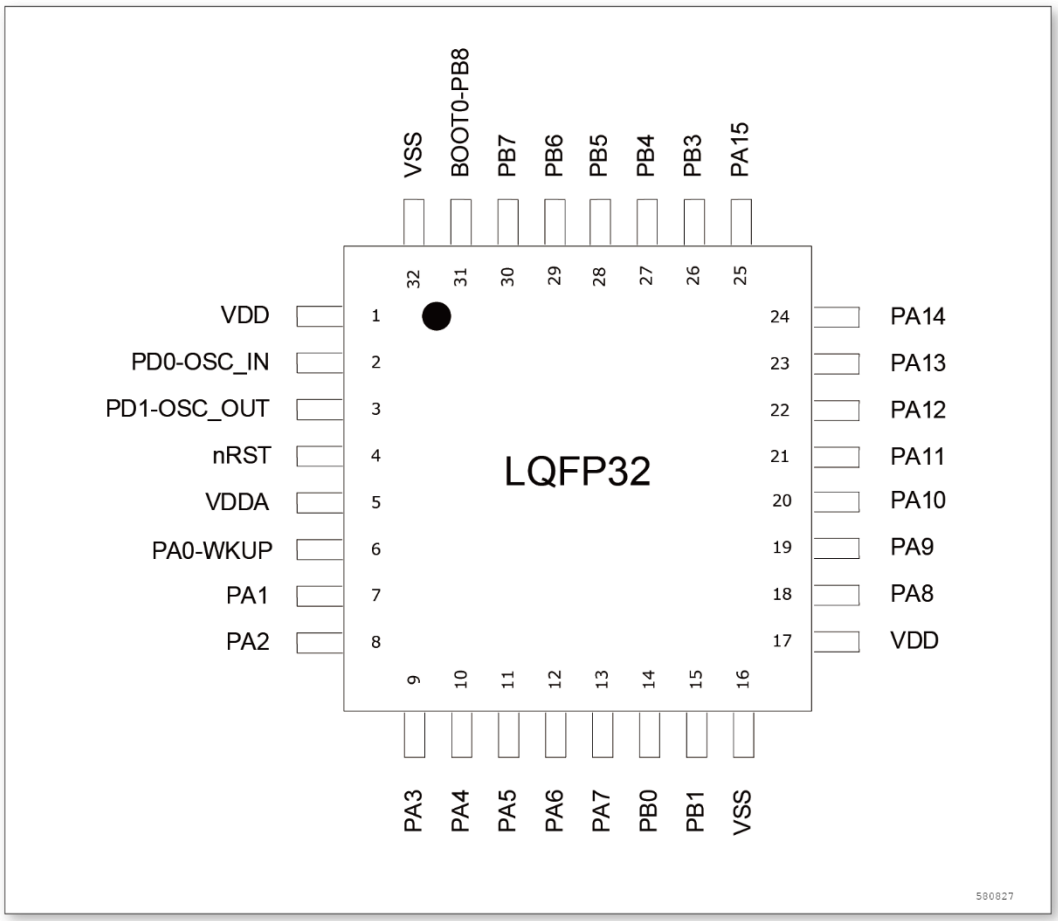

Figure8 LQFP32 pinout diagram

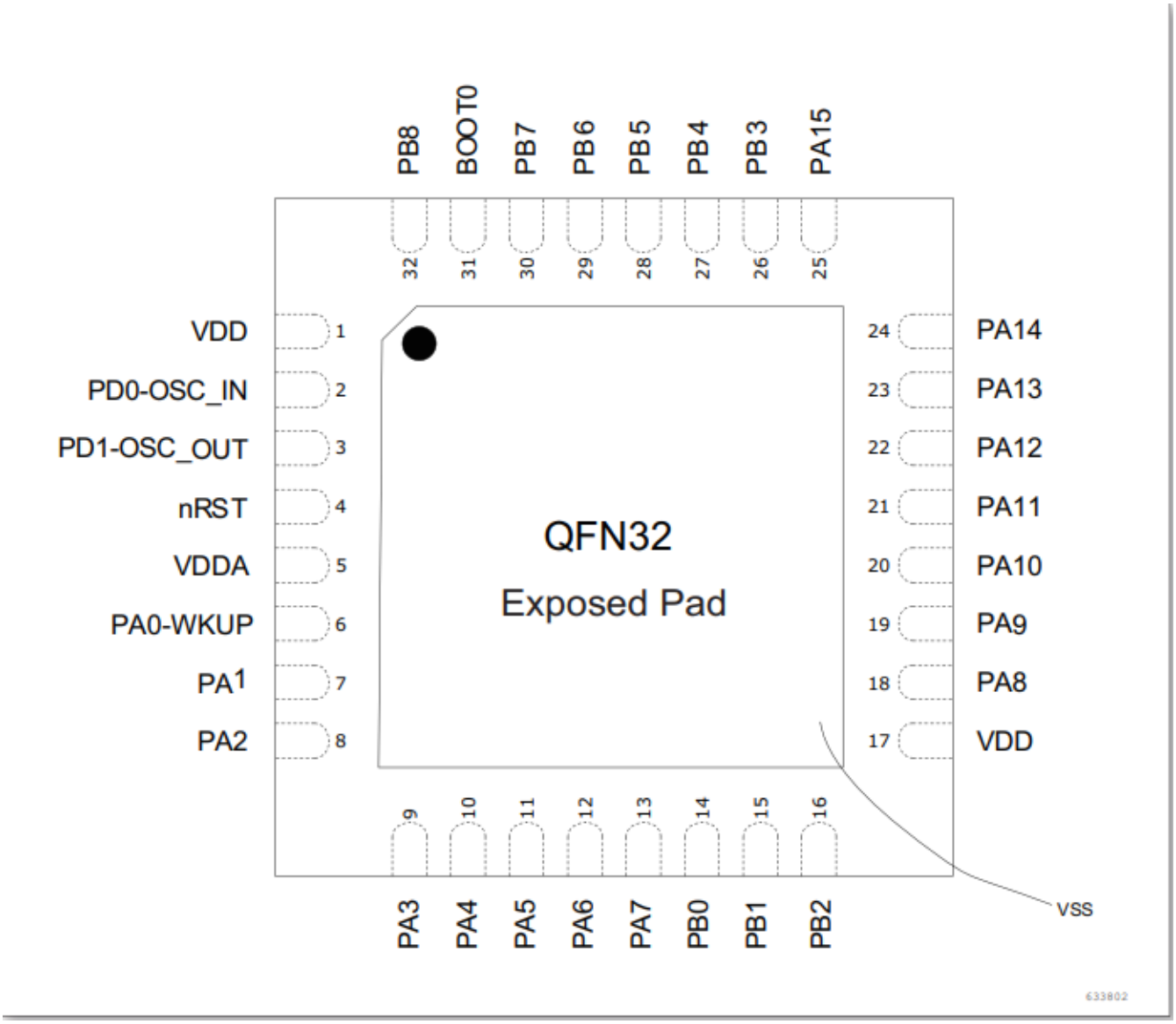

Figure 9 QFN32 pinout diagram

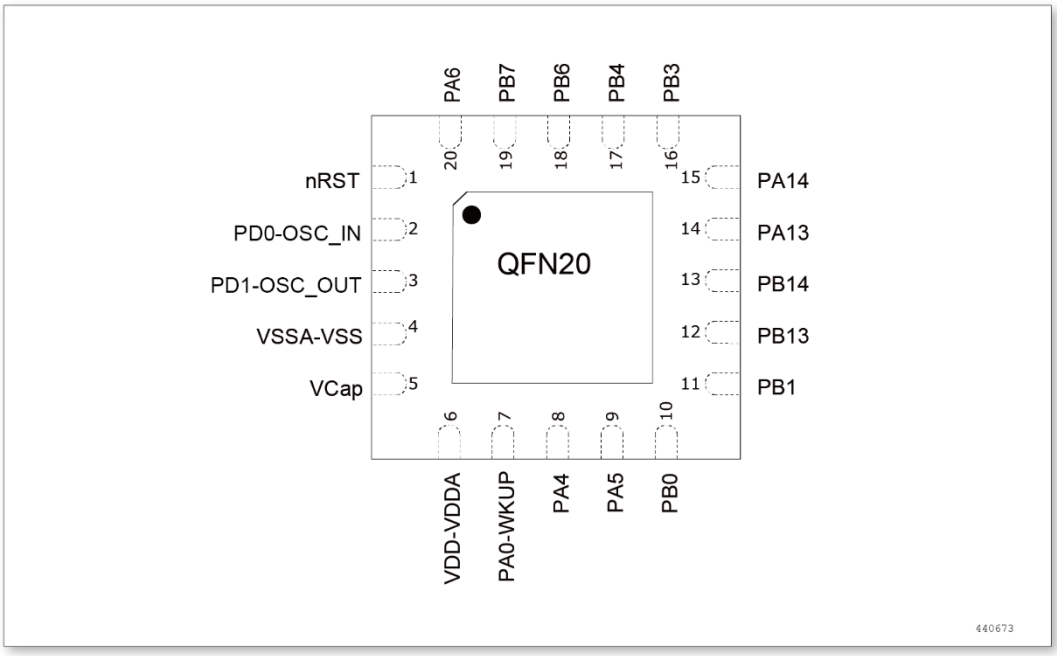

Figure 10 QFN20 pinout diagram

Pin definition and Alternate Function

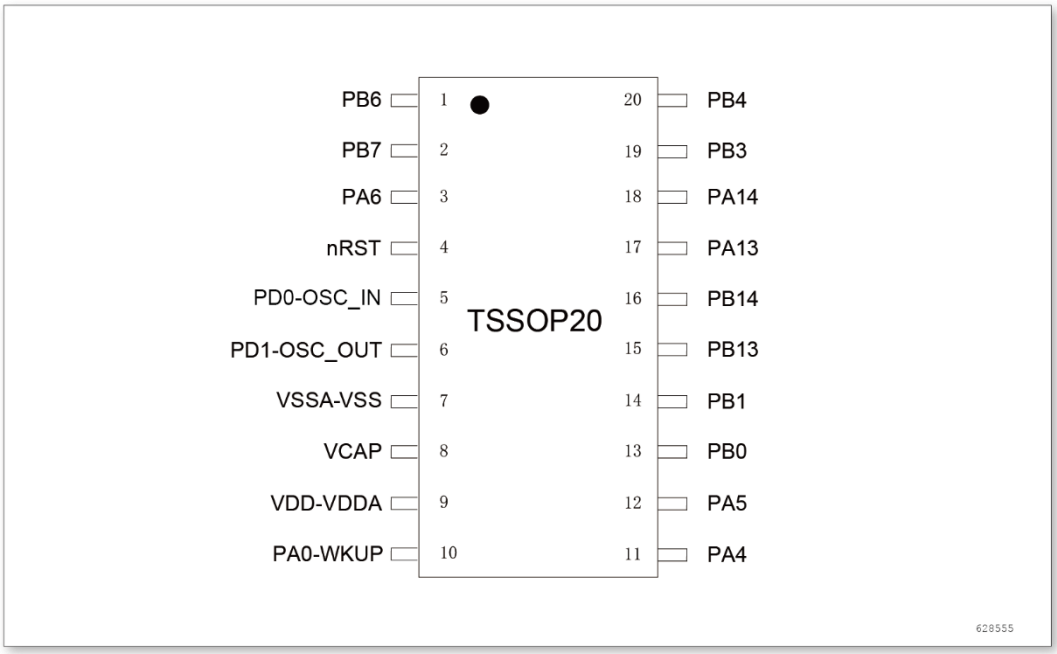

Figure 11 TSSOP20 pinout diagram

Annotate: VCap should be setted to float or connect to ground with 0.1uF-0.01uF capacitor.

3.2 Pin Assignment Table

Table 5 Pin assignment table

Pin number					Pin name	Type (1)	I/Olevel (2)	Main Function	Alternate functions	Additional functions
LQFP48	LQFP32	QFN32	TSSOP20	QFN20						
1	-	-	-	-	NC	S	-	NC		
2	-	-	-	-	PC13	I/O	FT	PC13	TIM2_CH1	-
3	-	-	-	-	PC14	I/O	FT	PC14	TIM2_CH2	-
4	-	-	-	-	PC15	I/O	FT	PC15	TIM2_CH3	
5	2	2	5	2	PD0 OSC_IN	I/O	FT	PD0	I2C1_SDA	-
6	3	3	6	3	PD1 OSC_OUT	I/O	FT	PD1	I2C1_SCL	-
7	4	4	4	1	NRST	I/O	FT	NRST	-	-
8	-	-	-	4	VSSA	S	-	VSSA	-	-
9	5	5	9	6	VDDA/VDD	S	-	VDDA	-	-
10	6	6	10	7	PA0 WKUP	I/O	TC	PA0	UART2_CTS/ TIM2_CH1_ETR/ SPI2_NSS/ TIM2_CH3/ COMP1_OUT	ADC1_VIN[0]
11	7	7	-	-	PA1	I/O	TC	PA1	UART2_RTS/ TIM2_CH2	ADC1_VIN[1]/ COMP1_INP[0]
12	8	8	-	-	PA2	I/O	TC	PA2	UART2_TX/ TIM2_CH3/ SPI2_NSS	ADC1_VIN[2]/ COMP1_INP[1]
13	9	9	-	-	PA3	I/O	TC	PA3	UART2_RX/ TIM2_CH4	ADC1_VIN[3]/ COMP1_INP[2]
14	10	10	11	8	PA4	I/O	TC	PA4	SPI1_NSS/ TIM1_BKIN/ TIM14_CH1/ I2C1_SDA	ADC1_VIN[4]/ COMP1_INP[3]
15	11	11	12	9	PA5	I/O	TC	PA5	SPI1_SCK/ TIM2_CH1_ETR/ TIM1_ETR/ I2C1_SCL/ TIM1_CH3N	ADC1_VIN[5]/ COMP1_INM[0]
16	12	12	3	20	PA6	I/O	TC	PA6	SPI1_MISO/ TIM3_CH1/ TIM1_BKIN/ UART2_RX/ TIM1_ETR/ TIM16_CH1/ TIM1_CH3/ COMP1_OUT	ADC1_VIN[6]/ COMP1_INM[1]
17	13	13	-	-	PA7	I/O	TC	PA7	SPI1_MOSI/ TIM3_CH2/ TIM1_CH1N/ TIM14_CH1/ TIM17_CH1/ TIM1_CH2N/ TIM1_CH3N	ADC1_VIN[7]/ COMP1_INM[2]
18	14	14	13	10	PB0	I/O	TC	PB0	TIM3_CH3/ TIM1_CH2N/ TIM1_CH1N/ TIM1_CH3	ADC1_VIN[8]
19	15	15	14	11	PB1	I/O	TC	PB1	TIM14_CH1/ TIM3_CH4/ TIM1_CH3N/ TIM1_CH4/ TIM1_CH2N/ MCO/ TIM1_CH2/ TIM1_CH1N	ADC1_VIN[9]
20	-	16	-	-	PB2	I/O	FT	PB2	-	-
21	-	-	-	-	PB10	I/O	FT	PB10	I2C1_SCL/ TIM2_CH3/ SPI2_SCK	-

Pin definition and Alternate Function

Pin number					Pin name	Type (1)	I/Olevel (2)	Main Function	Alternate functions	Additional functions
LQFP48	LQFP32	QFN32	TSSOP20	QFN20						
22	-	-	-	-	PB11	I/O	FT	PB11	I2C1_SDA/ TIM2_CH4	-
23	16	-	7	4	VSS	S	-	VSS	-	-
24	17	17	9	6	VDD	S	-	VDD	-	-
25	-	-	-	-	PB12	I/O	FT	PB12	SPI2_NSS/ SPI2_SCK/ TIM1_BKIN/ SPI2_MOSI/ SPI2_MISO	-
26	-	-	15	12	PB13	I/O	FT	PB13	SPI2_SCK/ SPI2_MISO/ TIM1_CH1N/ SPI2_NSS/ SPI2_MOSI/ I2C1_SCL/ TIM1_CH3N/ TIM2_CH1	-
27	-	-	16	13	PB14	I/O	FT	PB14	SPI2_MISO/ SPI2_MOSI/ TIM1_CH2N/ SPI2_SCK/ SPI2_NSS/ I2C1_SDA/ TIM1_CH3/ TIM1_CH1	-
28	-	-	-	-	PB15	I/O	FT	PB15	SPI2_MOSI/ SPI2_NSS/ TIM1_CH3N/ SPI2_MISO/ SPI2_SCK/ TIM1_CH2N/ TIM1_CH2	-
29	18	18	-	-	PA8	I/O	FT	PA8	MCO/ TIM1_CH1/ TIM1_CH2/ TIM1_CH3	-
30	19	19	-	-	PA9	I/O	FT	PA9	UART1_TX/ TIM1_CH2/ UART1_RX/ I2C1_SCL/ MCO/ TIM1_CH1N/ TIM1_CH4	-
31	20	20	-	-	PA10	I/O	FT	PA10	TIM17_BKIN/ UART1_RX/ TIM1_CH3/ UART1_TX/ I2C1_SDA/ TIM1_CH1/ SPI2_SCK	-
32	21	21	-	-	PA11	I/O	FT	PA11	UART1_CTS/ SPI2_MOSI/ TIM1_CH4/ I2C1_SCL/ COMP1_OUT	-
33	22	22	-	-	PA12	I/O	FT	PA12	UART1_RTS/ TIM1_ETR/ SPI2_MISO/ I2C1_SDA/ TIM1_CH2	-
34	23	23	17	14	PA13	I/O	FT	PA13	SWDIO/ SPI2_MISO/ MCO/ TIM1_CH2/ TIM1_BKIN	-
35	-	-	-	-	PD2	I/O	FT	PD2	-	-

Pin definition and Alternate Function

Pin number					Pin name	Type (1)	I/Olevel (2)	Main Function	Alternate functions	Additional functions
LQFP48	LQFP32	QFN32	TSSOP20	QFN20						
36	-	-	-	-	PD3	I/O	FT	PD3	-	-
37	24	24	18	15	PA14	I/O	FT	PA14	SWDCLK/ UART2_TX/ SPI1_NSS	-
38	25	25	-	-	PA15	I/O	FT	PA15	SPI1_NSS/ UART2_RX/ TIM2_CH1_ETR	-
39	26	26	19	16	PB3	I/O	TC	PB3	SPI1_SCK/ TIM2_CH2/ UART1_TX/ TIM2_CH3/ TIM1_CH1/ TIM2_CH1	ADC1_VIN[10]
40	27	27	20	17	PB4	I/O	TC	PB4	SPI1_MISO/ TIM3_CH1/ UART1_RX/ TIM17_BKIN/ TIM1_CH2/ TIM2_CH2	ADC1_VIN[11]
41	28	28	-	-	PB5	I/O	FT	PB5	SPI1_MOSI/ TIM3_CH2/ TIM16_BKIN/ MCO/ TIM1_CH3/ TIM2_CH3	-
42	29	29	1	18	PB6	I/O	FT	PB6	UART1_TX/ I2C1_SCL/ TIM16_CH1N/ TIM2_CH1	-
43	30	30	2	19	PB7	I/O	TC	PB7	UART1_RX/ I2C1_SDA/ TIM17_CH1N/ UART2_TX	ADC1_VIN[12]
44	31	31	-	-	BOOT0	I/O	FT	BOOT0	-	-
45	31	32	-	-	PB8	I/O	FT	PB8	I2C1_SCL/ TIM16_CH1/ UART2_RX	-
46	-	-	-	-	PB9	I/O	FT	PB9	I2C1_SDA/ TIM17_CH1/ TIM1_CH4/ SPI2_NSS	-
47	32	-	-	4	VSS	S	-	VSS	-	-
48	1	1	-	6	VDD	S	-	VDD	-	-
-	-	-	8	5	VCap	S	-	1.5V regulator capacitor	-	-

1. I = input, O = output, S = power pins, HiZ = high resistance
2. TC: standard IO, input signal level should not exceed V_{DD}
3. Only exist in QFN20 and TSSOP package types.

3.3 Multiplex Function Table

Table 6 Multiplex function for PA port: AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1_ETR	SPI2_NSS	TIM2_CH3	-	-	COMP1_OUT
PA1	-	UART2_RTS	TIM2_CH2	-	-	-	-	-
PA2	-	UART2_TX	TIM2_CH3	SPI2_NSS	-	-	-	-
PA3	-	UART2_RX	TIM2_CH4	-	-	-	-	-
PA4	SPI1_NSS	-	-	TIM1_BKIN	TIM14_CH1	I2C1_SDA	-	-
PA5	SPI1_SCK	-	TIM2_CH1_ETR	TIM1_ETR	-	I2C1_SCL	TIM1_CH3N	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	UART2_RX	TIM1_ETR	TIM16_CH1	TIM1_CH3	COMP1_OUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	TIM1_CH2N	TIM1_CH3N
PA8	MCO	-	TIM1_CH1	-	-	-	TIM1_CH2	TIM1_CH3
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	TIM1_CH1N	TIM1_CH4
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	-	TIM1_CH1	SPI2_SCK
PA11	-	UART1_CTS	TIM1_CH4	-	SPI2_MOSI	I2C1_SCL	-	COMP1_OUT
PA12	-	UART1_RTS	TIM1_ETR	-	SPI2_MISO	I2C1_SDA	-	TIM1_CH2
PA13	SWDIO	-	-	-	SPI2_MISO	MCO	TIM1_CH2	TIM1_BKIN
PA14	SWDCLK	UART2_TX	-	SPI1_NSS	-	-	-	-
PA15	SPI1_NSS	UART2_RX	TIM2_CH1_ETR	-	-	-	-	-

Pin definition and Alternate Function

Table 7 Multiplex function for PB port: AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH4	TIM1_CH2N	MCO	TIM1_CH2	TIM1_CH1N
PB2	-	-	-	-	-	-	-	-
PB3	SPI1_SCK	-	TIM2_CH2	UART1_TX	TIM2_CH3	-	TIM1_CH1	TIM2_CH1
PB4	SPI1_MISO	TIM3_CH1	-	UART1_RX	-	TIM17_BKIN	TIM1_CH2	TIM2_CH2
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	MCO	-	-	TIM1_CH3	TIM2_CH3
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	TIM2_CH1	-	-	-
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	UART2_TX	-	-	-
PB8	-	I2C1_SCL	TIM16_CH1	-	UART2_RX	-	-	-
PB9	-	I2C1_SDA	TIM17_CH1	-	TIM1_CH4	SPI2_NSS	-	-
PB10	-	I2C1_SCL	TIM2_CH3	-	-	SPI2_SCK	-	-
PB11	-	I2C1_SDA	TIM2_CH4		-	-	-	-
PB12	SPI2_NSS	SPI2_SCK	TIM1_BKIN	SPI2_MOSI	SPI2_MISO	-	-	-
PB13	SPI2_SCK	SPI2_MISO	TIM1_CH1N	SPI2_NSS	SPI2_MOSI	I2C1_SCL	TIM1_CH3N	TIM2_CH1
PB14	SPI2_MISO	SPI2_MOSI	TIM1_CH2N	SPI2_SCK	SPI2_NSS	I2C1_SDA	TIM1_CH3	TIM1_CH1
PB15	SPI2_MOSI	SPI2_NSS	TIM1_CH3N	SPI2_MISO	SPI2_SCK	-	TIM1_CH2N	TIM1_CH2

Table 8 Multiplex function for PC port: AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC13	-	-	-	-	-	-	TIM2_CH1	-
PC14	-	-	-	-	-	-	TIM2_CH2	-
PC15	-	-	-	-	-	-	TIM2_CH3	-

Table 9 Multiplex function for PD port: AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	I2C1_SDA	-	-	-	-	-	-
PD1	-	I2C1_SCL	-	-	-	-	-	-

4 Electrical Characteristics

4.1 Test Condition

Unless otherwise specified, all voltages are referenced to V_{SS}

4.1.1 Loading Capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.

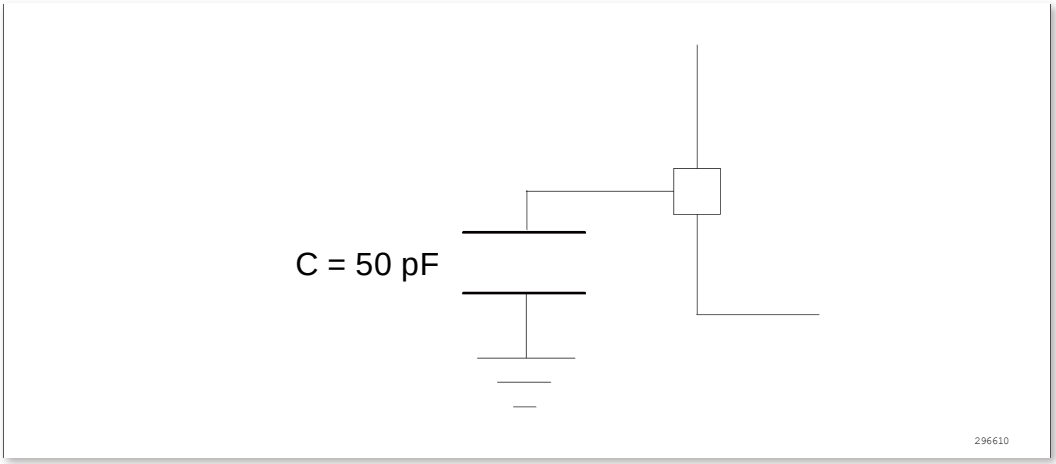

Figure 12 Pin loading conditions

4.1.2 Pin input voltage

The input voltage measurement on a pin of the device is described in the figure below.

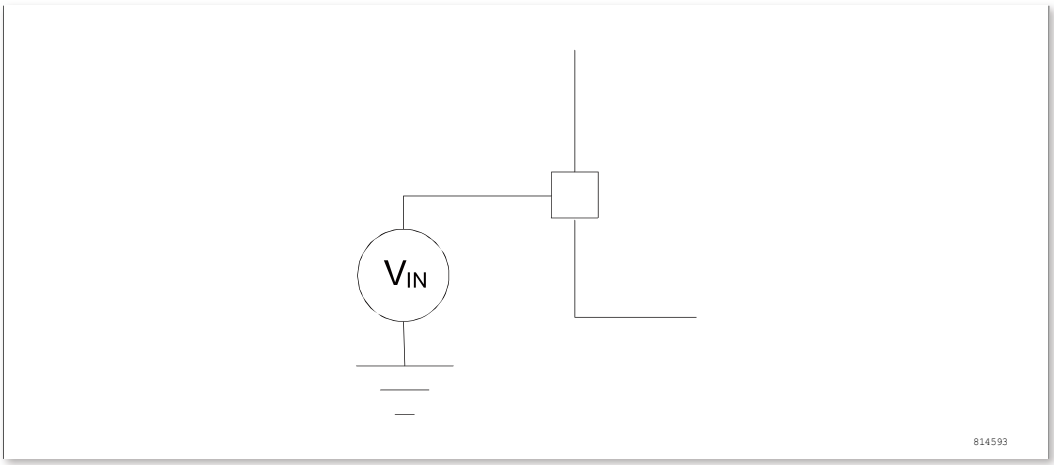

Figure13 Pin input voltage

4.1.3 Power Supply Scheme

The power supply scheme is shown in the figure below.

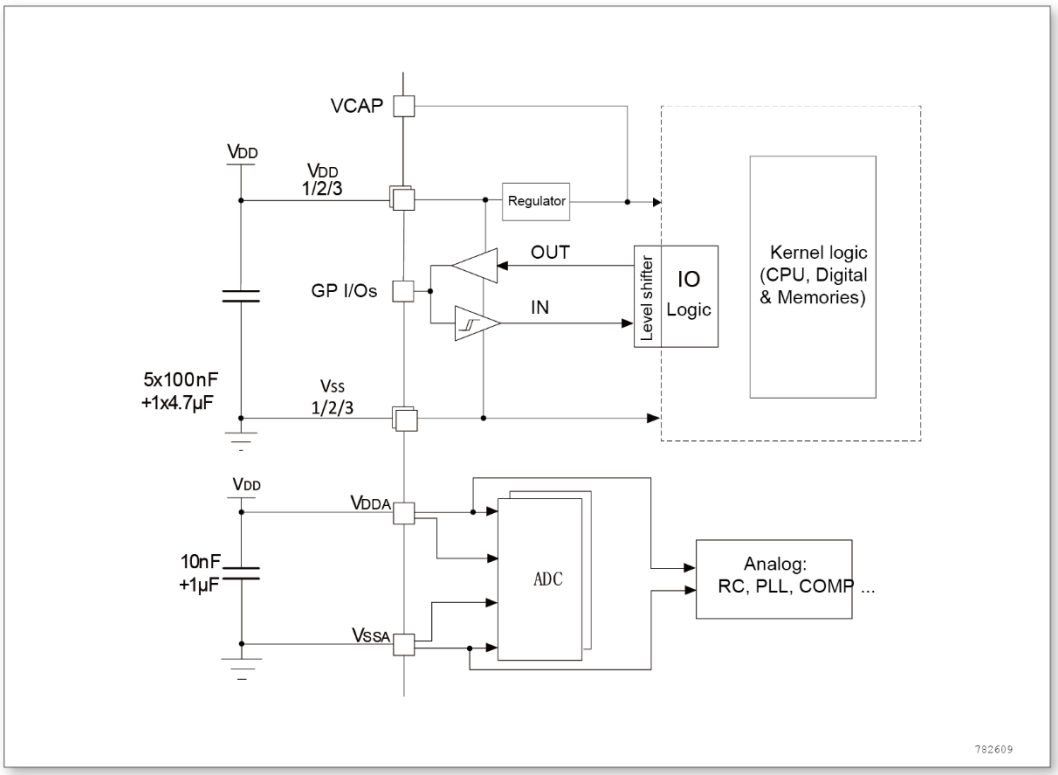

Figure 14 Power supply scheme

4.1.4 Current Consumption Measurement

The current consumption measurement on a pin is shown in the figure below.

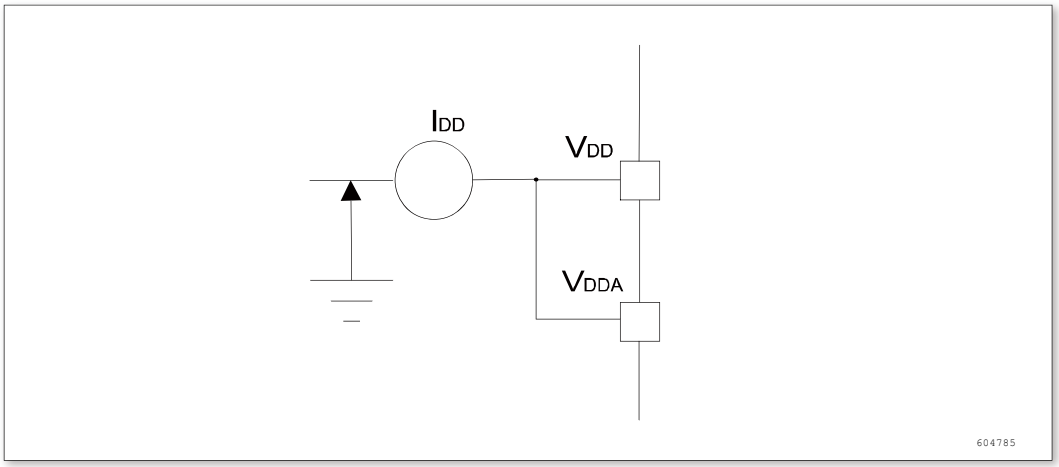

Figure 15 Current consumption measurement scheme

4.2 Absolute Maximum Ratings

Stresses above “the absolute maximum ratings” listed in (Table 10 and Table 11) may cause permanent damage to the device. These are stress maximum ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DDx}-V_{SSx}	External main supply voltage (including V_{DDA} and V_{SSA}) (1)	-0.3	5.8	V
V_{IN}(2)	Input voltage on the 5 Vtolerant pin	VSS-0.3	5.8	
	Input voltage on other pins	VSS-0.3	V_{DD}+0.3	
|△ V_{DDx}|	Voltage variations between different		50	mV

Symbol	Description	Min	Max	Unit
	power pins			
|Vssx-Vss|	Voltage variations between different ground pins		50	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to the table below for the maximum allowed injected current values.

Table 11 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (supply current) (1)	+120	mA
I_{VSS}	Total current out of V_{SS} wire (outflow current) (1)	-120	
I_{IO}	Output sink current on any I/O and control pins	+20	
	Output current on any I/O and control pins	-18	
$I_{INJ(PIN)}$ (2)(3)	Injection current on NRST pin	±5	
	Injection current on OSC_IN pin of HSE and OSC_IN pin LSE	±5	
	injection current on other pins (4)	±5	
$\sum I_{INJ(PIN)}$ (4)	Total injection current on all I/O and control pins (4)	±25	

3. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply within the permissible range
4. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sunk/pulled between two consecutive power pins that refer to LQFP package with dense pins.
5. The reverse injection current can interfere with the analog performance of the device.
6. A positive injection current is induced by VIN > VDDA while a negative injection current is induced by VIN < VSS. IINJ(PIN) must never be exceeded.
7. When several inputs are submitted to a current injection, the maximum ΣIINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 12 General operating conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	-	72	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	f_{HCLK}	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	f_{HCLK}	
V_{DD}	Digital operating voltage	-	2.0	-	5.5	V
V_{DDA}	Analog operating voltage (ADC used)	Must be the same voltage as V_{DD}	2.5	-	5.5	V
	Analog operating voltage (ADC not used)		2.0	-	2.5	
P_D	TA=85℃(industrial) or TA=105℃ (extended industrial) power dissipation)	QFN20	-	-	266	mW
		TSSOP20	-	-	-	
T_A	Ambient temperature	-	-40	-	105	℃
T_J	Junction temperature range (3)	-	-40	-	125	℃

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during powerup and operation.。

4.3.2 Thermal characteristics

The maximum junction temperature of the chip must not exceed the value given in the ”General operating conditions”.

The maximum junction temperature is calculated as follows:

$T_j max = T_A max + P_D max \times \theta_{JA}$

$T_A max$：Maximum ambient temperature；

$P_D max$：Total chip power consumption, including the sum of internal and IO power consumption.

Table 13 Package thermal characteristics

Symbol	Description	数值	单位
θ_{JA}	QFN20 Thermal resistance from junction temperature to ambient temperature	75	℃/W
	TSSOP20 Thermal resistance from junction temperature to ambient temperature	-	

4.3.3 Operating conditions at powerup/powerdown

The parameters given in the table below are based on tests under normal operating conditions.

Table14 Operating conditions at powerup/powerdown

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
t_{DD}	V_{DD} rise time rate	T_A = 25℃	300	-	∞	Us/V
	V_{DD} fall time rate		300	-	∞	

1. All powerups need to start at 0V, to ensure that the chip can be powered up reliably

4.3.4 Embedded reset and power control block characteristics

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 12.

Table 15 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000（Rising edge）	-	1.82	-	V
		PLS[3:0]=0000（Falling edge）	-	1.71	-	
		PLS[3:0]=0001（Rising edge）	-	2.12	-	
		PLS[3:0]=0001（Falling edge）	-	2.00	-	
		PLS[3:0]=0010（Rising edge）	-	2.41	-	
		PLS[3:0]=0010（Falling edge）	-	2.30	-	
		PLS[3:0]=0011（Rising edge）	-	2.71	-	
		PLS[3:0]=0011（Falling edge）	-	2.60	-	
		PLS[3:0]=0100（Rising edge）	-	3.01	-	
		PLS[3:0]=0100（Falling edge）	-	2.90	-	
		PLS[3:0]=0101（Rising edge）	-	3.31	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		PLS[3:0]=0101（Falling edge）	-	3.19	-	
		PLS[3:0]=0110（Rising edge）	-	3.61	-	
		PLS[3:0]=0110（Falling edge）	-	3.49	-	
		PLS[3:0]=0111（Rising edge）	-	3.91	-	
		PLS[3:0]=0111（Falling edge）	-	3.79	-	
		PLS[3:0]=1000（Rising edge）	-	4.21	-	
		PLS[3:0]=1000（Falling edge）	-	4.09	-	
		PLS[3:0]=1001（Rising edge）	-	4.51	-	
		PLS[3:0]=1001（Falling edge）	-	4.39	-	
		PLS[3:0]=1010（Rising edge）	-	4.81	-	
		PLS[3:0]=1010（Falling edge）	-	4.69	-	
$V_{POR/PDR}$	Power on/down reset threshold	-	-	1.66	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	110	-	mV
$T_{RSTTEMPO}$(2)	Reset duration	-	-	0.61	-	ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: The reset duration is measured from poweron (POR reset) to the time when the user application code reads the first instruction.

4.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Runmode current consumption measurements given in this section are performed with a reduced code.

Current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level — V_{DD} or V_{SS} (no load).
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted to the fHCLK (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHz is 2 waiting periods).
- The instruction prefetching function is on. When the peripherals are enabled：$f_{HCLK}=f_{PCLK1}=f_{PCLK2}$。

Note：The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the following tables are derived from tests performed

under ambient temperature and V_{DD} supply voltage conditions summarized in Table 12。

Table 16 Typical current consumption in Run mode, code executing from Flash

Symbol	Parameter	Conditions	f_{HCLK}(HZ)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in Run mode	Internal clock	72M	13.99	14.40	14.76	14.84	8.02	8.32	8.60	8.66	mA
			48M	10.23	10.55	10.81	10.91	6.27	6.51	6.73	6.81	
			8M	3.08	3.25	3.43	3.49	2.45	2.59	2.77	2.86	

Table 17 Typical current consumption in sleep mode, code executing from Flash

Symbol	Parameter	Conditions	f_{HCLK}(HZ)	Typical value All peripherals enabled				Typical value All peripherals disabled				Unit
				-40℃	25℃	85℃	105℃	-40℃	25℃	85℃	105℃	
I_{DD}	Supply current in Sleep mode	Internal clock	72M	9.81	10.08	10.33	10.39	3.83	3.98	4.15	4.20	mA
			48M	6.87	7.09	7.30	7.36	2.89	3.03	3.18	3.24	
			8M	2.10	2.21	2.35	2.40	1.44	1.55	1.69	1.74	

1. When the HCLK frequency is less than 8MHz, the system clock is HSI 8M, and the AHB clock is obtained by dividing the frequency

Table 18 Typical and maximum current consumption in stop and standby modes (1)

Symbol	Parameter	Conditions	Typical T_A=25℃	Unit
I_{DDx}	Supply current in Stop mode	Enter the stop mode after reset	6	μA
	Supply current in Standby mode	Enter the standby mode after reset	0.4	

1. Data based on characterization results, not tested in production.The IO state is an analog input.

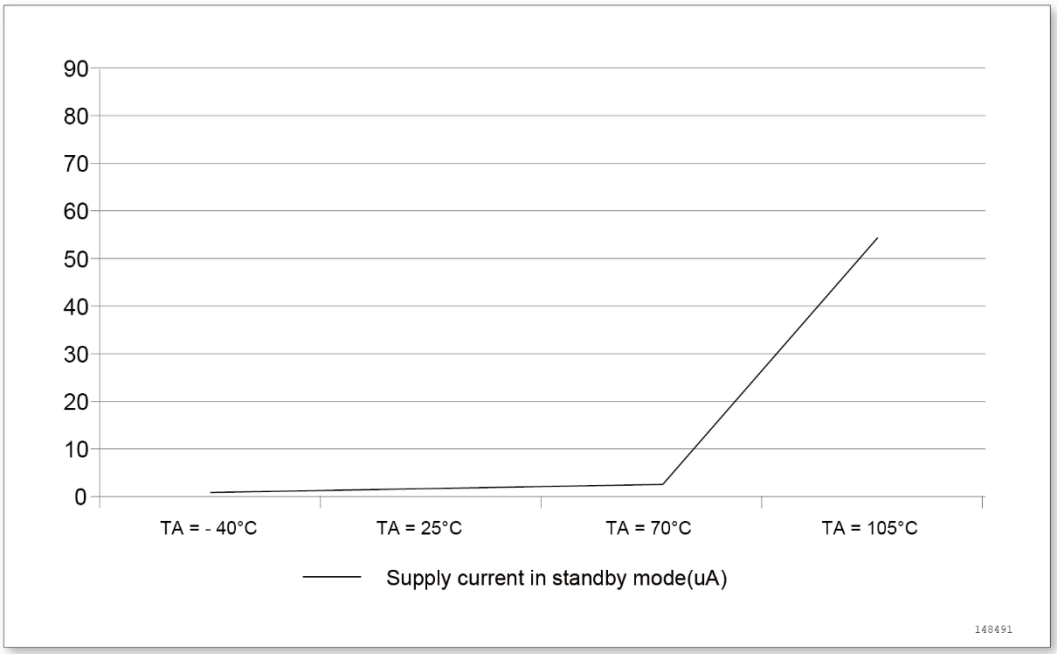

Figure 16 Typical current consumption in standby mode vs. temperature at V_{DD} = 3.3V

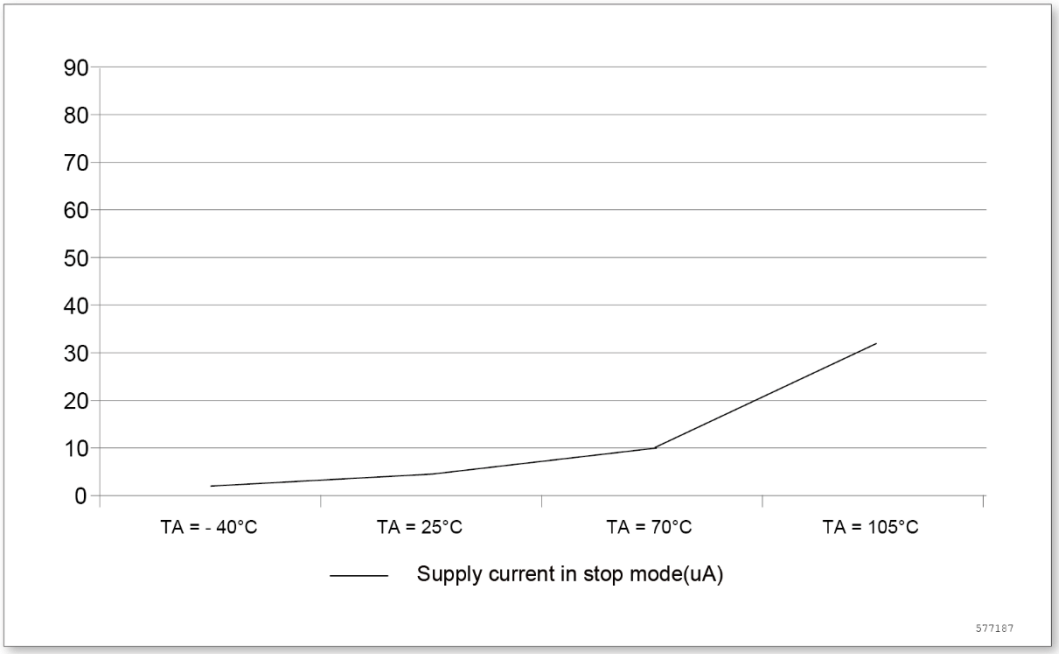

Figure 17 Typical current consumption in stop mode vs. temperature at V_{DD} = 3.3V

Built-in peripheral current consumption

The current consumption of the built-in peripherals is given in Table 19. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level — V_{DD} or V_{SS} (no load).
- All peripherals are disabled except when explicitly mentioned.
- The given value is calculated by measuring the current consumption.
- With all peripherals clocked OFF
- With only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions V_{DD} summarized in Table 12.

Table 19 Built-in peripheral current consumption (1)

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	GPIOD	AHB	0.75	uA/MHz
	GPIOC		0.58	
	GPIOB		0.71	
	GPIOA		0.71	
	CRC		1.00	
	HWDIV		2.17	
	DMA		4.38	
	PWM	APB2	1.75	
	TIM17		3.29	
	TIM16		3.17	
	TIM14		3.17	
	COMP		0.58	
	SPI		7.92	
	TIM1		17.04	
	ADC		1.54	
	SYSCFG		0.37	
	UART1		5.38	
	PWR	APB1	0.79	
	I2C		9.58	
	WWDG		5.96	
	TIM3		8.83	
	TIM2		0.50	
	UART2		5.96	

1. f_{HCLK}=72MHz，$f_{APB1}=f_{HCLK}/2$，$f_{APB2}=f_{HCLK}$，the prescaler coefficient of each peripheral is the default value.

Wake-up Time from Low-power Mode

- The wake-up times given in the following tables are measured in the wake-up phase of the internal clock HSI. The used clock source for wake-up is determined according to the present operation mode:
- Stop or Standby mode: Clock source is the oscillator
- Sleep mode: The clock source is the one used in the Sleep mode and the time is measured under the ambient temperature and supply voltage conforming to the general operating conditions in Table 12.

Table 20 Low-power mode wake-up time

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode	The system clock is HSI	4.2	μS
t_{WUSTOP}	Wake-up from Stop mode	HSI clock wakeup < 2μS	12	μS
$t_{WUSTDBY}$	Wake-up from Standby mode	HSI clock wakeup < 2μS The regulator wakes up from the off mode < 38μS	230	μS

4.3.6 External clock source characteristics

High-speed external user clock generated from an external oscillator source

The parameters of characteristics given in the following table are measured by a high-speed external clock source, and the ambient temperature and supply voltage conform to the general operating conditions

Table 21 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{HSE_ext}	User external clock frequency (1)	-	2	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7VDD	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low	-	V_{SS}	-	$0.3V_{DD}$	V

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
	level voltage					
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	16	-	-	ns
$t_{r(HSE)}$	OSC_IN rise time				20	ns
$T_{f(HSE)}$	OSC_IN fall time				20	ns
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN input leakage current	VSS ≤ VIN ≤ VDD			±1	μA

1. Guaranteed by design, not tested in production.

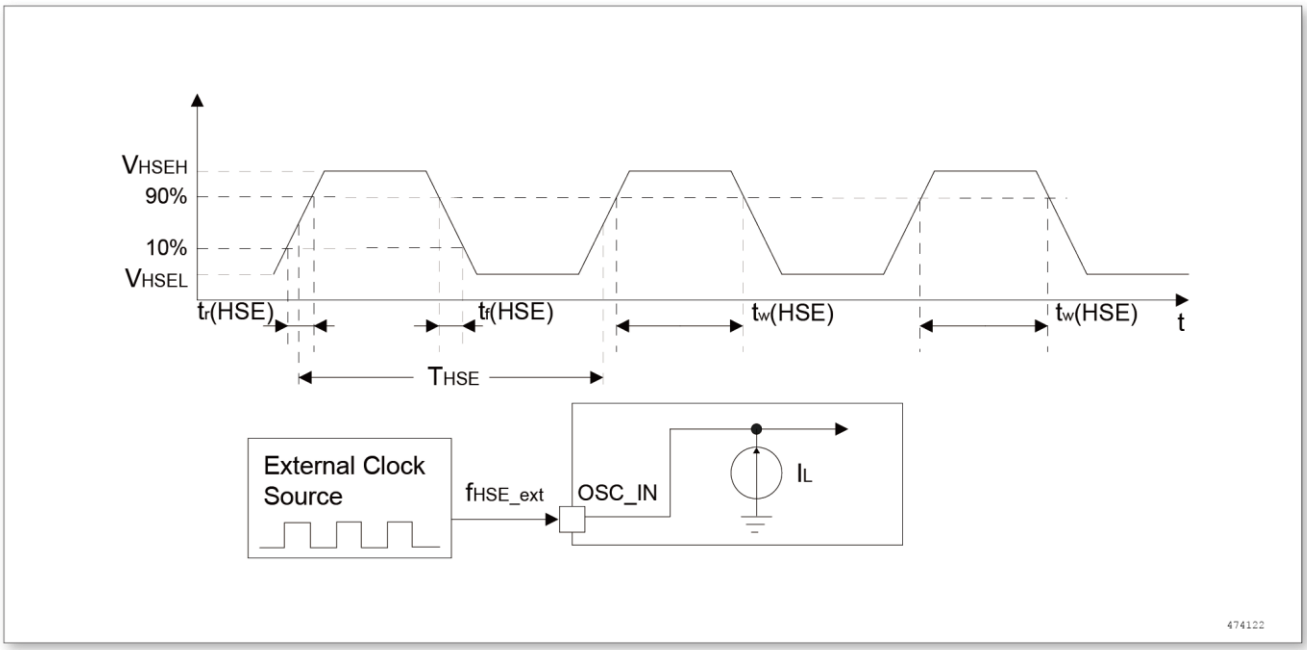

Figure 18 High-speed external user clock alternate current timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be generated by an oscillator composed of an 4 ~ 24MHz crystal/ceramic resonator. All the information given in this section is based on the results obtained from comprehensive characteristic evaluation with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and stabilization time at startup. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy, etc.).

Table22 HSE 8~24MHz oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	24	MHz
R_F	Feedback resistance	-	-	1000	-	kΩ
C_{L1}/ C_{L2} (3)	The proposed load capacitance corresponds to the crystal serial	R_S = 30 Ω	-	30	-	Ω

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
	impedance (RS) (4)					
I_2	HSE current consumption	V_{DD} = 3.3V V_{IN} = V_{SS} 30pF load	-	-	4.5	mA
g_m	Oscillator transconductance	Startup	-	8.5	-	mA/V
$t_{SU(HSE)}$ (5)	Startup time	V_{DD} is stabilized	-	3	-	mS

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer
2. Drawn from comprehensive evaluation, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5pF to 25pF range (typical value) designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} usually have the same parameters. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10pF can be used as a rough estimate of the combined pin and board capacitance) when choosing choosing C_{L1} and C_{L2}.
4. The relatively low R_F resistance value can provide protection and avoid problems occurred when operating in a humid environment. Changes have been made to leakage and bias conditions generated in this environment. However, if the MCU is used in harsh humid conditions, such parameters need to be considered in designing.
5. $t_{SU(HSE)}$ is the startup time, measured from the moment it is enabled HSE by software to a stablized 8 MHz is reached. This value is measured from a standard crystal resonator and it can vary significantly with the crystal manufacturer.

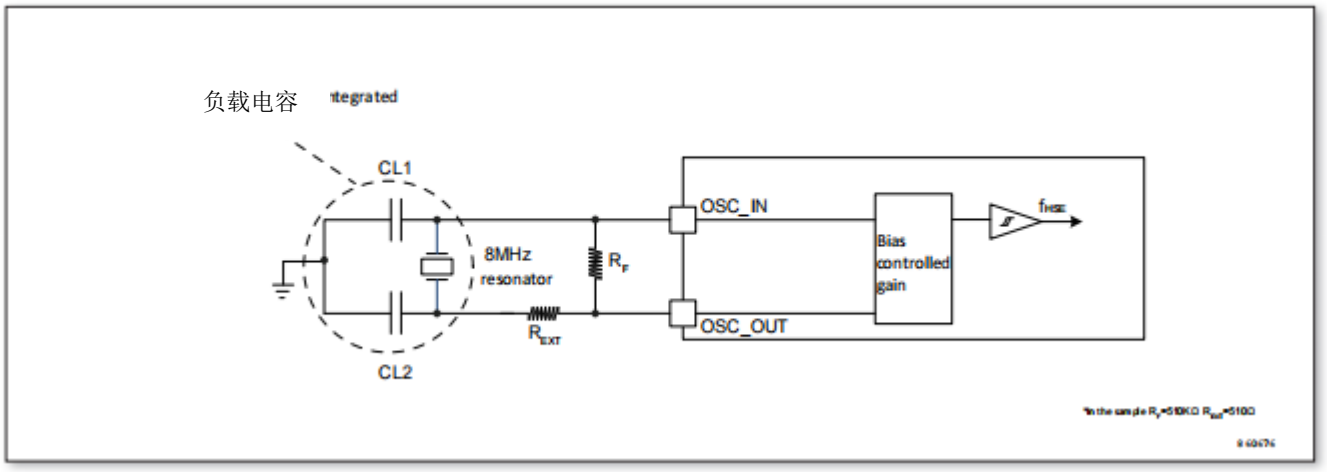

Figure 19 Typical application with an 8MHz crystal

4.3.7 Internal Clock Source Characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and supply voltage conforming to the general operating conditions.

High-speed internal (HSI) oscillator

Table23 HSI oscillator characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{HSI}	Frequnecy	-	-	48/72	-	MHz
ACC_{HSI}	HSI oscillator accuracy	T_A=-40℃~105℃	-2.5	-	+2.5	%
		T_A=-10℃~105℃	-2		+2	%
		T_A=25°C	-1	-	+1	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	-	10	-	μS
$T_{stab(HSI)}$	HSI oscillator stablization time	-	-		-	μS
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	200	-	μA

1. V_{DD} = 3.3V, T_A = - 40℃~ 105℃, unless otherwise specified.

2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 24 LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{LSI}(2)	Frequnecy	-	-	40	-	KHz
$t_{SU(LSI)}$(3)	LSI oscillator startup time	-	-	-	100	μS
$t_{stab(LSI)}$(3)	LSI oscillator stablization time	-	-	-		μS
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	-	1.1	1.7	μA

1. V_{DD} = 3.3V, T_A = - 40℃~ 105℃, unless otherwise specified.
2. Guaranteed by design, not tested in production.

4.3.8 Memory Characteristics

Table 25 Flash memory characteristics

Symbol	参数	条件	最小值	典型值	最大值	单位
t_{prog}	16-bit programming time	-	-	28	-	μS
t_{ERASE}	Page (1024K bytes) erase time	-	-	8	10	mS
t_{ME}	Full erase time	-	-	30	40	mS
I_{DD}	Average current consumption	Read mode 40MHz	-	9	-	mA
	-	Write mode	-	-	7	mA
	-	Erase mode	-	-	2	mA

Table 26 Flash memory endurance and data retention period (1)(2)

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
N_{END}	Erase times		20000	-	-	Times
T_{DR}	Data retention	T_A=105℃	20	-	-	Years
		T_A=25℃	100	-	-	

4.3.9 EMC Charcateristics

Susceptibility tests are performed on a sample basis during device comprehensive evaluation.

Functional EMS (electromagnetic susceptbility)

When a simple application is executed (toggling two LEDs through I/O ports), the test sample is stressed by one electromagnetic interference until an error occurs. The error is indicated by the flashing LEDs.

- EFT：In V_{DD} and V_{SS}, impose a pulse group (forward and backward) with a transient voltage by a 100 pF capacitor until a functional error is generated. This test complies with the IEC61000-4-4 standard.

Chip reset can restore normal operation of the system. The test results are listed in the table below.

Table 27 EMS characteristics

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=3.3V，T_A=+25℃，f_{HCLK}=72MHz。Conforming to IEC61000-4-2	2A

Symbol	Parameter	Conditions	Level/class
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}=3.3V，T_A=+25℃，f_{HCLK}=72MHz。Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC evaluation and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and qualification tests in relation with the EMC.

Software recommendations

The software flowchart must include the management of runaway conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or the crystal oscillator pins for 1 second.

To complete ESD test, a voltage can be applied directly on the chip, over the range of application requirements. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.3.10 Functional EMS (electrical sensitivity)

Based on three different tests (ESD, LU), using specific measurement methods, the chip is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive then a negative pulse separated by 1 second) are applied to the all pins of each sample. The sample size depends on the number of supply pins on the chip (3 parts x (n + 1) supply pins). This test conforms to the JEDEC JS-001-2017/002-2018 standard.

Static latchup

Two complementary static latchup tests are required on six samples to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin. This test is compliant with the EIA/JESD78E IC latchup standard.

Table 28 ESD characteristics

Electrical Characteristics

Symbol	Parameter	Conditions	Level/class	Max.	Unit
VESD(HBM)	Electrostatic discharge voltage (mannequin)	TA=25℃，conforming ESDA/JEDECJS-001-2017	2	±4000	V
VESD(CDM)	Electrostatic discharge voltage (charging device model)	TA=25℃，conforming ESDA/JEDECJS-002-2018	C1	±500	V
ILU	Electrostatic latchup (Latchup current)	TA=25℃，conforming JESD78E	IA	±100	mA

4.3.11 GPIO port general input/output characteristics

Unless otherwise specified, the parameters listed in the table below are derived from tests performed under the conditions summarized in Table 10. All I/O ports are CMOS-compliant.

Table 29 I/O static characteristics

SPEED	Parameter	Conditions	Min.	Typical	Max.	Unit
V_{IL}	Input low level voltage	2.5V< VDD < 5.5V	-	-	0.3*VDD	V
V_{IH}	Input high level voltage	2.5V< VDD < 5.5V	0.7*VDD	-	-	V
V_{hy}	I/O pin Schmidt trigger voltage hysteresis (1)	2.5V< VDD < 5.5V	-	0.1*VDD	-	V
I_{lkg}	Input leakage current (2)	2.5V< VDD < 5.5V	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistance (3)	2.5V< VDD < 5.5V	10	-	100	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	2.5V< VDD < 5.5V	10	-	100	kΩ
C_{IO}	I/O pin capacitor	-	-	-	10	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. In case of a negative current back flow in the adjacent pin, the leakage current may be higher than the maximum value.
3. Pull-up and pull-down resistance is MOS resistance.

Output drive current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA current

In user application, the number of I/O pin must ensure that the drive current must be limited to respect the absolute maximum rating specified in Section 4.2:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum running current of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents absorbed and sunk by all the I/O pins on V_{SS}, plus the maximum running current of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS}.

Output voltage

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 12. All I/O ports are CMOS-compliant.

Table 30 Output voltage characteristics

SPEED	Symbol	Parameter	Conditions	Min	Typical	Max	Unit
11 (50MHz)	V_{OL}(1)	Output low level	$\|I_{IO}\|$=6mA，VDD=3.3V			0.40	V
	V_{OH}(2)	Output high level		2.80			

Electrical Characteristics

SPEED	Symbol	Parameter	Conditions	Min	Typical	Max	Unit
	V_{OL}(1)(3)	Output low level	|I_{IO}|=8mA，VDD=3.3V			0.40	
	V_{OH}(2)(3)	Output high level		2.80			
	V_{OL}(2)(3)	Output low level	|I_{IO}|=20mA，VDD=3.3V			0.80	
	V_{OH}(2)(3)	Output high level		2.20			
10 (2MHz)	V_{OL}(1)	Output low level	|I_{IO}|=6mA，VDD=3.3V			0.40	
	V_{OH}(2)	Output high level		2.80			
	V_{OL}(1)(3)	Output low level	|I_{IO}|=8mA，VDD=3.3V			0.60	
	V_{OH}(2)(3)	Output high level		2.60			
	V_{OL}(2)(3)	Output low level	|I_{IO}|=20mA，VDD=3.3V			1.00	
	V_{OH}(2)(3)	Output high level		1.80			
01 (10MHz)	V_{OL}(1)	Output low level	|I_{IO}|=6mA，VDD=3.3V			0.60	
	V_{OH}(2)	Output high level		2.60			
	V_{OL}(1)(3)	Output low level	|I_{IO}|=8mA，VDD=3.3V			0.60	
	V_{OH}(2)(3)	Output high level		2.40			
	V_{OL}(2)(3)	Output low level	|I_{IO}|=20mA，VDD=3.3V			1.40	
	V_{OH}(2)(3)	Output high level					

1. The I_{IO} current sourced by the chip must always respect the absolute maximum rating specified in the table, and the sum of I_{IO} (all I/O ports and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} sunk by the chip must always respect the absolute maximum rating speified in the table, and the sum of I_{IO} (all I/O ports and control pins) cannot exceed I_{VDD}.
3. Drawn from comprehensive evaluation.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in Unless otherwise specified, the parameter listed in Table 34 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 12.

Table 31 and Figure 20, respectively.

Unless otherwise specified, the parameter listed in Table 34 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 12.

Table 31 Input/output AC characteristics (1)(3)

SPEED[1:0] configuration	Symbol	Parameter	Conditions	Min	Typical	Max	Unit
11	$t_{f(IO)out}$	Output high to low level fall time	C_L=50pF VDD=3.3V		4.0		ns
	$t_{r(IO)out}$	Output low to high level rise time			5.0		ns
10	$t_{f(IO)out}$	Output high to low level fall time			5.0		ns
	$t_{r(IO)out}$	Output low to high level rise time			6.2		ns
01	$t_{f(IO)out}$	Output high to low level fall time			7.2		ns
	$t_{r(IO)out}$	Output low to high level rise time			11.0		ns

1. The I/O port speed is configured through MODEx[1:0]. Refer to the Reference manual for a description of the GPIO port configuration register.
2. The maximum frequency is defined in Figure 20.
3. Guaranteed by design, not tested in production.

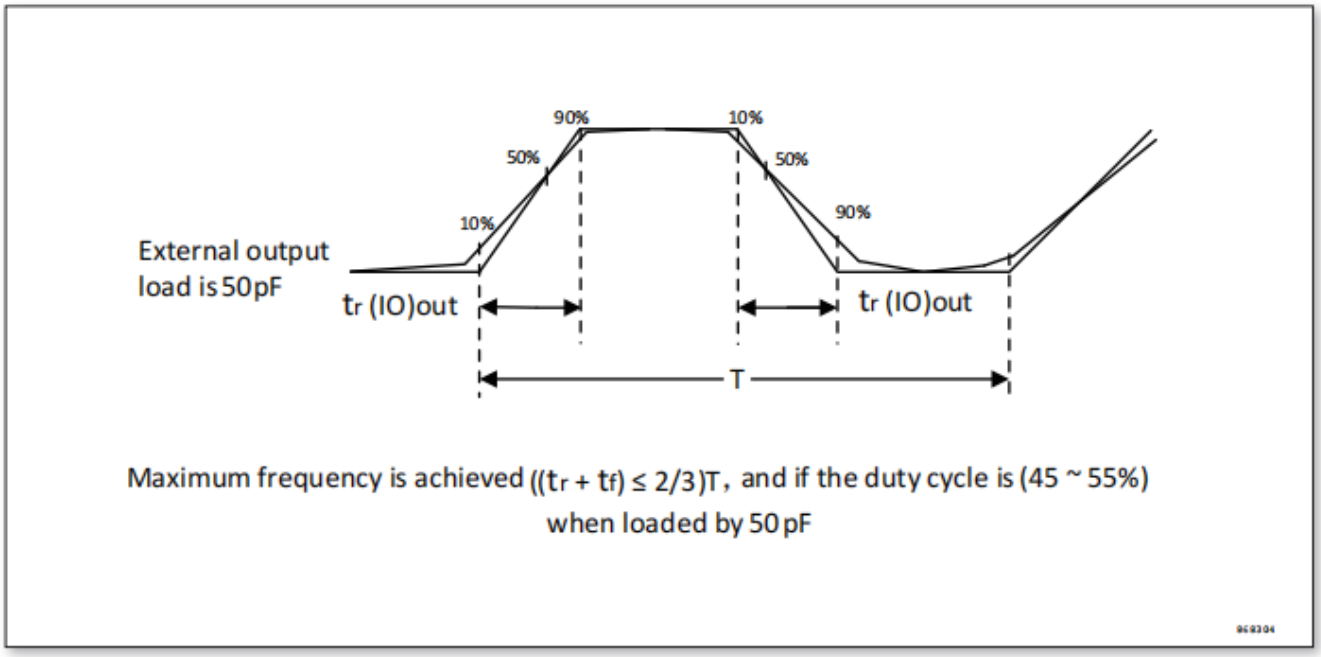

Figure 20 Input/output AC characteristics definition

4.3.12 NRST Pin Characteristics

The NRST pin input driver uses the CMOS technology, and it is connected to a permanent pull-up resistor, RPU. Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 12 General operating conditionsTable 12。

Table32 NRST characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage		-0.3	-	0.3*VDD	V
$V_{IH(NRST)}$(1)	NRST input high level voltage		0.7*VDD	-	VDD	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		-	0.1*VDD	-	V
R_{PU}	Weak pull-up equivalent resistor (2)	V_{IN}=V_{SS}	-	50		kΩ

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is a MOS resistor.

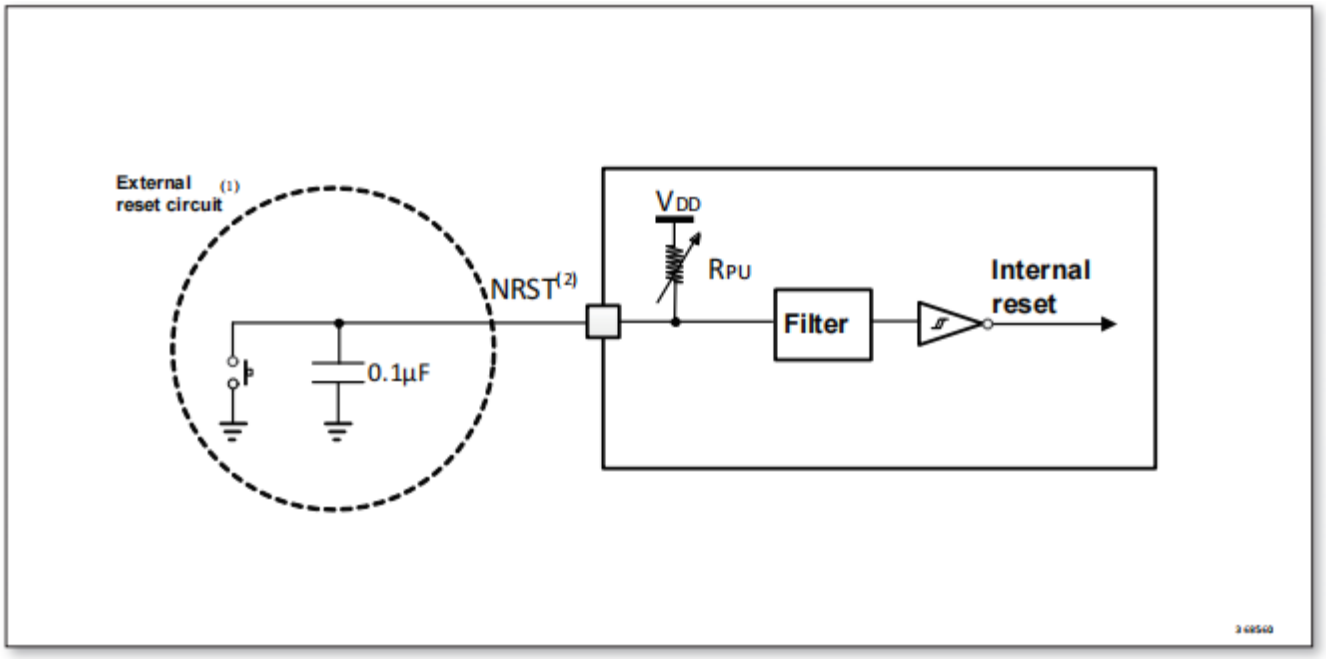

Figure 21 Recommended NRST pin protection

1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 44, otherwise the MCU cannot be reset.

4.3.13 Timer characteristics

The parameters given in the table below are guaranteed by design.

Refer to Section 4.3.11 GPIO port general input/output characteristics for details on the input/output alternate function pin (output compare, input capture, external clock, PWM input).

Table33 TIMx(1) characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=24MHz	41.6	-	nS
f_{EXT}	CH1 to CH4 timer external clock frequency	-	0	$f_{TIMxCLK}$	MHz
		$f_{TIMxCLK}$=24MHz	0	24	
Res_{TIM}	Timer resolution	-	-	16	位
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=24MHz	0.0417	2732	µS
t_{MAX_COUNT}	Maximum possible count(TIM_PSC adjustable)	-	-	65536*65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=24MHz	-	178.9	S

4.3.14 Communication Interface

I2C interface characteristics

Unless otherwise specified, the parameters given in the table below are derived from the tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in Table 12.

The I2C interface complies with the standard I2C communication protocol, but has the following limitations: the SDA and SCL are not "true open-drain " pins. When

configured as open-drain, the PMOS tube connected between the pin and V_{DD} is disabled, but is still present.

I2C interface characteristics are listed in the table below. Refer to section 4.3.11 for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 34 I2C characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C(1)		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	μs
$t_{su(SDA)}$	SDA establishment time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data retention time	0(3)	-	0(4)	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	2.0+0.1C_b	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated start condition establishment time	4.7	-	0.6	-	μs
$t_{su(STO)}$	Stop condition establishment time	4.0	-	0.6	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (Bus Free)	4.7	-	1.3	-	μs
C_b	Capacitive load of each bus	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. To reach the maximum frequency of I2C standard mode, f_{PCLK1} must be greater than 3MHz. To reach the maximum frequency of I2C fast mode, f_{PCLK1} must be greater than 12MHz
3. If the low-level time of the SCL signal is not required to be lengthened, only the maximum hold time of the startup condition needs to be met.
4. In order to cross the undefined area of the falling edge of SCL, a hold time of at least 300nS on the SDA signal must be guaranteed inside the MCU.

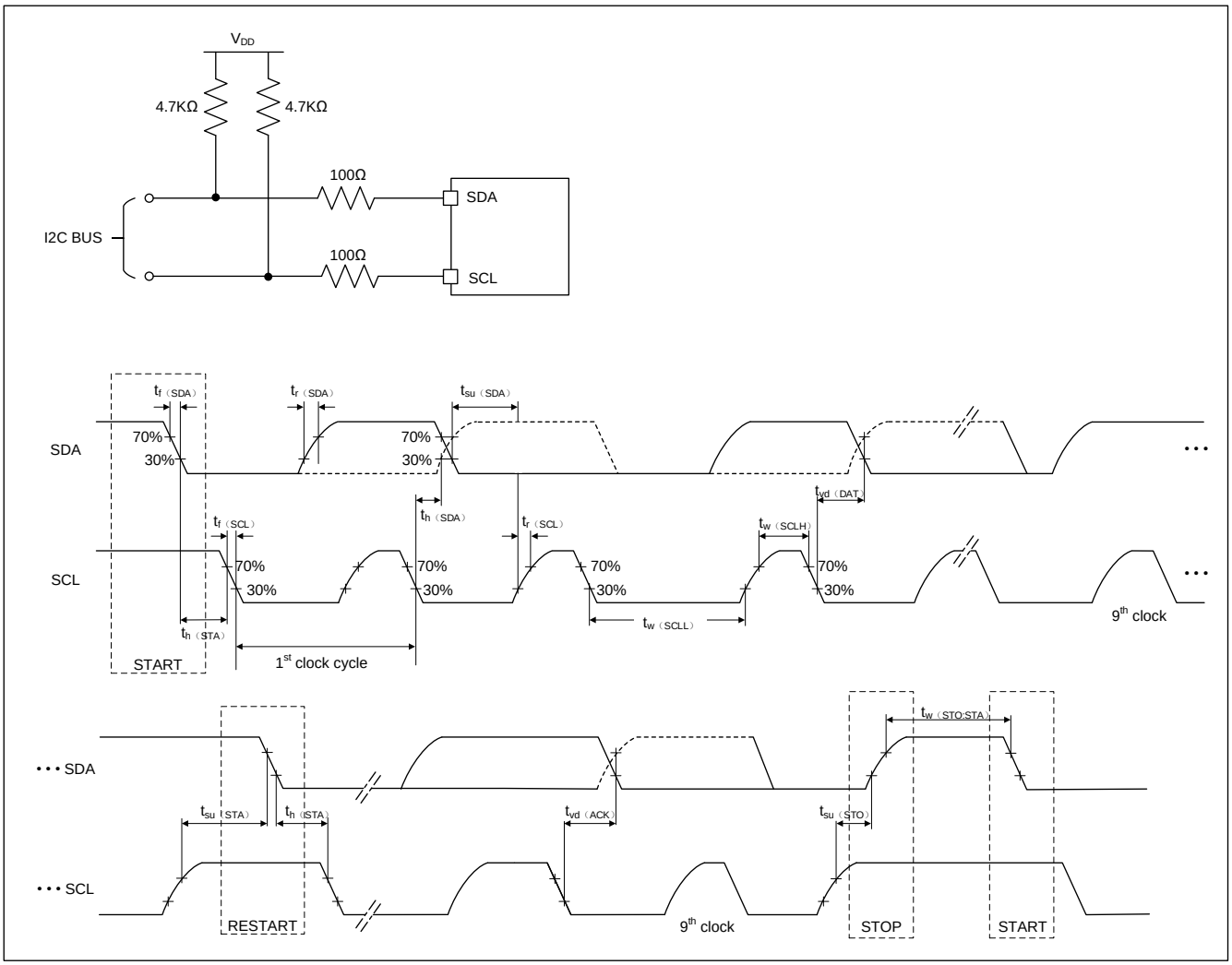

Figure 22 I2C bus AC waveform and measurement circuit (1)

1. The measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$

SPI interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, fPCLKx frequency and VDD supply voltage conditions summarized in Table 12.

Refer to section 4.3.11 for more details on the input/output alternate function pins (NSS, SCK, MOSI, MISO)

Table 35 SPI characteristics (1)

Symbol	Parameter	Conditions	Min.	Max.	Unit
$f_{SCK}1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	36	MHz
		Slave mode	0	18	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	8	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance:C = 15pF	-	8	nS
$t_{su(NSS)}$(1)	NSS establishment time	Slave mode	$4t_{PCLK}$	-	nS
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	73	-	nS
$t_{w(SCKH)}$(1)	SCK high level time	Master mode，f_{PCLK} = 36MHz， prescale coefficient = 4	50	60	nS
$t_{w(SCKL)}$(1)	SCK low level time	Master mode，f_{PCLK} = 36MHz， prescale coefficient = 4	50	60	nS

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{su(MI)}$(1)	Data input establishment time	Master mode	-	-	nS
$t_{su(SI)}$(1)		Slave mode	1	-	nS
$t_{h(MI)}$(1)	Data input hold time	Master mode	-	-	nS
$t_{h(SI)}$(2)		Slave mode	3	-	nS
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode，f_{PCLK} = 36MHz， prescale coefficient = 4	0	55	nS
		Slave mode，f_{PCLK} = 24MHz		4*t_{PCLK}	nS
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	10		nS
$t_{v(MO)}$(2)(1)	Data output valid time	Master mode (after enable edge)	-	3	nS
$t_{v(SO)}$(2)(1)		Slave mode (after enable edge)	-	25	nS
$t_{h(MO)}$(2)	Data output hold time	Master mode (after enable edge)	4		nS
$t_{h(SO)}$(2)		Slave mode (after enable edge)	25		nS

1. Drawn from comprehensive evaluation.
2. The minimum value indicates the minimum time for driving output, and the maximum value indicates the maximum time to obtain data correctly.
3. The minimum value represents the minimum time for closing output, and the maximum value represents the maximum time to put the data line in the high impedance state.

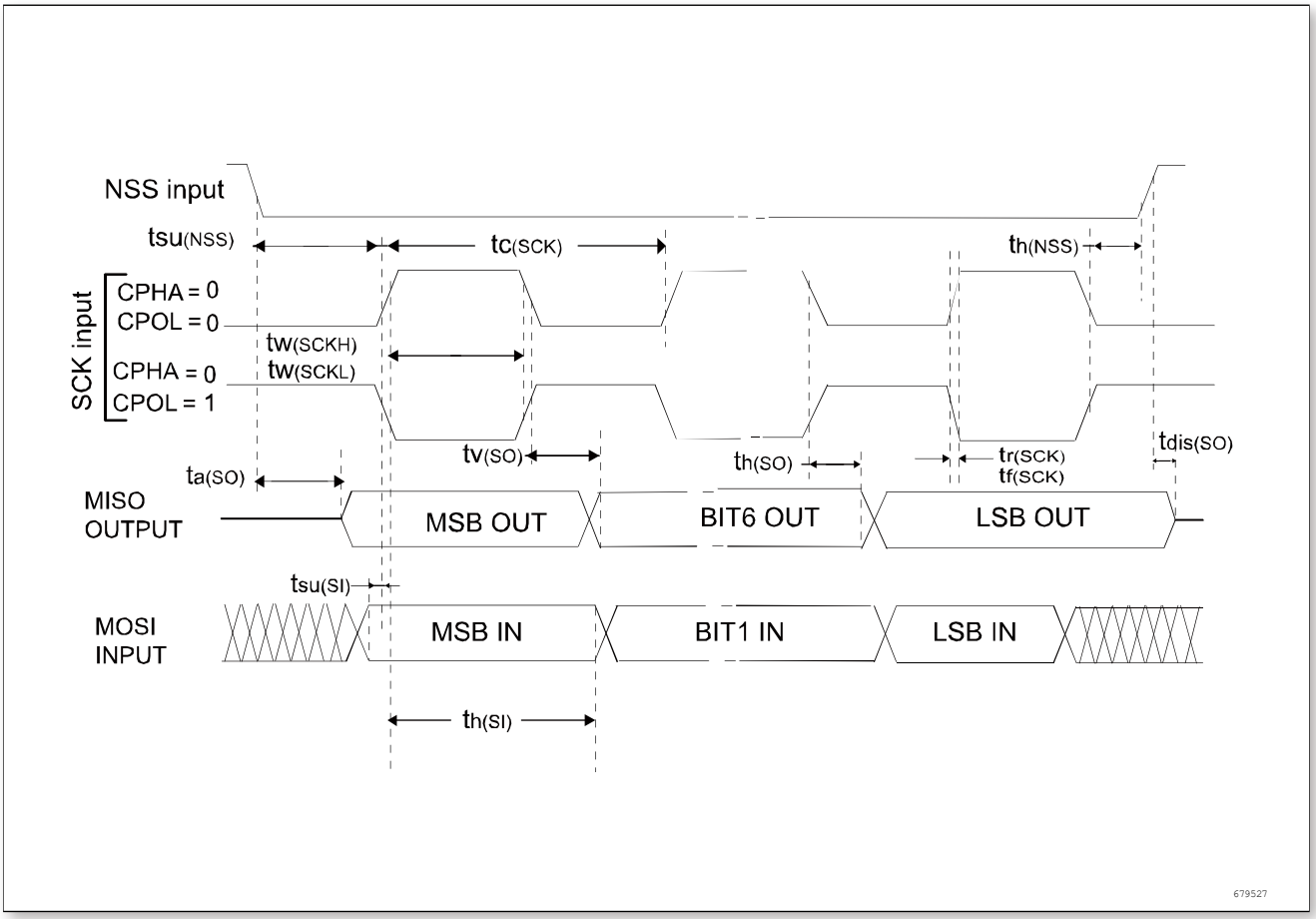

Figure 23 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

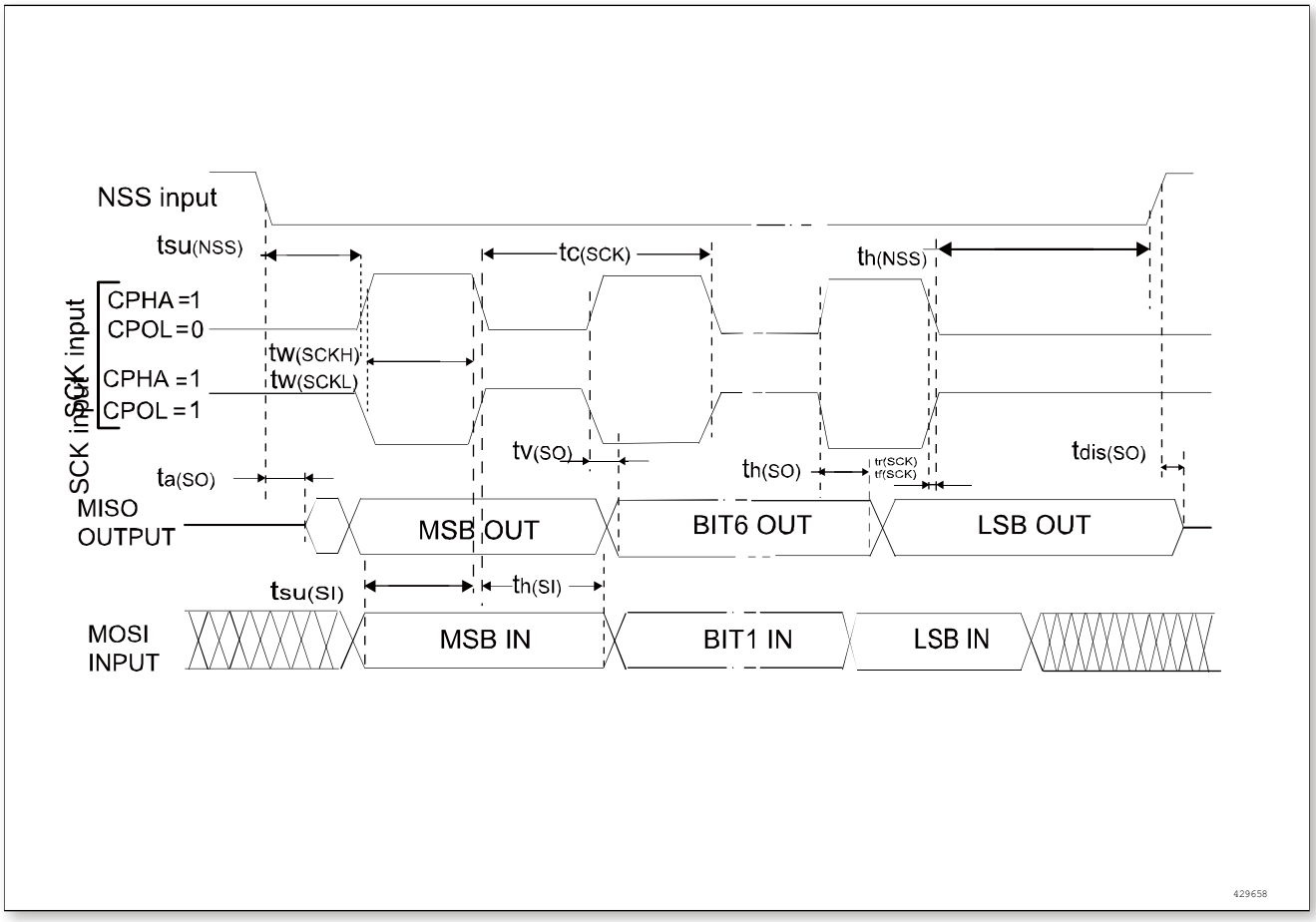

Figure 24 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)

1. Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$

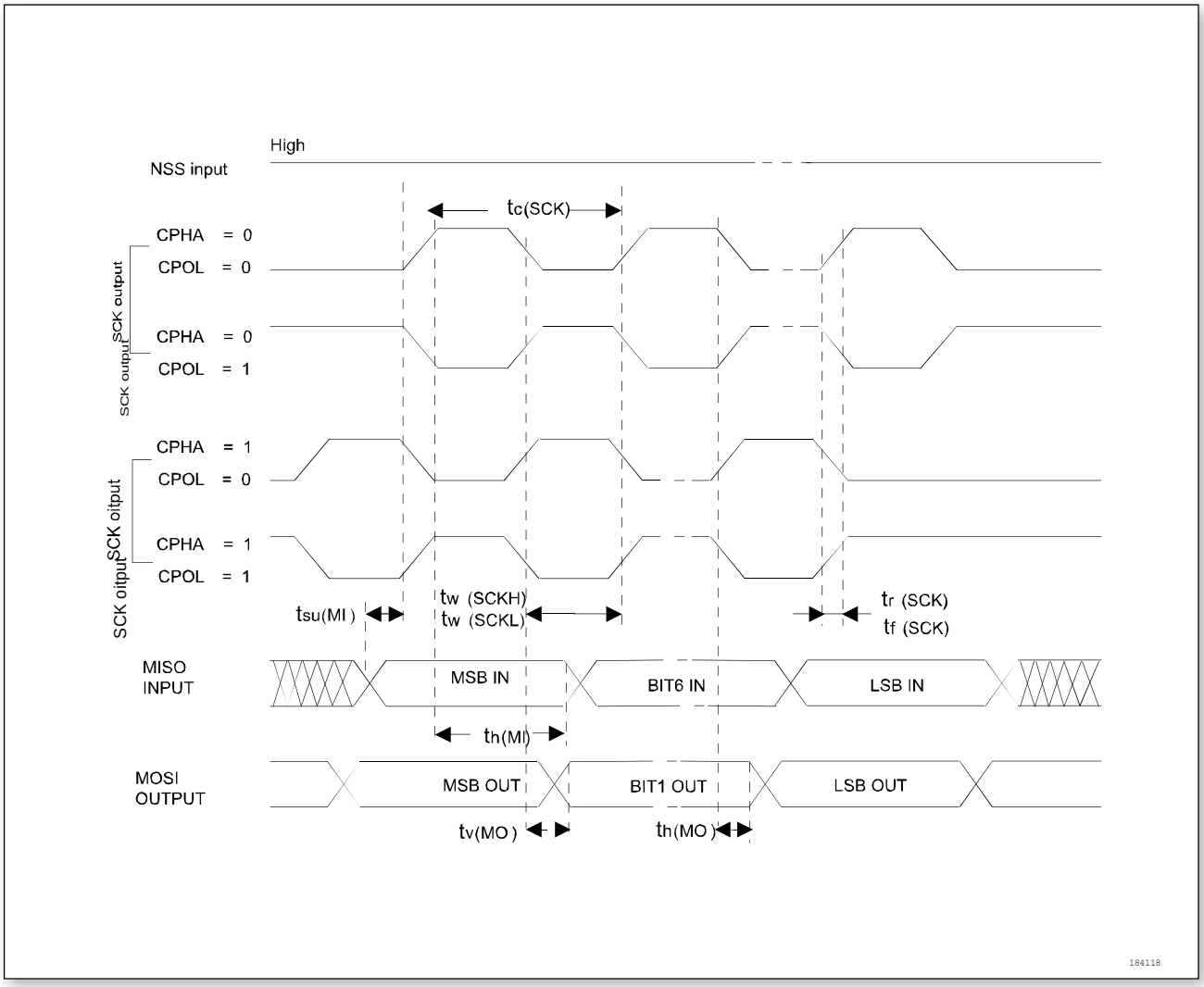

Figure 25 SPI timing diagram-master mode (1)

1. Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.15 ADC Characteristics

Unless otherwise specified, the parameters in the following table are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage specified in Table 12.

Table 36 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	15(1)	MHz
f_S(2)	Sampling rate	-	-	-	1	MHz
f_{TRIG}(2)	External trigger frequency (3)	12bits;f_{ADC}=15MHz	-	-	823	kHz
		12bits	-	-	1/17	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range	-	V_{SSA}	-	V_{DDA}	V
R_{AIN}(2)	External input impedance	-	See Formulas 1 and Table 37			kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
C_{ADC}(2)	Internal sample and hold capacitor	-	-	10	-	pF
t_s(2)	Sampling time	f_{ADC} = 15MHz	0.1	-	16	μS
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(1)	Power-on time	-	-	1	-	μS
T_{conv}(2)	Total conversion Time (Including sampling time)	f_{ADC} = 15MHz	1		16.9	μS
			15 ~ 253 (sampling t_{S+}) stepwise approximation 13.5			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product series, V_{REF+} is connected to V_{DDA}, V_{REF-} connected to V_{SSA} internally.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of 1/ f_{ADC} must be added to the delay.

Input impedance list

$$R_{AIN} < \frac{TS}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12bit resolution) .

Table 37 Maximum R_{AIN} at f_{ADC} = 15MHz(1)

T_S（cycles）	t_S（μS）	R_{AIN} max（kΩ）
1.5	0.1	0.1
7.5	0.5	4.0
13.5	0.9	7.8
28.5	1.9	17.5
41.5	2.76	25.9
55.5	3.7	34.9
71.5	4.77	45.2
239.5	16.0	153.4

1. Guaranteed by design, not tested in production.

Table38 ADC static parameter (1)(2)

Symbol	Parameter	Conditions	Typical	Unit	Parameter
ET	Composite error	f_{PCLK2}=60MHz， f_{ADC}=15MHz，R_{AIN}<10kΩ， V_{DDA}=3.3V，T_A=25°C	±10	±14	LSB
EO	Offset error		±4	±10	
EG	Gain error		±6	±8	
ED	Differential linearity error		±2	±4	
EL	Integral linearity error		±4	±6	

1. Correlation between ADC accuracy and negative injection current: Injecting negative current on any standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input pin. It is recommended to add a Schottky diode (pin to ground) to standard analog pins that may potentially inject negative current. If the forward injection current is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in Section 4.3.12, the ADC accuracy will not be affected.
2. Guaranteed by comprehensive evaluation, not tested in production.
3. ET = Total unadjusted error: the maximum deviation between the actual and ideal transfer curves.
4. EO = Offset error: the deviation between the first actual transition and the first ideal one.
5. EG = Gain error: the deviation between the last ideal transition and the last actual one.
6. ED = Differential linearity error: the maximum deviation between the actual steps and the ideal ones.

7. EL = Integral linearity error: the maximum deviation between any actual transition and the endpoint correlation line.

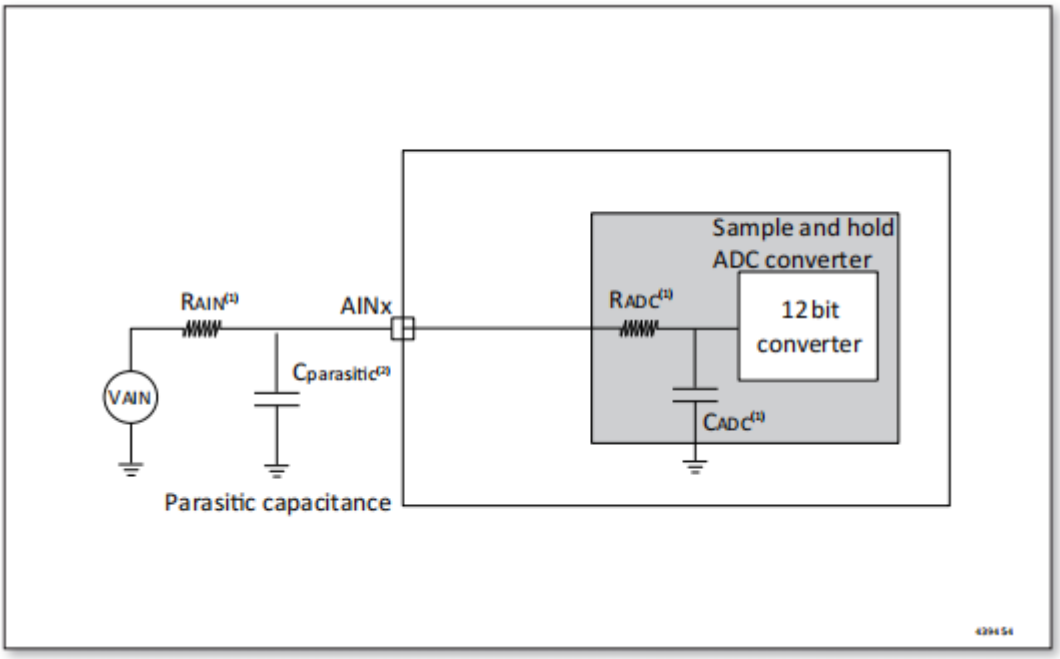

Figure 26 Typical connection diagram using ADC

1. Refer to Table 36 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the parasitic capacitance (about 7pF) on the PCB (dependent on soldering and PCB layout quality) and the pad. A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design guidelines

Power supply decoupling should be performed as shown in the diagram below. The 10 nF capacitor should be ceramic and it should be placed as close as possible to the MCU chip.

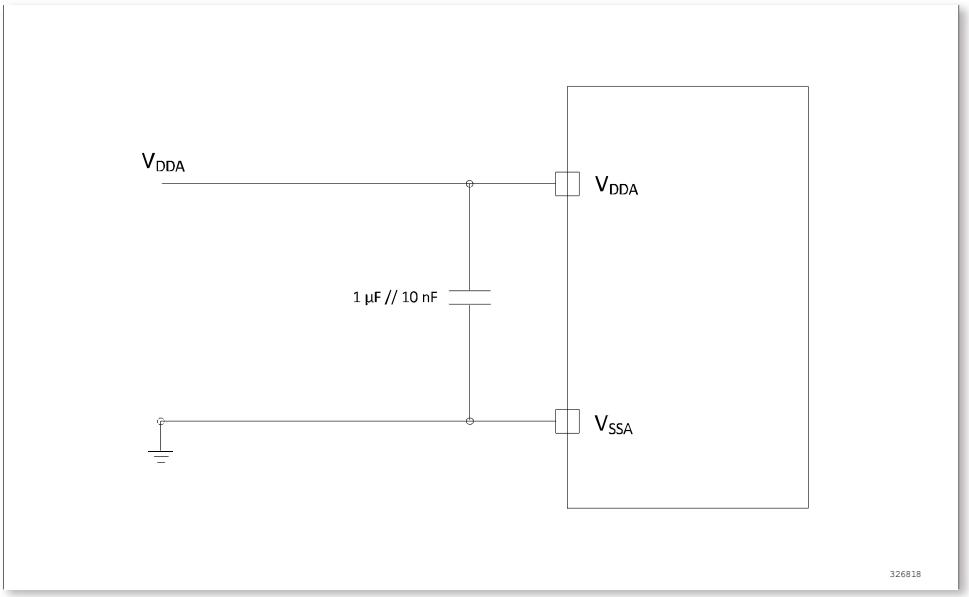

Figure 27 Decoupling circuit of power supply and reference power supply

4.3.16 Temperature Sensor Characteristics

Table 39 Temperature sensor characteristics (3)(4)

Electrical Characteristics

Symbol	Parameter	Min.	Typical	Max.	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±5	-	◦C
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/◦C
V_{25}(1)	Voltage at 25℃	1.433	1.451	1.467	V
t_{START}(2)	Establishment time	-	-	10	μS
t_{S_temp}(2)	ADC sampling time when reading the temperature	10	-	-	μS

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by application through multiple circulations.
4. V_{DD} = 3.3V
5. Temperature formula: TS_adc = 25 + (value*vdda – offset*3300)/(4096*Avg_slope), offset recorded in 0x1FFFF7F6 low 12-bit.

4.3.17 Comparator Characteristics

Table 40 Comparator characteristics

Comparator characteristics						
Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
t_{HYST}	Hysteresis	00	-	0	-	mV
		01	-	15	-	mV
		10	-	30	-	mV
		11	-	90	-	mV
V_{OFFSET}	Offset voltage	00	0.091	0.213	0.358	mV
		01	3.23	7.51	12.08	mV
		10	9.79	15	20.8	mV
		11	34.25	47.4	62.22	mV
t_{DELAY}(1)	Propagation delay	00	-	80	-	ns
		01	-	51	-	ns
		10	-	26	-	ns
		11	-	9	-	ns
I_q(2)	Average operating current	00	-	4.5	-	uA
		01	-	4.4	-	uA
		10	-	4.4	-	uA
		11	-	4.4	-	uA

1. Time difference between output flip 50% and input flip.
2. Mean value of the total consumption current, running current.

5 Package Dimensions

5.1 Package LQFP48

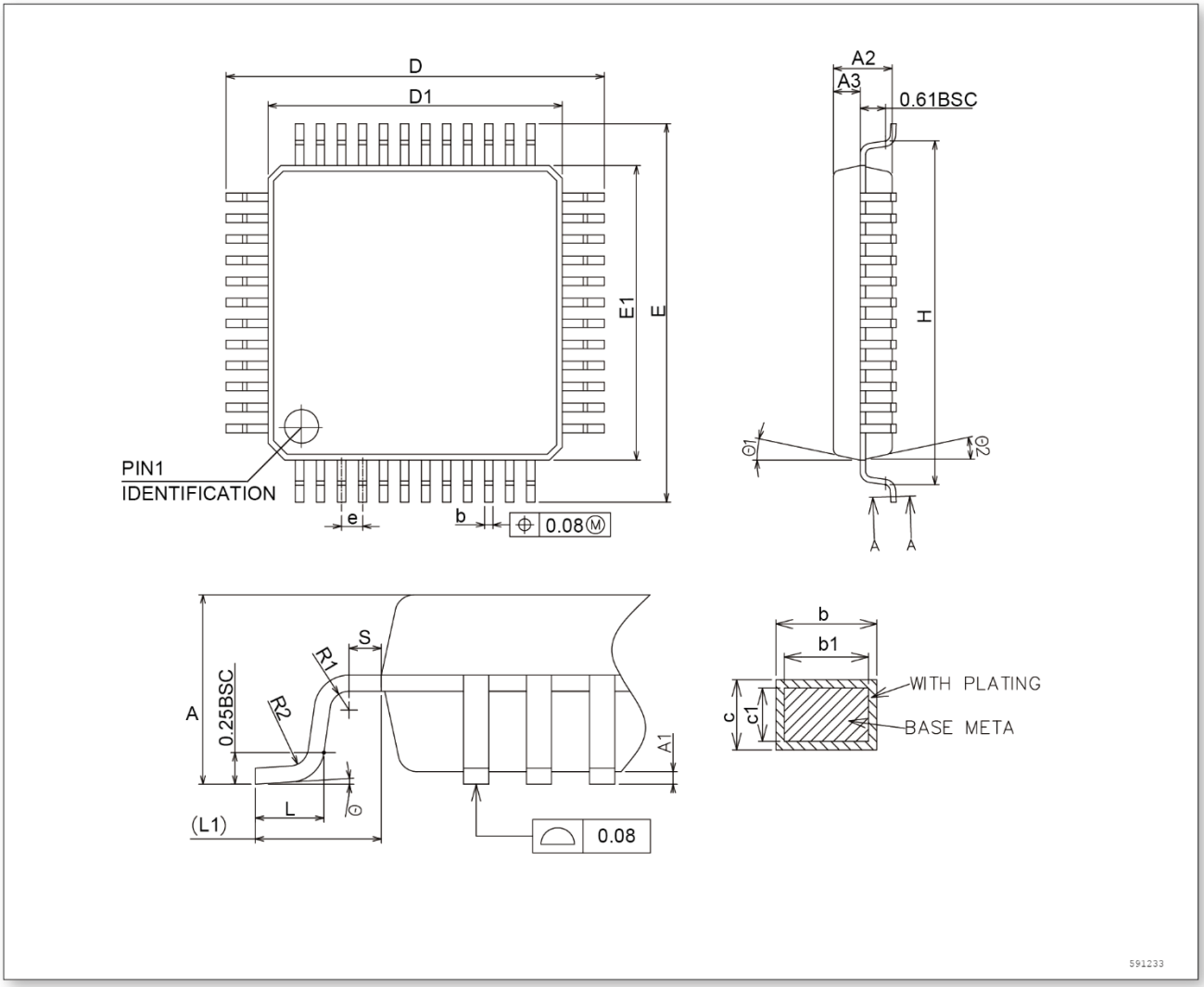

Figure 28 LQFP48, 48-pin low-profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Package Dimensions

Table 41 LQFP48 dimensions

Symbol	Milimeter		
	Minimum	Typical	Maximum
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
Θ3	11°	12°	13°

5.2 Package LQFP32

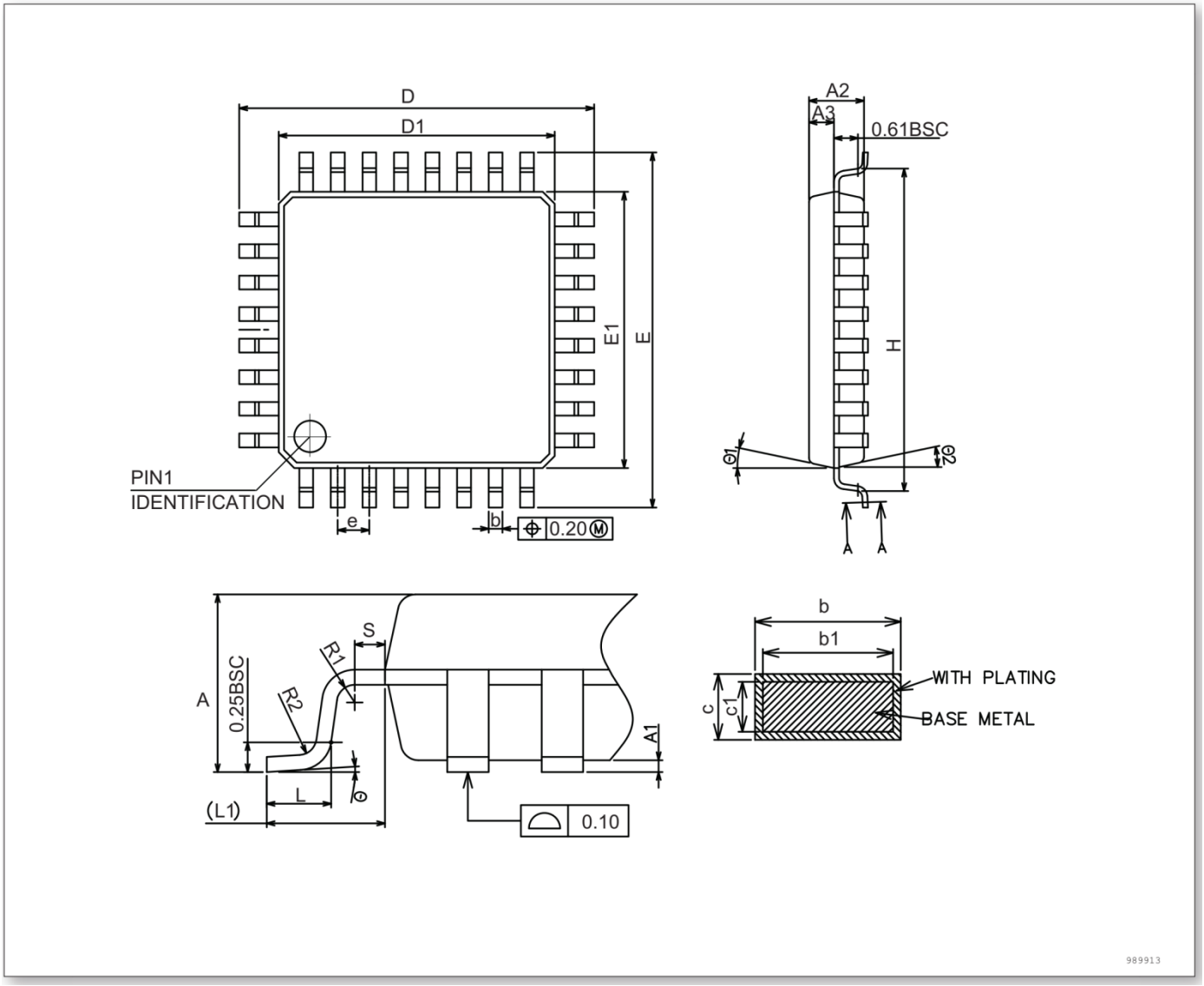

Figure 29 LQFP32, 32-pin low profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Package Dimensions

Table 42 LQFP32 dimensions

Symbol	Milimeter		
	Minimum	Typical	Maximum
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
A3	0.59	0.64	0.69
b	0.32		0.43
b1	0.31	0.35	0.39
c	0.13		0.18
c1	0.12	0.127	0.134
D	8.8	9	9.2
D1	6.9	7	7.1
E	8.8	9	9.2
E1	6.9	7	7.1
e	0.8		
L	0.45	0.6	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08		
R2	0.08		0.2
S	0.2		
θ	0 ◦	3.5 ◦	7 ◦
θ1	11 ◦	12 ◦	13 ◦
θ2	11 ◦	12 ◦	13 ◦

5.3 Package QFN32

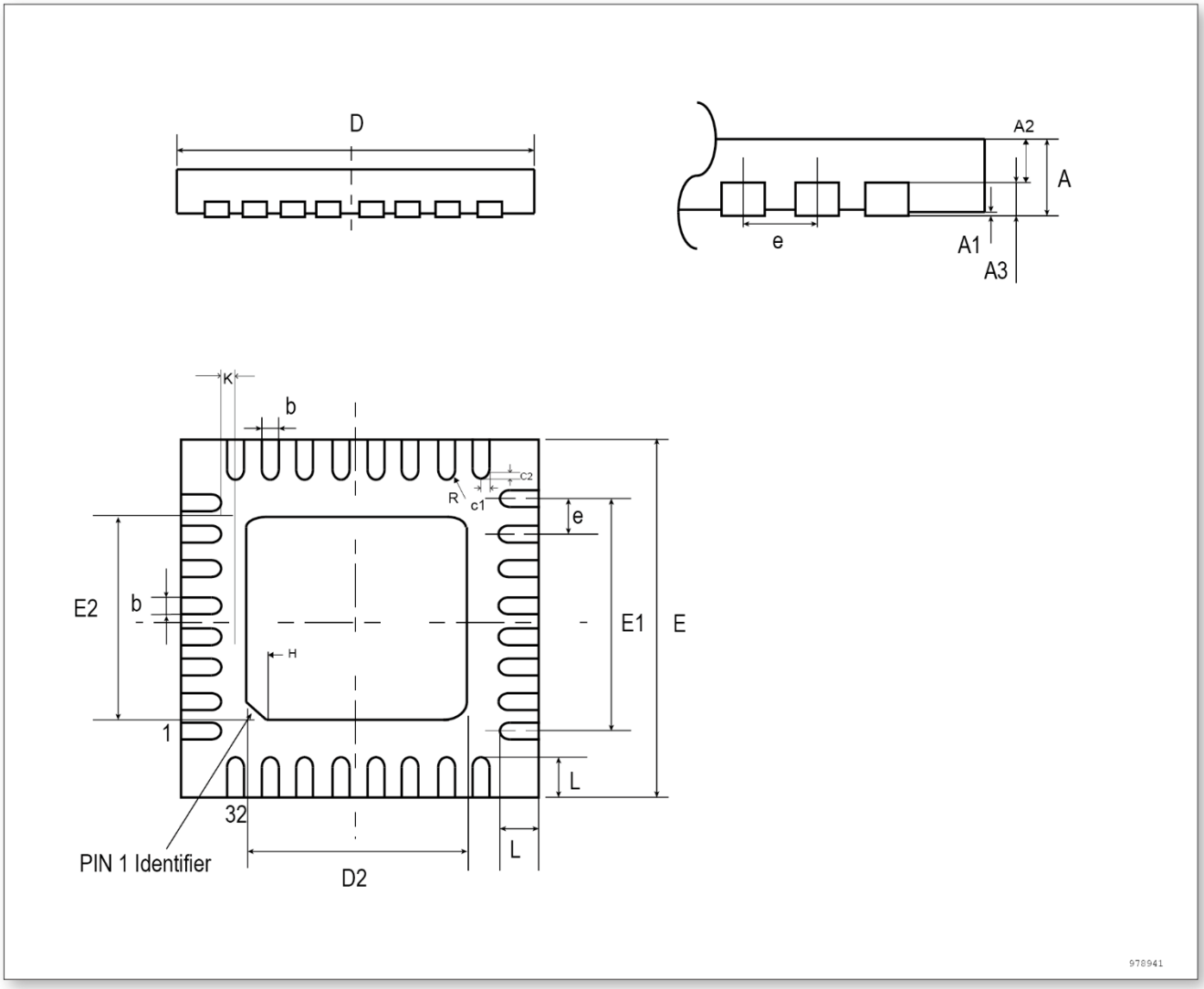

Figure 30 QFN32, 32-pin low profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 43 QFN32 dimensions

Symbol	Milimeter		
	Minimum	Typical	Minimum
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.20	0.25	0.30
c1	-	0.08	-
c2	-	0.08	-
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
e		0.50	
H	0.30REF		
K	0.35REF		
L	0.35	0.40	0.45
R	0.09	-	-

5.4 Package QFN20

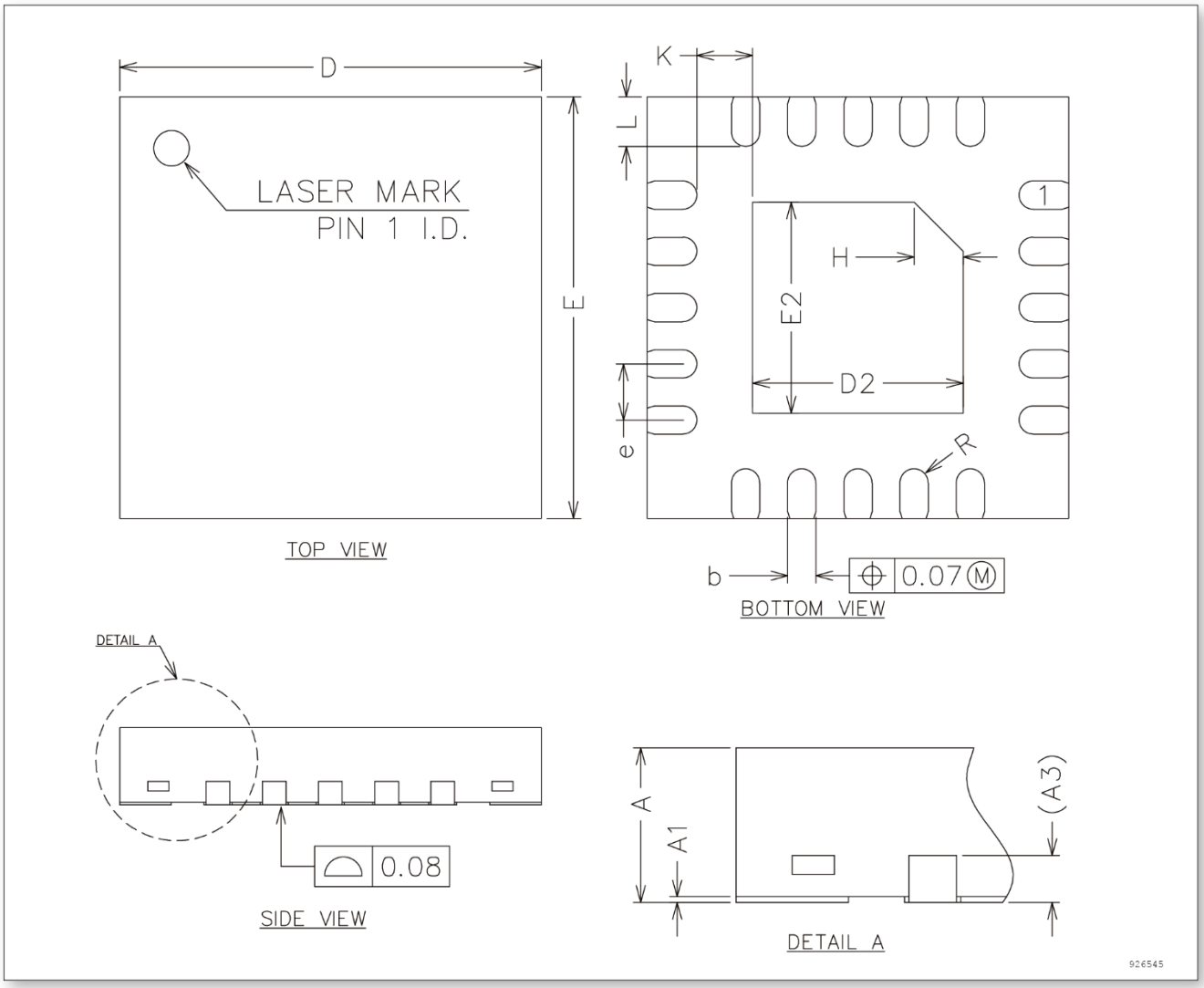

Figure 31 QFN20, 20-pin low profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Package Dimensions

Table 44 QFN20 dimensions

Symbol	Milimeter		
	Minimum	Typical	Maximum
A	0.50	55	0.60
A1	0.00	0.02	0.05
A3	0.152REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e	0.30	0.40	0.50
H	0.35REF		
K	0.40REF		
L	0.25	0.35	0.45
R	0.075		
N	Number of pins = 20		

5.5 Package TSSOP20

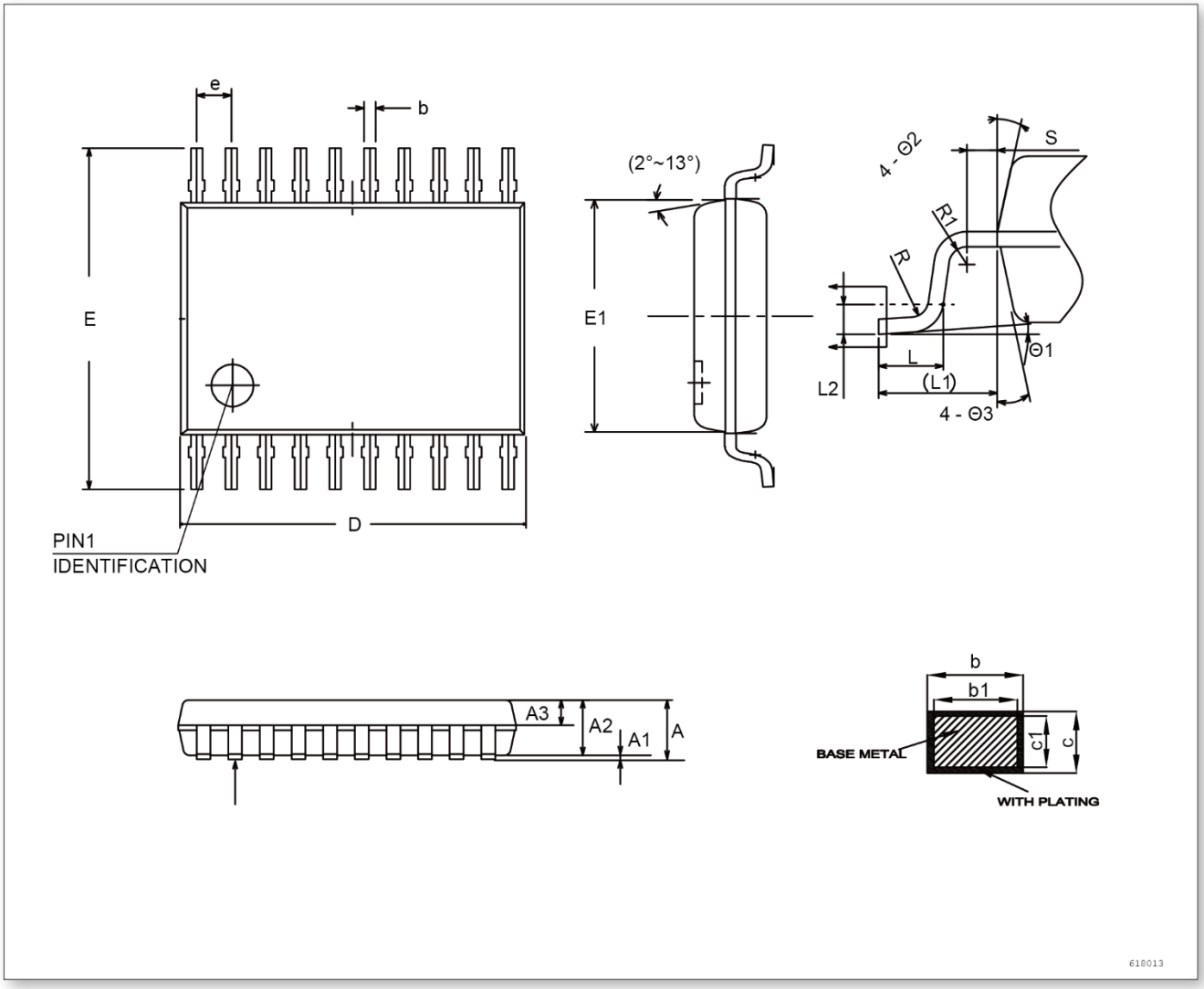

Figure 32 TSSOP20, 20-pin low profile quad flat package

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 45 TSSOP20 dimensions

Symbol	Milimeter		
	Minimum	Typical	Minimum
A	1.0	-	1.10
A1	0.05	-	0.15
A2	-	-	0.95
A3	0.39	-	0.40
b	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	-	0.15
D	6.40	6.45	6.50
E	6.25	6.40	6.55
E1	-	4.35	4.40
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	-	-
θ1	0°	-	8°

6 Product Naming Rule

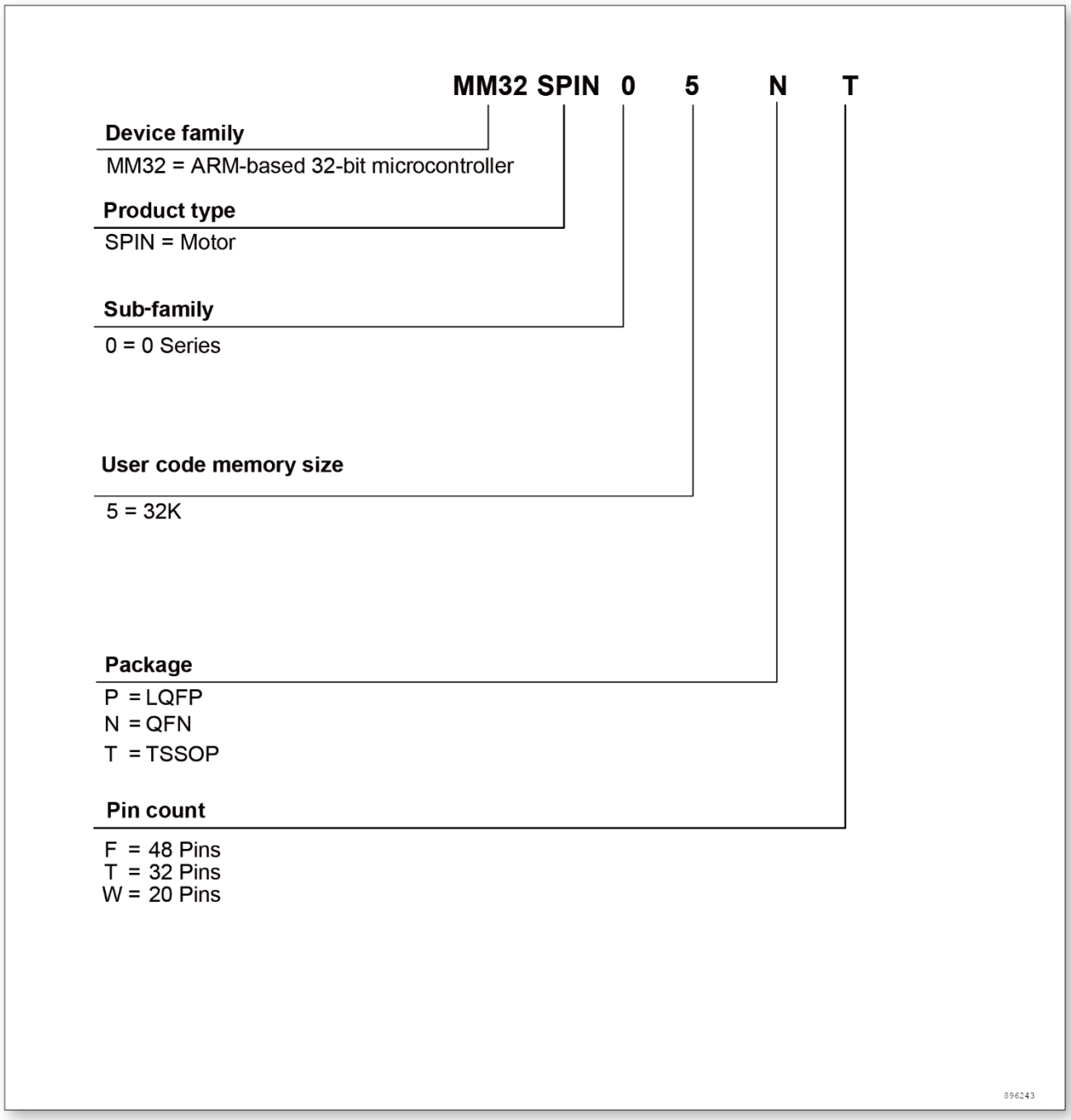

Figure 33 MM32 model naming

7 Revision History

Date	Revision	Description
2018/08/04	Rev1.00	Initial release.
2018/08/26	Rev1.01	Modify pin definition.
2018/10/11	Rev1.02	Modify electrical parameters.
2018/11/12	Rev1.03	Modify descriptions.
2018/11/13	Rev1.04	Modify descriptions.
2018/12/14	Rev1.05	Modify ADC descriptions.
2019/01/07	Rev1.06	Modify ADC voltage parameters.
2019/01/10	Rev1.07	Add the QFN20 package.
2019/03/06	Rev1.08	Modify the package parameters.
2019/03/11	Rev1.09	Modify the package parameters.
2019/05/05	Rev1.10	Modify pin definition.
2019/07/08	Rev1.11	Modify ADC parameters in the selection guide.
2019/07/26	Rev1.12	Modify selection guide.
2020/01/17	Rev1.13	Modify typical current consumption
2020/04/07	Rev1.14	Modify highspeed internal oscillator
2020/05/10	Rev1.15	Modify electrical parameters.
2020/08/27	Rev1.16	Modify AF parameters in the pin definition.
2021/09/08	Rev1.17	Modify IO static characteristics.
2021/09/30	Rev1.18	Modify temperature characteristics.
2021/11/10	Rev1.19	Modify highspeed internal oscillator
2022/01/12	Rev1.20	Modify P_D and add thermal characteristics
2022/01/21	Rev1.21	Modify the maximum value of the voltage characteristics.
2022/06/06	Rev1.22	Update IO parameters; add annoation 1 in table 14; change the NRST figure.
2022/08/24	Rev1.23	Update the parameters of operating
2023/03/06	Rev1.24	Update the electrical characteristics