R61529

16,777,216–Color, 320x480-Dot Graphics Liquid Crystal Controller Driver for TFT Panel

REJxxxxxxx-xxxx
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Description

The R61529 is liquid crystal controller driver LSI for TFT panel sized 320RGB x 480-dot at maximum. For efficient data transfer, the R61529 supports MIPI DSI (1 data lane) and MDDI (Ver.1.2 Type 1, 1 data lane) as system interface to microcomputer. The R61529 also supports MIPI DPI, MIPI DBI (Type B), MIPI DBI (Type C), and I2C.

The R61529 incorporates step-up and voltage follower circuits to generate drive voltage required for a-Si TFT and a dynamic backlight control function to control backlight brightness depending on image data, reducing power consumption at the backlight with the slightest influence on image quality. The R61529 also supports a function which blocks someone's eye by making the display image hard to be seen in order to protect privacy. By synchronizing the moving picture data rewrite operation with VSYNC interface/TE effect, the R61529 can display moving picture without tearing.

Other features include a power management function, making the R61529 best suitable for small-and-mid-sized portable devices with color graphics display such as digital mobile phones, small PDAs and Smartphone.

*MIPI: Mobile Industry Processor Interface, *DCS: Display Command Set, *DSI: Display Serial Interface, *DPI: Display Pixel Interface, *DBI: Display Bus Interface, MDDI: Mobile Display Digital Interface, *VESA: Video Electronics Standards Association, *I2C: Inter-Integrated Circuit.

Note: The MDDI supported by the R61529 is designed and produced based on the licensing of technology from Qualcomm. The MDDI must be adopted in the module, which incorporates a Qualcomm's CDMA ASIC. Any claims, including, but not limited to the third party's right to use the MDDI for industrial purposes shall not be accepted by Renesas Technology unless the above-mentioned condition is met.

Features

- Single chip driver for 16, 777, 216-color TFT 320RGB x 480-dot graphics with LCM power supply circuit
- Resolution: 320RGB x 480 dots
- Panel drive method: Dot inversion and column inversion
- Command set (Compliant with MIPI DCS Version 1.01.00) *DCS: Display Command Set, MDDI
- System interface
  - MIPI DSI (380Mbps/lane @video mode, TBD): 1 data lane/1 clock lane
    MIPI DSI: Version 1.01.00r11 21-Feb-2008 (Command mode and video mode are supported)
    MIPI D-PHY: Version 1.00.00 14-May-2009
  - MIPI DBI Type B 8bits/16bits/18bits/24bits (MIPI DBI Version 2.00)
  - MIPI DBI Type C Option 1/Option 3 (MIPI DBI Version 2.00)
  - MIPI DPI (MIPI DPI Version 2.00)
  - MDDI Ver.1.2 Type 1 (VESA Mobile Display Digital Interface Standard Version 1,2 July 9, 2008)
  - I2C (Inter-Integrated Circuit)

- Video image display interface (see Note 1)
  - TE-I/F (MIPI DBI + TE synchronization signal output)
  - VSYNC-I/F (MIPI DBI + VSYNC)
  - MIPI DSI TE-reporting

- Abundant color display and drawing functions
  - 16,777,216-color display
  - RGB separate γ correction function
  - Partial display function
  - Making the display image hard to be seen (Privacy filter mode)

- Low-power consumption architecture (allowing direct input of interface I/O power supply)
  - Deep standby mode
  - Input power supply voltage:
    Interface power supply: IOVCC1
    Analog and logic power supply: VCI
    MIPI D-PHY/MDDI power supply: IOVCC2

- Dynamic backlight control function
- Internal liquid crystal drive power supply circuit
  - Source driver and VCOM: VSP-GND, VSN-GND
  - DC power supply for VCOM drive: VCOMDC
  - Gate driver power supply: VGH-GND, GND-VGL

- Internal frame memory: 460,800 bytes (320 x 480 x 24 bits)
- Liquid crystal display drive circuits: 960 source signal lines and 480 gate signal lines
- One-chip solution for COG module
- Internal NVM: Data can be rewritten up to 5 times.
- Dummy pins used to fix pin to VCC or GND (see note 2)

Notes: 1. Japanese Patent No. 3,826,159
Korean Patent No. 747,636
United States Patent No. 7,176,870
2. Japanese Patent No. 3,980,066
United States Patent No. 6,323,930
Korean Patent No. 401,270
Taiwan Patent No. 175,413
Japanese Patent No. 4,226,627
United States Patent No. 6,924,868

Power Supply Specification

Table 1 R61529 Power Supply Specification

No.	Item		R61529
1	TFT data lines drive circuit		960 outputs
2	TFT gate lines drive circuit		480 outputs
3	Liquid crystal drive output	S1-S960	V0 ~ V255 grayscales
		G1-G480	VGH-VGL
		VCOMDC	VCOMDC = -0.3V ~ -3.0V
4	Input voltages	IOVCC1 (interface voltage)	1.65V ~ 3.30V (See note 1)
		VCI (power supply voltage for LCD drive)	2.40V ~ 3.30V (See note 1)
		IOVCC2 (MIPI DSI-PHY/MDDI power supply)	2.40V ~ 3.30V (See note 1)
5	System interface (MIPI DBI Type B, MIPI DBI Type C, I2C)	CSX, DCX, WRX, RDX, DIN, DOUT, IM[3:0], RESX, DB23-DB0 (used for DPI, too)	IOVCC1-GND (See note 1)
6	Video image display interface (MIPI DPI)	VSYNC, HSYNC, DE, PCLK, DB23-DB0 (used for DBI, too)	IOVCC1-GND (See note 1)
7	Differential small-amplitude interface	STB_CLKP/N, DATA0P/N,	IOVCC2-GND (See note 2)
8	LED I/F	LEDPWM	IOVCC1-GND (See note 1)
9	LCD drive supply voltages	VSP	4.6V ~ 6.0V
		VSN	-4.6V ~ -6.0V
		VGH	13.0V ～ 20.0V
		VGL	-9.0V ~ -15.0V
		VGH-VGL	Max. 28V

Notes: 1. Connect these power supplies to other power supplies on the FPC when they are set at the same electrical potential as other power supplies.
2. Connect to VCI on the FPC. For voltage, see DC Characteristics in Electrical Characteristics.

Block Diagram

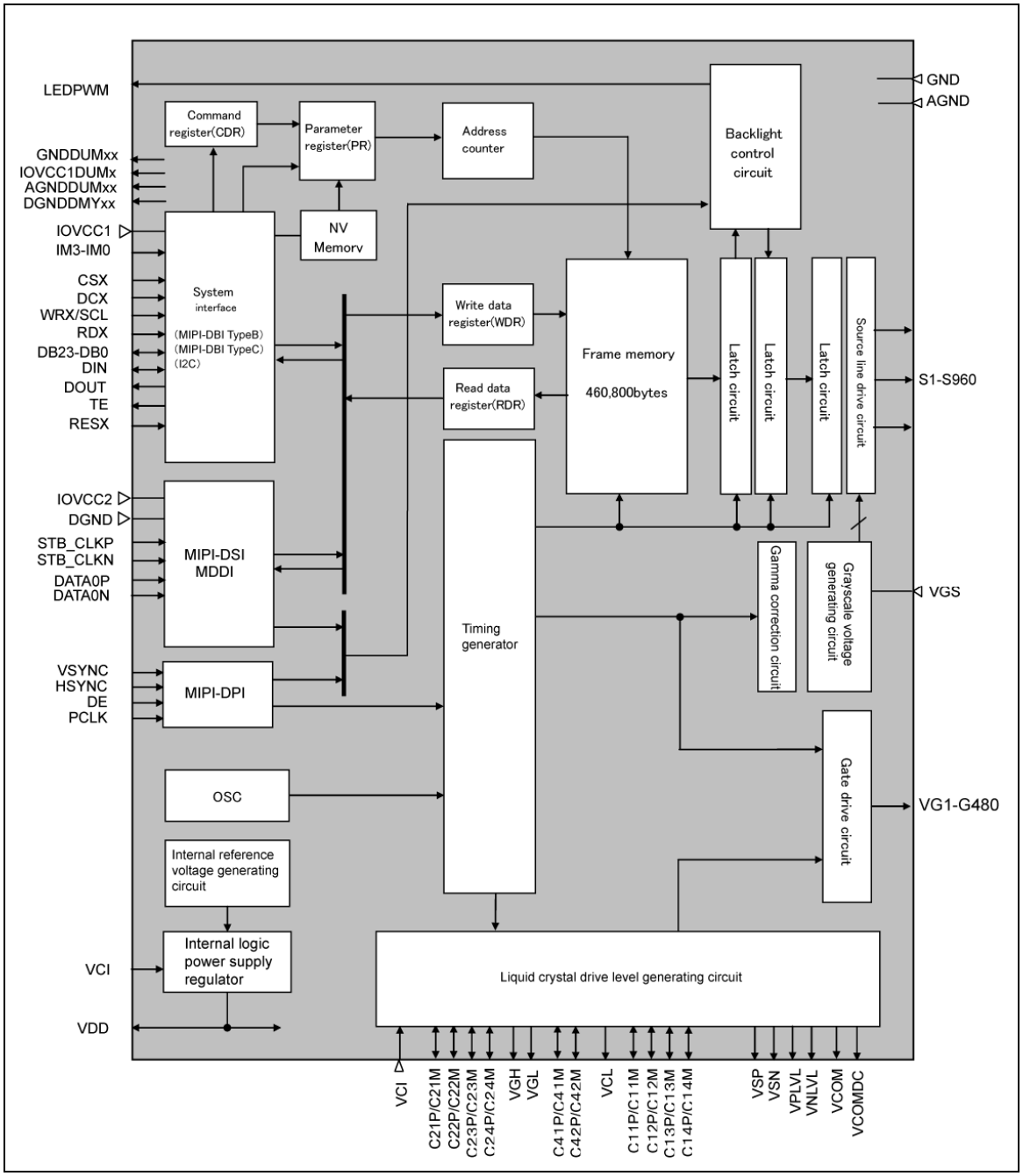


Figure 1

Block Function

1. System Interface

The R61529 supports MIPI DSI (Command Mode and Video Mode), MDDI (Command Mode and Active Refresh Mode), MIPI DBI Type B, MIPI DBI Type C (Option 1 and Option 3), MIPI DPI, and I2C. The R61529 also supports TE synchronization signal and VSYNC interface as display interface for video image.
The interface is selected by setting IM0-3 pins. Using more than one interface set by the IM pins at the same time is inhibited. When MIPI DBI Type C or I2C is selected, display data can be transferred via DPI. When MIPI DBI Type B is selected, display data can be transferred via VSYNC interface. Set the number of available colors using set_pixel_format (3Ah).The interface is selected by setting IM0-3 pins.

Table 2

IM3	IM2	IM1	IM0	Interface	Used pin	Number of available colors
0	0	0	0	I2C (with Noise Cancel Circuit)	DIN	-
0	0	0	1	MIPI DBI Type C 9 bits (Option 1)	DIN, DOUT	-
0	0	1	0	MDDI	DATA0P/N	65,536 / 262,144 / 16,777,216
0	0	1	1	MIPI DSI Command Mode	DATA0P/N	262,144 / 16,777,216
0	1	0	0	MIPI DBI Type B 8 bits	DB7-DB0	65,536 / 262,144 / 16,777,216
0	1	0	1	MIPI DBI Type B 16 bits	DB15-DB0	65,536 / 262,144 / 16,777,216
0	1	1	0	MIPI DBI Type B 18 bits (Note 1)	DB17-DB0	65,536 / 262,144 / 16,777,216
0	1	1	1	MIPI DBI Type B 24 bits (Note 1)	DB23-DB0	65,536 / 262,144 / 16,777,216
1	0	0	0	I2C (with Noise Cancel Circuit) for NVM	DIN	-
1	0	0	1	MIPI DBI Type C 8 bits (Option 3)	DIN, DOUT	-
1	0	1	0	MDDI Active Refresh Mode	DATA0P/N	65,536 / 262,144 / 16,777,216
1	0	1	1	MIPI DSI Video Mode	DATA0P/N	262,144 / 16,777,216
1	1	0	0	Setting inhibited	-	-
1	1	0	1	Setting inhibited	-	-
1	1	1	0	Setting inhibited	-	-
1	1	1	1	Setting inhibited	-	-

Notes: 1. MIPI DBI Type B standard does not define these interfaces.

(a) MIPI DSI

The R61529 supports MIPI DSI (Command Mode and Video Mode).

(b) MIPI DBI Type B

The R61529 supports MIPI DBI Type B (8/16/18/24 bits) that uses command method which has 8-bit command registers and 8-bit parameter registers. Also, the R61529 has a 24-bit write register (WDR) and read register (RDR). The WDR is used to store data temporarily that is automatically written to the internal frame memory through internal operation of the chip. The RDR is used to temporarily store the data read out from the frame memory. When reading data from the frame memory, the R61529 first stores the data in the RDR. For this reason, invalid data is sent to the data bus at first and valid data is sent as the R61529 reads second and subsequent data from the frame memory.

Table 3 Register Selection

DCX	RDX	WRX	Function
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

(c) MIPI DBI Type C (Option 1 and Option 3)

The R61529 supports 9-bit (Option 1) and 8-bit (Option 3) serial interface that uses signals CSX, DCX, WRX/SCL, DIN, and DOUT.

(d) MDDI

The R61529 supports MDDI as a differential small amplitude serial interface for high-speed data transfer via STB_CLKP, STB_CLKN, DATA0P and DATA0N. The number of data lanes can be chosen.

2. Video Image Interface

The R61529 supports TE synchronization signal, DPI, and VSYNC interface as display interface for video image. When DBI is selected, display data is written in synchronization with TE signal which is generated from internal clock to prevent flicker on the panel. When DSI is selected, display data is written in synchronization with a start of the frame period by TE-reporting function. This enables updating image data without flicker on the panel. When DPI is selected, externally supplied VSYNC, HSYNC, and PCLK signals drive the chip. Display data (DB[23:0]) is written in synchronization with those synchronous signals following data enable signal (DE). This enables updating image data without flicker on the panel. The R61529 does not write the display data to the frame memory. In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, i.e. synchronization with the VSYNC signal. The R61529 writes display data to the frame memory via system interface (DBI).

3. Frame Memory

The R61529 incorporates the frame memory that has a capacity of 460,800 bytes, which can store bit-pattern data of 320RGB x 480 graphics display at the maximum using 24 bits to represent one pixel.

4. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltage according to the grayscale setting value in the γ correction register. RGB separate γ correction setting enables maximum 16,777,216-color display.

5. LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates VPLVL, VNLVL, VGH, VGL, VCOMDC levels to drive the liquid crystal panel.

6. Timing Generator

The timing generator is used to generate timing signals for operating internal circuits.

7. Oscillator (OSC)

The R61529 incorporates an oscillator.

8. LCD Driver Circuit

The LCD driver circuit has a 960-channel source driver (S1-S960). When 320RGB pixels of data are input, the display pattern data is latched. The voltage is output from the source driver according to the latched data.

9. Internal Logic Power Supply Regulator

The internal logic power supply regulator generates power supply for the internal logic circuit.

10. Backlight Control Circuit

The backlight control circuit adjusts backlight brightness according to the histogram of image to reduce power consumption at the backlight. Brightness of the backlight and display data is adjusted.

11. NVM

The R61529 supports NVM that stores manufacturer command setting values.

Pin Function

Table 4 External Power Supply Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
VCI	I	Power supply	Power supply to analog circuit. VCI < 0.3V (When power is turned off.)	-
IOVCC1	I	Power supply	Power supply to interface pins. IOVCC1 < 0.3V (When power is turned off.)	-
IOVCC2	I	Power supply	Power supply to MIPI DSI D-PHY and MDDI. Connect to VCI on the FPC to prevent noise in case of COG.	-
GND	I	Power supply	GND for internal logic and interface pins. GND=0V.	-
AGND	I	Power supply	Analog GND (logic regulator and LCD power supply circuit). AGND = 0V. Connect to GND on the FPC to prevent noise in case of COG.	-
DGND	I	Power supply	GND for MIPI DSI D-PHY and MDDI. Connect to GND on the FPC to prevent noise in case of COG.	-

Table 5 System Interface Pins (Amplitude: IOVCC1 - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
IM0, IM1, IM2, IM3	I	IOVCC1 or GND	Interface select signal. Select interface from MIPI DSI, MIPI DBI Type B, MIPI DBI Type C (Option 1 and Option 3), MDDI, I2C, and MIPI DPI. See “Block Function.”	-
RESX	I	Host Processor or external RC circuit	Reset pin. The R61529 is initialized when RESX is Low. Make sure to execute power-on reset when turning power supply on.	-
TE	O	Host processor	Tearing effect output signal.	Open

Table 6 MIPI DBI Type B/MIPI Type C/I2C Pins (Amplitude: IOVCC1 - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
CSX	I	Host Processor	Chip select signal. Low: Select (Accessible) High: Not Select (Inaccessible) Make sure to connect to the host processor and control following AC characteristics. This pin can be High or Low when using I2C/MDDI.	IOVCC1
DCX	I	Host Processor	Command/data select signal. Low: Select command High: Select data This pin can be High or Low when using I2C/MDDI/MIPI-DSI/MIPI DBI Type C.	IOVCC1
WRX / SCL	I	Host Processor	Write strobe signal in MIPI DBI Type B operation When WRX is Low, write data. A synchronous clock signal in MIPI TDBI Type C and I2C operation. This pin can be High or Low when using MDDI/MIPI-DSI.	IOVCC1
RDX	I	Host Processor	Read strobe signal. Read out data when RDX is Low. This pin can be High or Low when using I2C/MDDI/MIPI DSI/MIPI DBI Type C.	IOVCC1
DB23-0	I/O	Host Processor	In MIPI DBI Type-B operation. 8-bit interface: Use DB7-0 16-bit interface: Use DB15-0 18-bit interface: Use DB17-0 24-bit interface: Use DB23-0 DPI operation Use DB23-0 Abnormal current (through current) does not occur when CSX is High and the data bus is Hi-Z.	IOVCC1 or GND
DIN	I/O	Host Processor	A serial data input pin in MIPI Type C operation to input data on the rising edge of the SCL signal. A serial input/output and ACK output pin in I2C operation.	IOVCC1 or GND
DOUT	O	Host Processor	A serial data output pin in MIPI DBI Type C operation to input data on the rising edge of the SCL signal.	IOVCC1 or GND

Table 7 MIPI DPI Pins (Amplitude: IOVCC1 - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
VSYNC	I	Host Processor	Flame synchronous signal in MIPI DPI operation. Low Active.	IOVCC1
HSYNC	I	Host Processor	Line synchronous signal in DPI operation. Low Active.	IOVCC1
DE	I	Host Processor	Data Enable signal in MIPI DPI operation. Low: Not select (inaccessible) High: Select (accessible)	IOVCC1
PCLK	I	Host Processor	Pixel clock signal in MIPI DPI operation.	IOVCC1 or GND

Table 8 MIPI DSI Pins (Amplitude: IOVCC2 - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
STB_CLKP	I	Host Processor	MIPI DSI Clock / MDDI strobe signal line (+).	DGND
STB_CLKN	I	Host Processor	MIPI DSI Clock / MDDI strobe signal line (-).	DGND
DATA0P	I/O	Host Processor	MIPI DSI / MDDI data-0 signal lines (+).	DGND
DATA0N	I/O	Host Processor	MIPI DSI / MDDI data-0 signal line (-).	DGND

Table 9 LED Driver Control Pins (Amplitude: IOVCC1 -GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
LEDPWM	O	LED driver	Control signal for brightness of LED backlight. PWM signal's width is selected from 256 values between 0% (Low) and 100% (High). When light is turned on, LEDPWM is High. When light is turned off, LEDPWM is Low.	Open

Table 10 Power Supply Circuit Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
VDD	O	Stabilizing capacitor	Outputs from internal logic power supply regulator. Connect to stabilizing capacitor.	-
VGH	O	Liquid crystal panel	Liquid crystal drive power supply. Pin to output voltage from positive side of liquid crystal panel. Sleep mode: VCI NVM write/erase operation: about 9V Display on sequence and display operation: VGH (according to VC2[2:0] setting)	-
VGL	O	Liquid crystal panel	Liquid crystal drive power supply. Pin to output voltage from negative side of liquid crystal panel. Sleep mode: GND NVM write/erase operation: about -9V Display on sequence and display operation: VGL (according to VC2[2:0] and VC3[2:0] setting)	-
C11P, C11M, C12P, C12M C13P, C13M, C14P, C14M	I/O	Step-up capacitor	Capacitor connection pins to generate VSP and VSN with a circuit. For details, see “Power Supply Generating Circuit.”	Open
C21P, C21M, C22P, C22M C23P, C23M, C24P, C24M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit. For details, see “Power Supply Generating Circuit.”	-
C41P, C41M, C42P, C42M	I/O	Step-up capacitor	Connect to external capacitor for generating VCL. For details, see “Power Supply Generating Circuit.”	-
VCL	O	Liquid crystal panel	Used for VSN reference voltage.	-

Table 11 Liquid Crystal Drive Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
VCOMDC	O	Stabilizing capacitor	VCOMDC level, which is set by internal electronic volume. Do not use VCOMDC as VCOM that supplies voltage to liquid crystal panel.	-
VCOM	O	Liquid crystal display	VCOM level, which is supplied to liquid crystal panel.	-
VGS	I	AGND	Reference level of the grayscale voltage generating circuit (GND level).	-
VSN	O	Stabilizing capacitor	Negative step-up voltage for source drivers and gamma circuit.	-
VSP	O	Stabilizing capacitor	Positive step-up voltage for source drivers and gamma circuit.	-
VPLVL	O	Liquid crystal panel	Reference voltage for liquid crystal display at positive side.	-
VNLVL	O	Liquid crystal panel	Reference voltage for liquid crystal display at negative side.	-
S1-S960	O	Liquid crystal panel	Liquid crystal application voltages.	Open
G1-G480	O	Liquid crystal display	Gate line output signals. VGH: Gate line is selected. VGL: Gate line is not selected.	Open

Table 12 Other Pins (Test and Dummy)

Signal	I/O	Connect to	Function	Connection when signal is unused
VREFC	I	GND	Test pin. Connect to GND.	-
VREF	O	Open	Test pin. Leave open.	Open
VREFM	O	Open	Test pin. Leave open.	Open
VREFD	O	Open	Test pin. Leave open.	Open
VDDTEST	I	GND	Test pin. Connect to GND.	-
GNDDUM1-xx, IOVCCDUM1-xx AGNDDUM1-xx	O	—	Used to fix electric potential. Connect to unused interface or test pins to fix electric potential on the glass. If not, leave open.	-
DGNDDMY1-xx	I/O	Open or GND	If MIPI DSI/MDDI is selected, draw the wire on to FPC and fix at GND. If MIPI DSI/MDDI is not selected, they are used to fix STB_CLKP/N and DATA0P/N pins to GND.	-
DUMMYR1-4	O	Open	Dummy pins to measure contact resistance. DUMMYR1 and DUMMYR2, and DUMMYR3 and DUMMY4 are short-circuited within the LSI.	Open
TEST1-4	I	GND	Test pins. Connect to GND.	-
TESTE	I	GND	Test pins. Connect to GND	-
TSC	I	GND	Test pin. Connect to GND.	-
VPP1	I	GND	Test pin. Connect to GND.	-

Pad Arrangement (T.B.D.)

Pad Coordinates (T.B.D.)

BUMP Arrangement (T.B.D.)

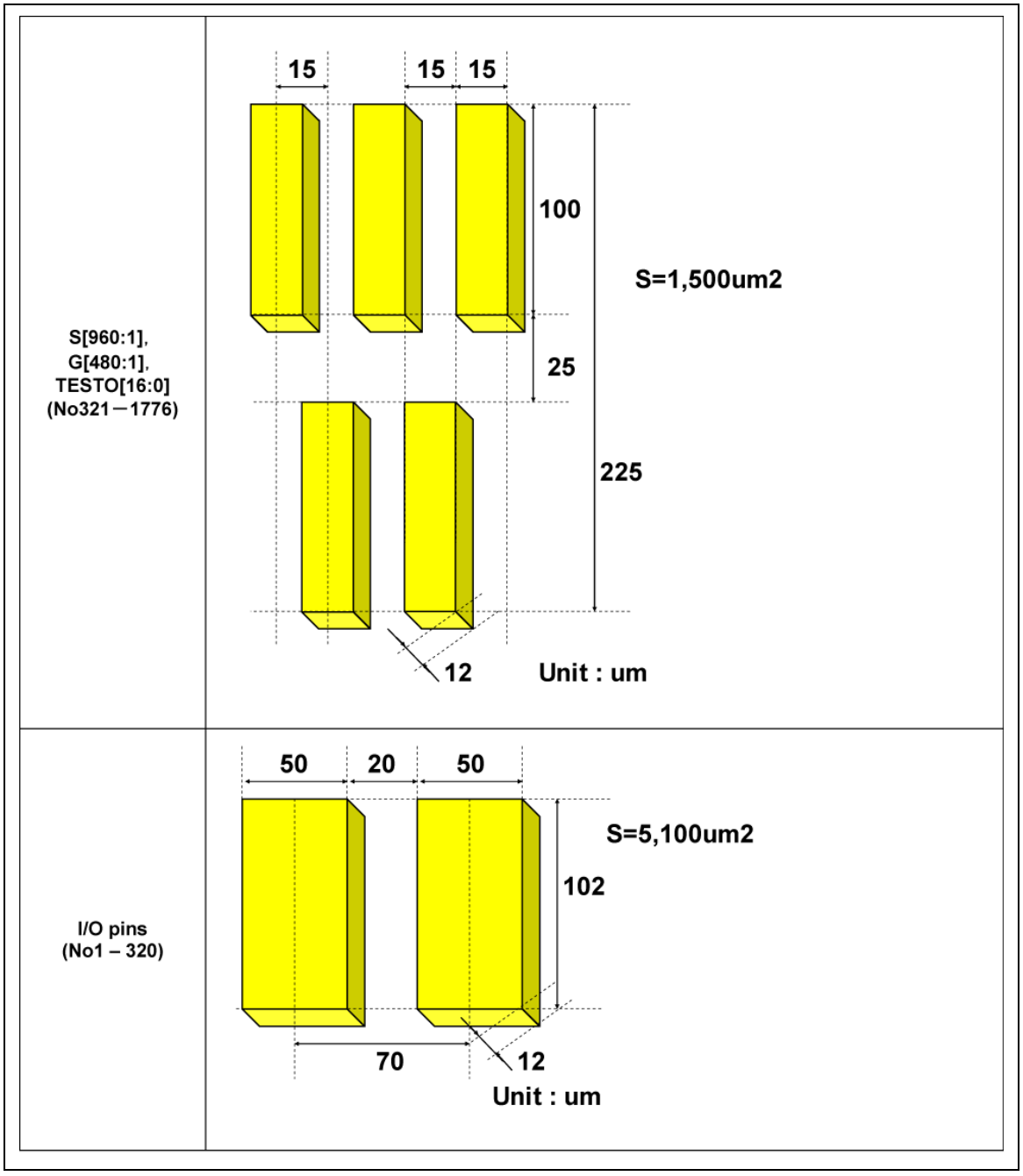


Figure 2

Alignment Mark (T.B.D.)

- Chip size: xx.x × x.x mm
- Chip thickness: 280 mm
- Pad coordinates: Pad center
- Coordinate origin: Chip center
- Au bump pitch: Refer to “Pad Coordinate.”
- Au bump height: 12um
- Alignment mark coordinate

Alignment mark	X	Y
(1-a)	-xxxxx.x	-xxx.x
(1-b)	xxxxx.x	-xxx.x

- Alignment mark

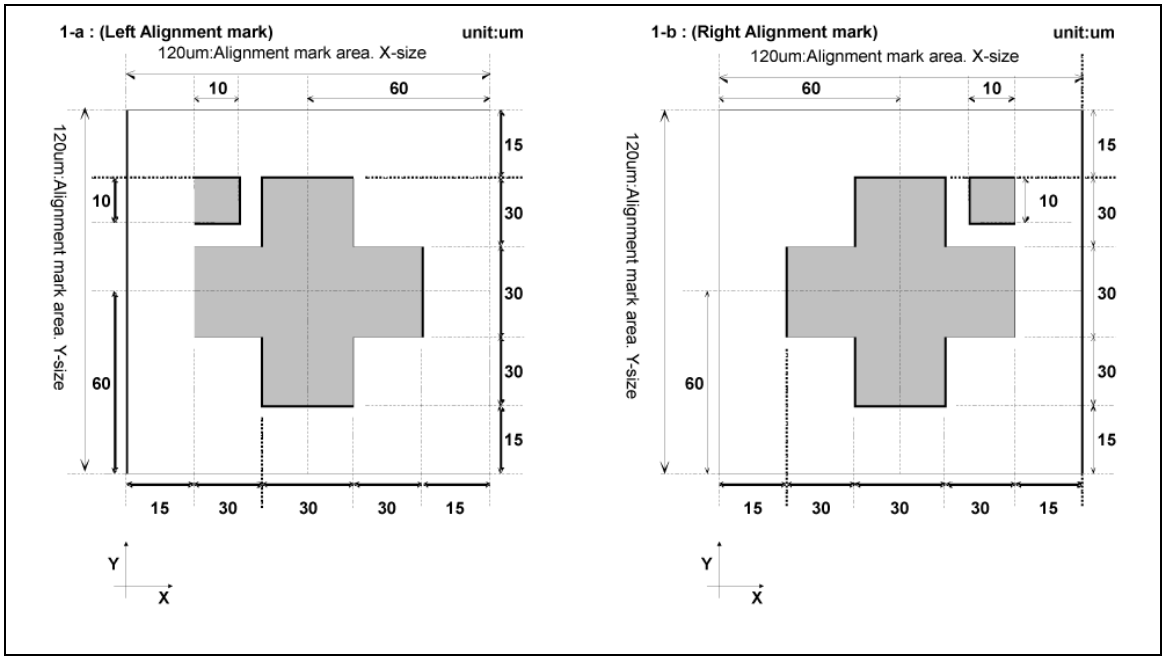


Figure 3

Recommended Resistance and Wiring Example (T.B.D.)

System Interface Configuration (MIPI DBI Type B)

Outline

The R61529 adopts 24-/18-/16-/8-bit bus display command interface to interface to high-performance host processor. The R61529 starts internal processing after storing control information of externally sent 24-/18-/16-/8-bit data in the command register (CDR) and the parameter register (PR). Since the internal operation of the R61529 is determined by signals sent from the host processor, command/parameter signal, read/write status signal (RDX/WRX), and internal 24-bit data bus signals (DB[23:0]) are called command.

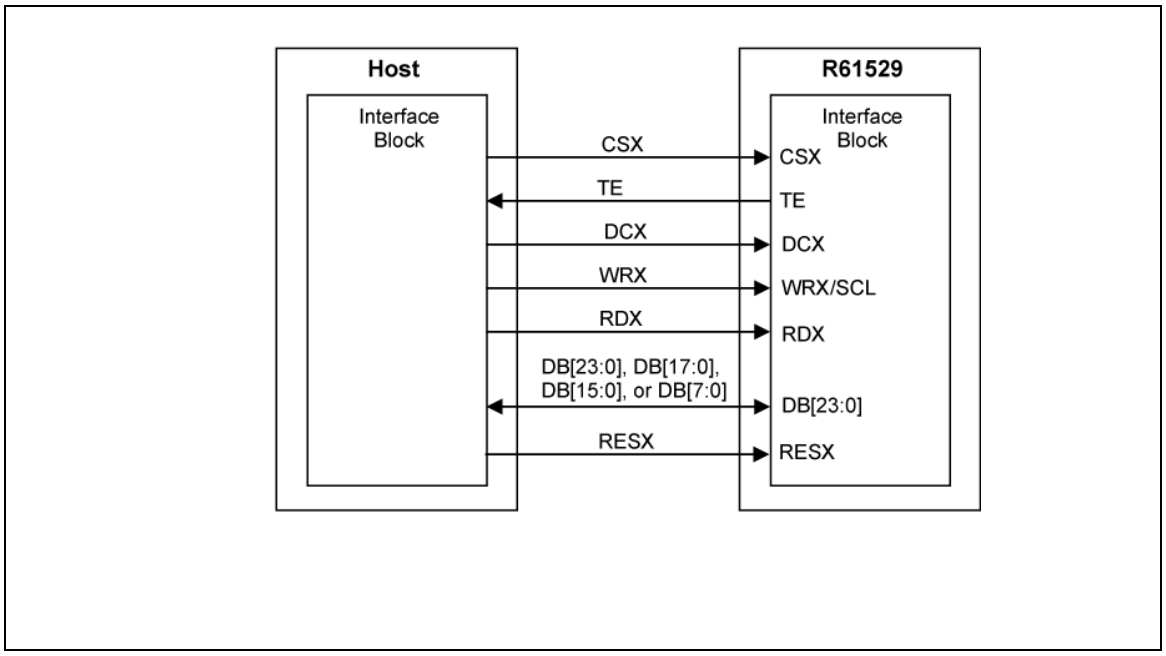
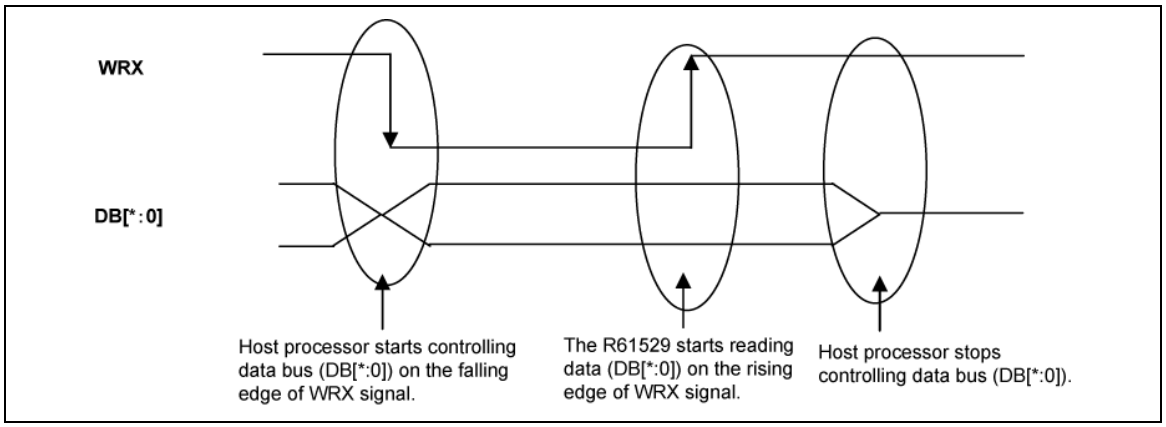


Figure 4 Example of DBI Type B

Write Cycle Sequence

In write cycle, data and/or command are written to the R61529 via the interface between the R61529 and the host processor. Each step of write cycle sequence (WRX high, WRX low, WRX high) comprises three control signals (DCX, RDX, WRX) and 24(DB[23:0])-bit data. The DCX bit indicates signal that is used to select command or data sent on the data bus.

When DCX = 0, data on DB[7:0] is command. When DCX="1", data on DB[15:0] is command parameter and data on DB[23:0] is image data. Setting RDX and WRX to "Low" simultaneously is prohibited. See the figure below for the write cycle sequences.



Note: WRX is not a synchronous signal (can be halted).

Figure 5 Write Cycle Sequence

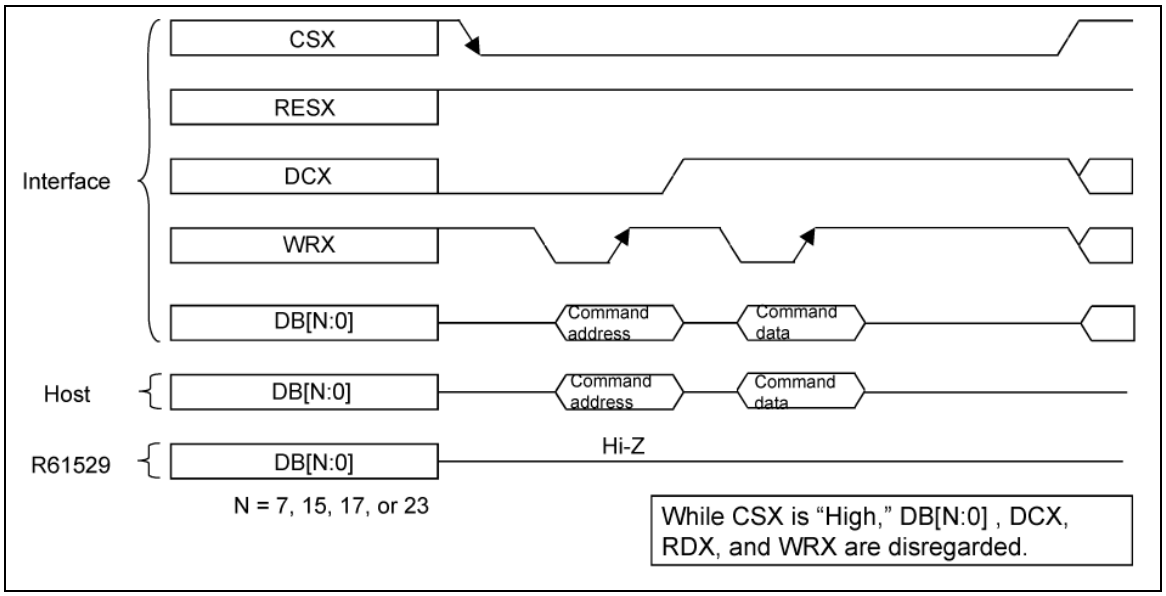
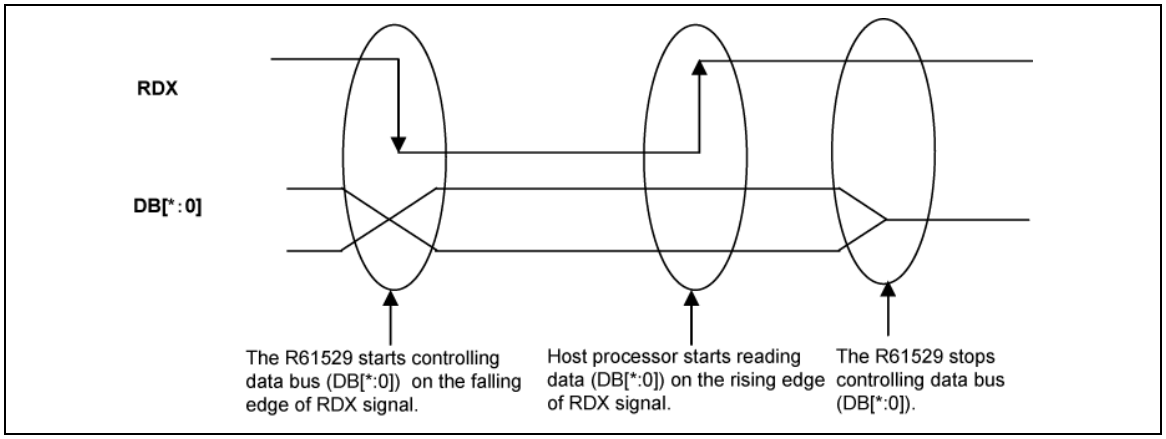


Figure 6 Write Cycle Sequence

Read Cycle Sequence

In read cycle, data and/or commands are read from the R61529 via the interface between the R61529 and the host processor. The data (DB[23:0], DB[17:0], DB[15:0], or DB[7:0]) are transmitted from the R61529 to the host processor on the falling edge of RDX. The host processor reads the data on the rising edge of RDX. Setting RDX and WRX to Low simultaneously is prohibited. See below for the write cycle sequence.



Note: RDX is not a synchronous signal (can be halted).

Figure 7 Read Cycle Sequence

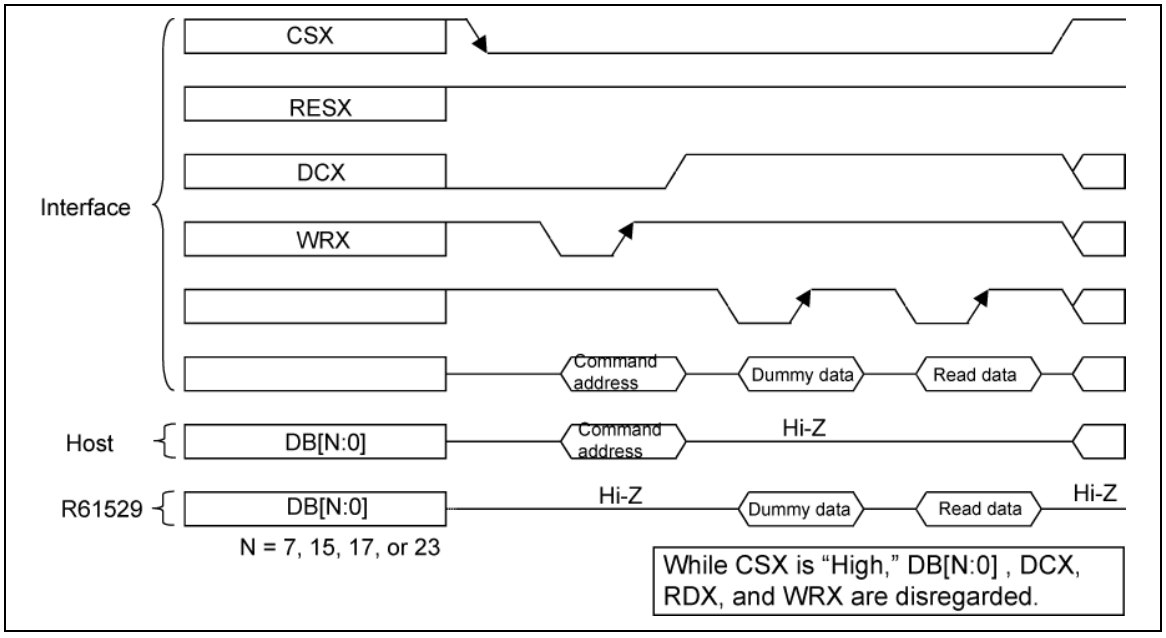


Figure 8 Read Cycle Sequence

Data Transfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the R61529, the command parameters sent to the R61529 before the break occurs are stored in the register of the R61529 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the R61529. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs. However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

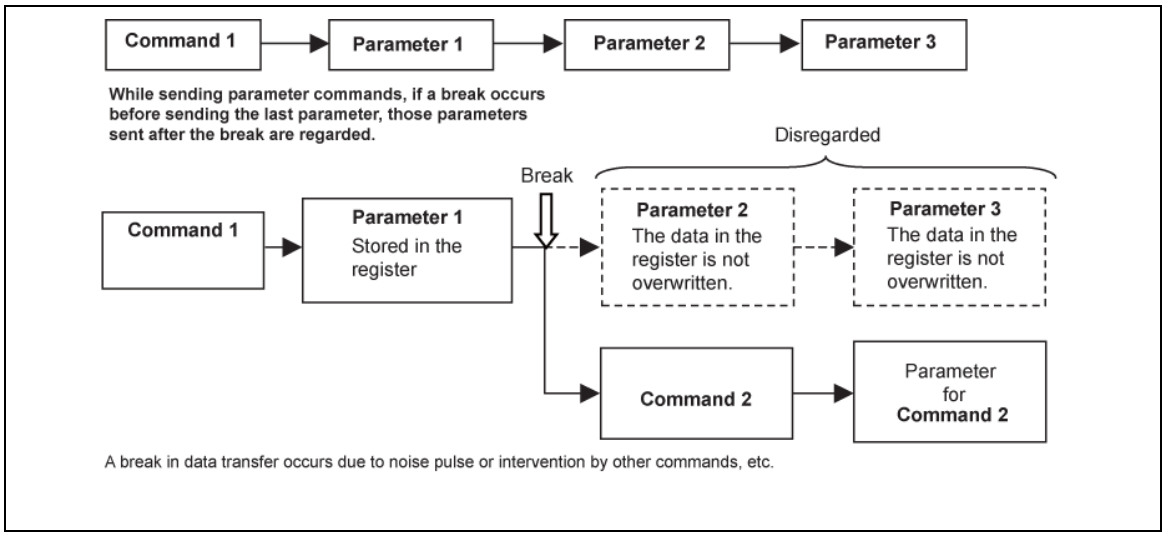


Figure 9

Data Transfer Pause (Command/Pause/Command)

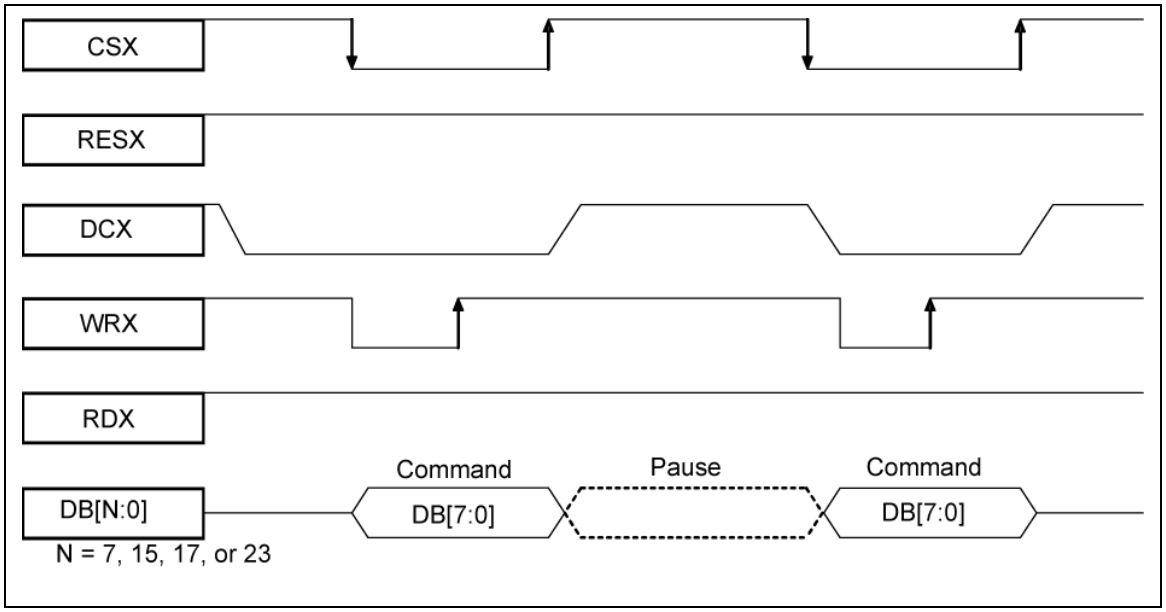


Figure 10

Data Transfer Pause (Command/Pause/Parameter)

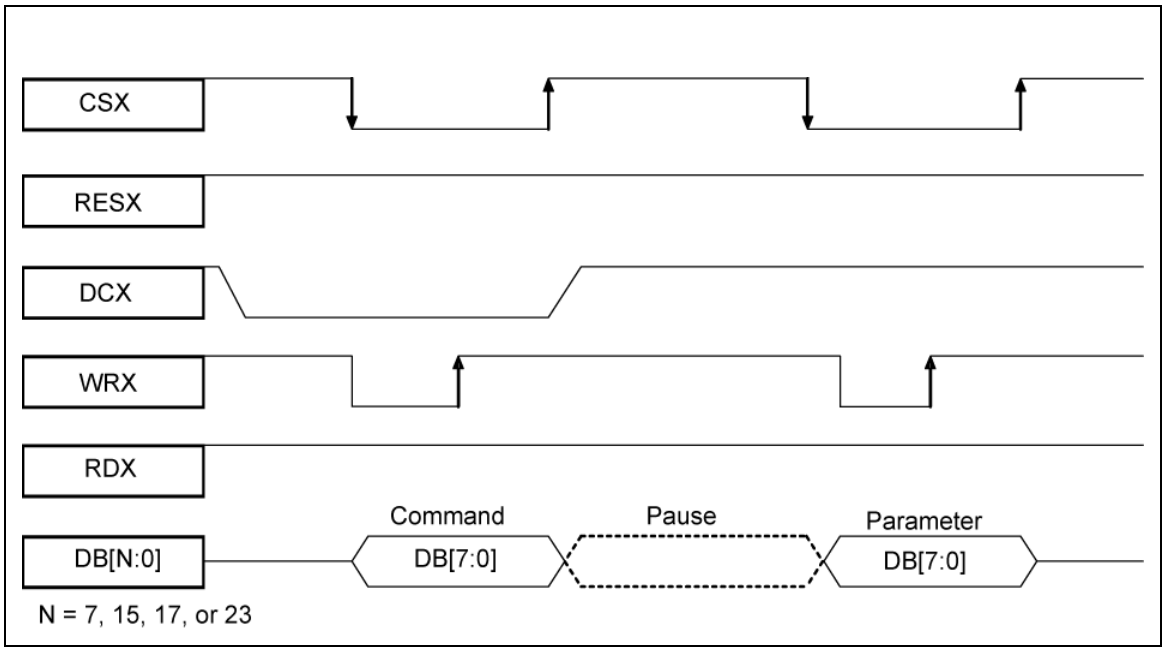


Figure 11

Data Transfer Pause (Parameter/Pause/Command)

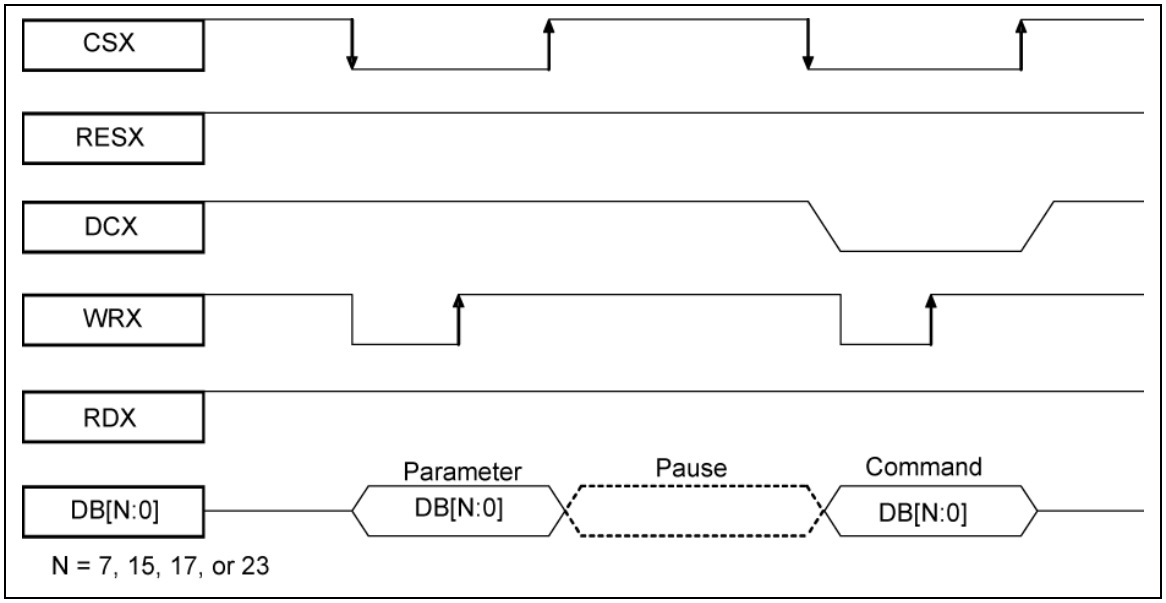


Figure 12

Data Transfer Pause (Parameter/Pause/Parameter)

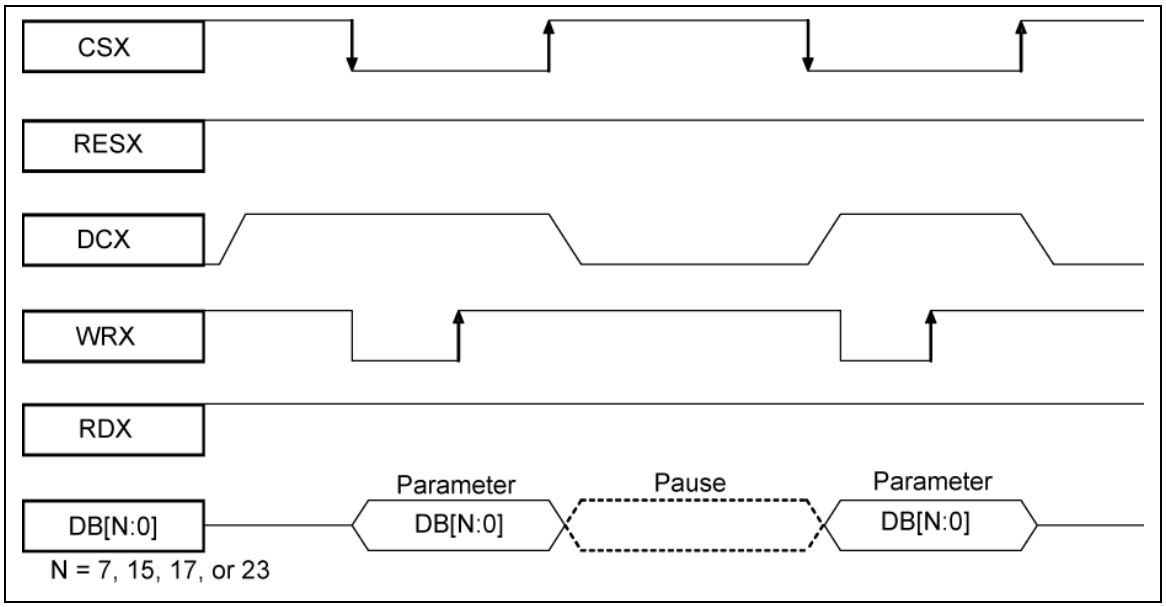


Figure 13

Data Transfer Mode

Two methods are available for writing data to the frame memory in the R61529.

Write Method 1 (Default)

One frame of image data is written to the frame memory. The amount of the transmitted data is over 1 frame, the data are disregarded. The write operation of the data to the frame memory is terminated when a command intervenes in the middle of the course. The R61529 writes the image data to the next frame when write_memory_start command (2Ch) is written. Set WEMODE =0 (Frame Memory Access and Interface Setting (B3h)).

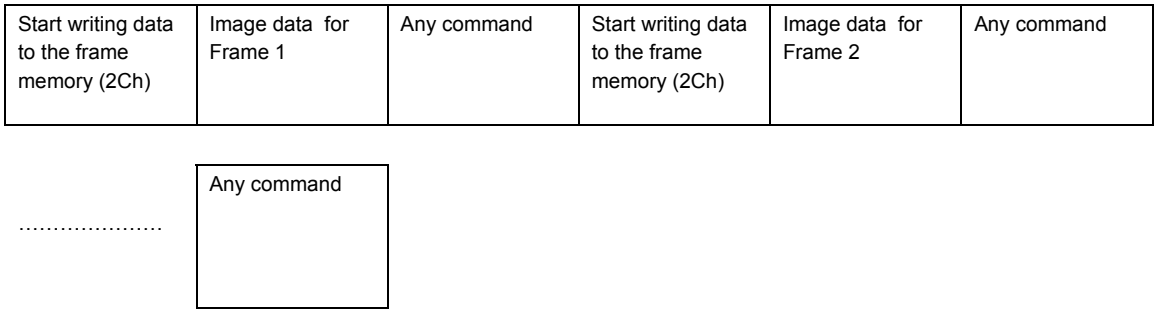


Figure 14

Write Method 2

The image data are written consecutively to the frame memory. The frame memory pointer is reset to the start point when the frame memory becomes full and the driver starts writing the image data of the next frame. Set WEMODE =1 (Frame Memory Access and Interface setting (B3h)).

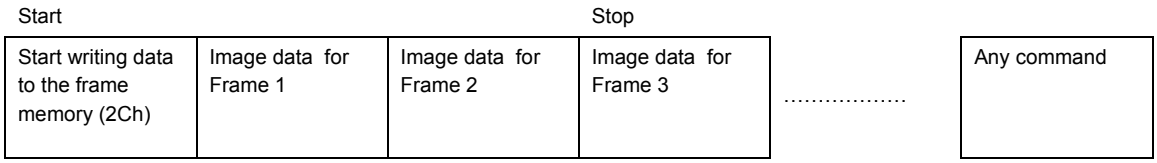


Figure 15

Notes: 1. Two write methods are available for all data transfer color modes in 16-/8-bit bus display command interface.

2. The number of pixel in one frame can be odd or even in both download methods. Only complete data sets are retained in the frame memory.
3. The data write operation to the frame memory is terminated when a command intervenes in the middle of the course. In this case, if write_memory_continue (3Ch) is executed, the write operation can be started again from the address where the write operation is halted.

DBI Type B Data Format

The R61529 supports color formats shown below.

Table 13

Type	IM3-0	Data pin	Color format	MIPI Spec.	R61529 implementation
Type B	0111	DB[23:0]	16bpp	No	Yes
			18bpp	No	Yes
			24bpp	No	Yes
	0110	DB[17:0]	16bpp	No	Yes
			18bpp	No	Yes
			24bpp	No	Yes
	0101	DB[15:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp (262,144-color Option1)	Yes	Yes
			18bpp (262,144-color Option2)	Yes	Yes
			24bpp (16,777,216-color Option1)	Yes	Yes
			24bpp (16,777,216-color Option2)	Yes	Yes
	-	DB[8:0]	18bpp	Yes	No
	0100	DB[7:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	No
			18bpp	Yes	Yes
			24bpp	Yes	Yes

Yes: Supported

No: Unsupported

1. 24-Bit Bus Interface

(a) Command/Parameter Write

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 16

(b) Command/Parameter Read

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 17

The first Command/Parameter Read after read command is issued is invalid. (Dummy read)

(c) 24bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h7. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 18

(d) 18bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h6. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 19

(e) 16bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h5. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 20

(f) 24bpp Frame Memory Read

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

Figure 21

2. 18-Bit Bus Interface [IM3-0 = 0110]

(a) Command/Parameter Write

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 22

(b) Command/Parameter Read

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 23

The first Command/Parameter Read after read command is issued is invalid. (Dummy read)

(c) 24bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h7. DFM = *.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st transfer									R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]
2nd transfer									B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	R2[7]	R2[6]	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]
3rd transfer									G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]

Figure 24

The first pixel data is written to frame memory after the 2nd transfer. If data transfer stops after the 2nd transfer, the first pixel data are written normally. This applies to the last address when the number of pixels is odd according to window setting.

(d) 18bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h6. DFM = *.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 25

(e) 16bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h5. DFM = *.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 26

(f) 24bpp Frame Memory Read

set_pixel_format (3Ah) = 3'h*. DFM = *.

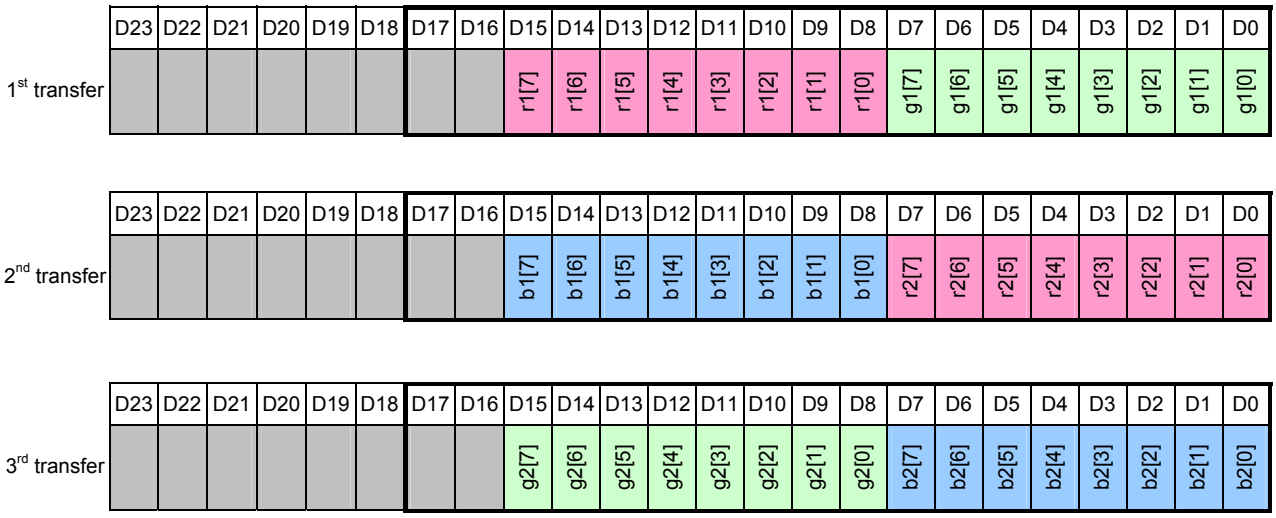


Figure 27

3. 16-Bit Bus Interface [IM3-0 = 0101]

(a) Command/Parameter Write

set_pixel_format (3Ah) = *. DFM = *.

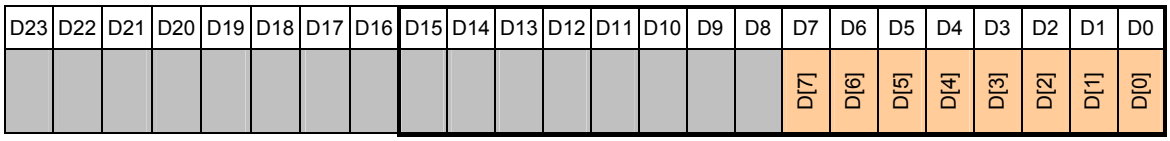


Figure 28

(b) Command/Parameter Read

set_pixel_format (3Ah) = *. DFM = *.

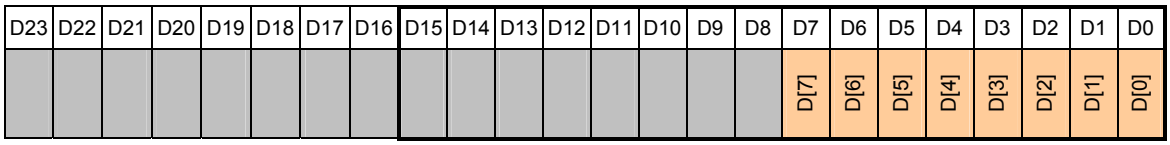


Figure 29

The first Command/Parameter Read after read command is issued is invalid. (Dummy read)

(c) 24bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h7. DFM = 0.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st transfer									R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]
2nd transfer									B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	R2[7]	R2[6]	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]
3rd transfer									G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]

Figure 30

The first pixel data is written to frame memory after the 2nd transfer. If data transfer stops after the 2nd transfer, the first pixel data are written normally. This applies to the last address when the number of pixels is odd according to window setting.

(d) 24bpp Frame Memory Write (Option 2)

set_pixel_format (3Ah) = 3'h7. DFM = 1.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st transfer																	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]
2nd transfer									G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 31

Data are written to the Frame Memory when data for one pixel are input.

(e) 18bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h6. DFM = 0.

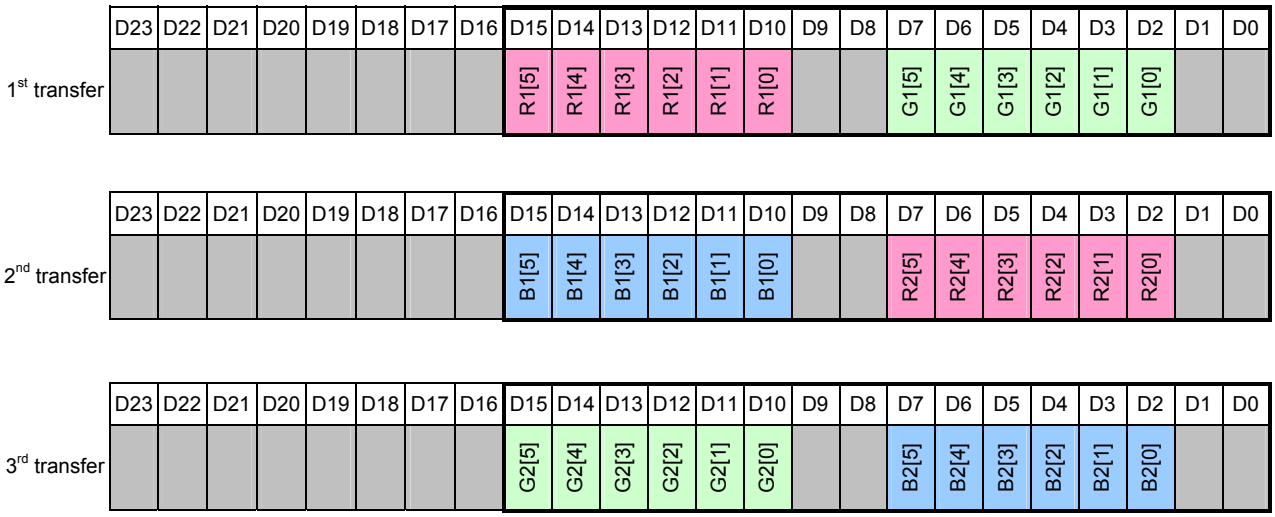


Figure 32

The first pixel data is written to frame memory after the 2nd transfer. If data transfer stops after the 2nd transfer, the first pixel data are written normally. This applies to the last address when the number of pixels is odd according to window setting.

(f) 18bpp Frame Memory Write (Option 2)

set_pixel_format (3Ah) = 3'h6. DFM = 1.

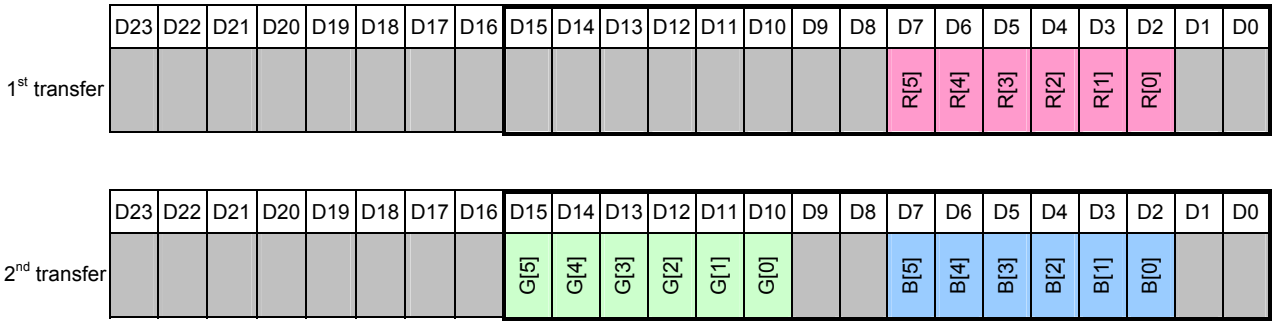


Figure 33

Data are written to the Frame Memory when data for one pixel are input.

(g) 18bpp Frame Memory Write (Option 3)

set_pixel_format (3Ah) = 3'h6. DFM = 2.

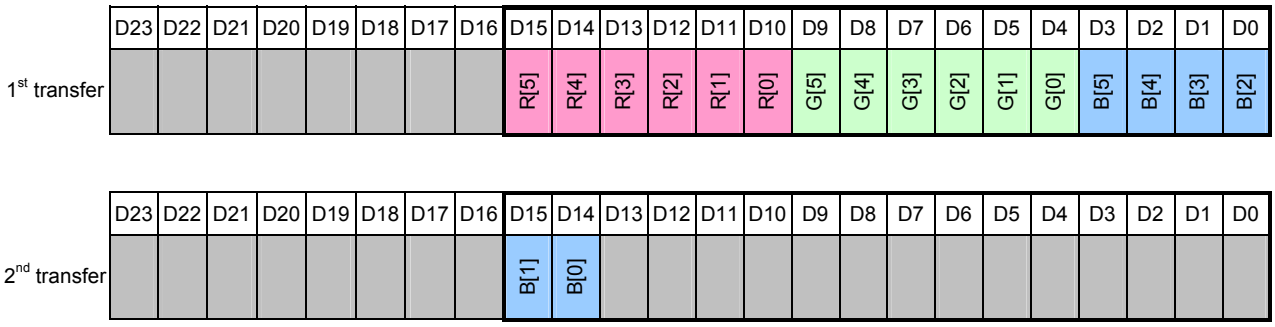


Figure 34

Data are written to the Frame Memory when data for one pixel are input.

(h) 16bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h5. DFM = *.

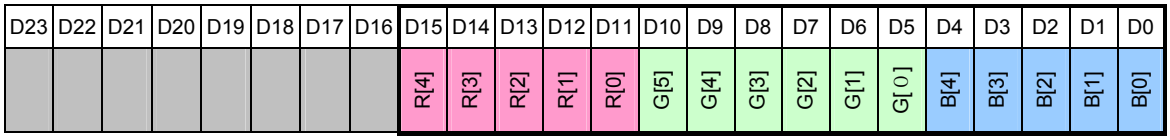


Figure 35

(i) 24bpp Frame Memory Read

set_pixel_format (3Ah) = *. DFM = 0.

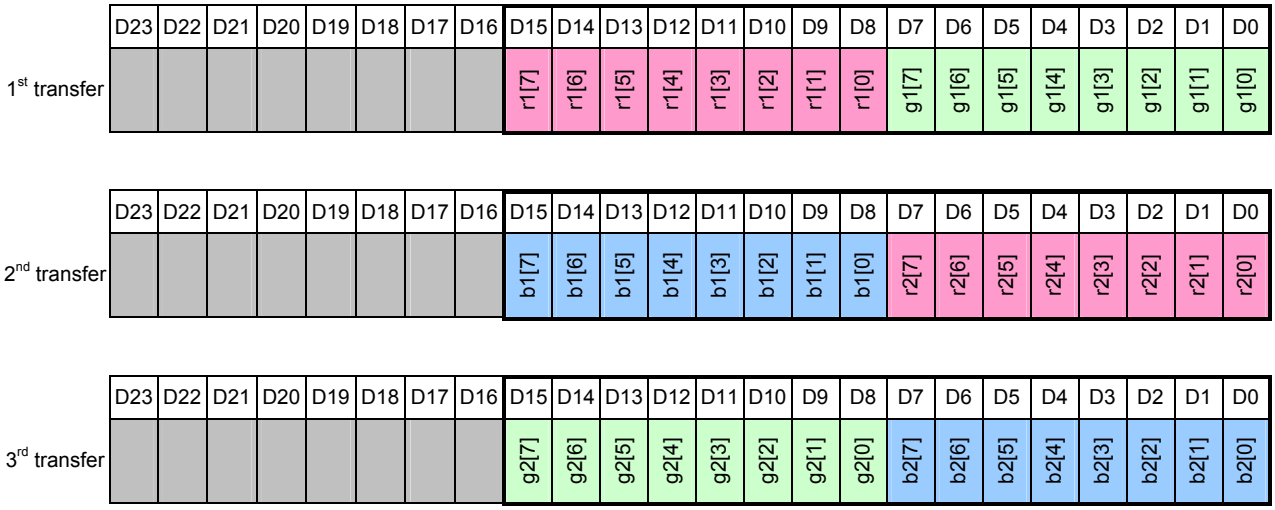


Figure 36

(j) 24bpp Frame Memory Read

set_pixel_format (3Ah) = *. DFM = 1.

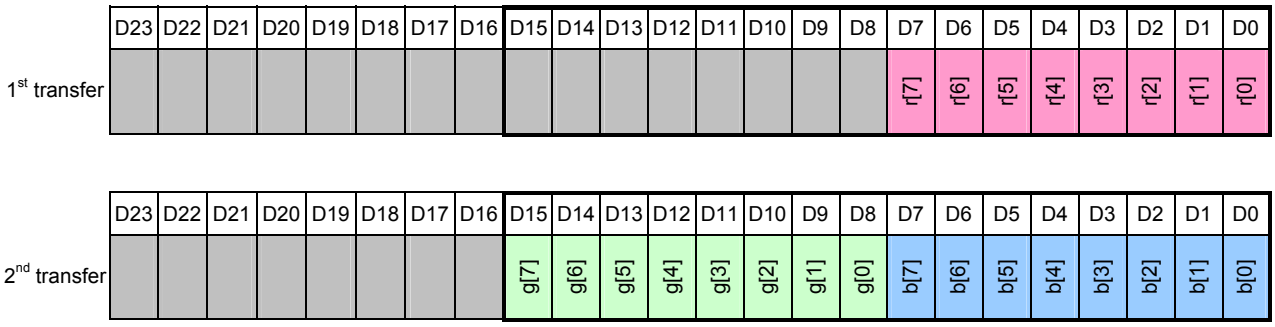


Figure 37

4. 8-Bit Bus Interface [IM3-0 = 0100]

(a) Command/Parameter Write

set_pixel_format (3Ah) = *. DFM = *.

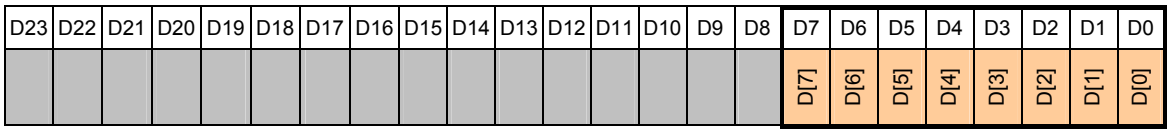


Figure 38

(b) Command/Parameter Read

set_pixel_format (3Ah) = *. DFM = *.

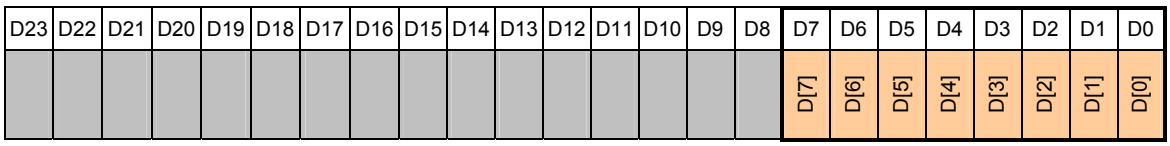


Figure 39

The first Command/Parameter Read after read command is issued is invalid. (Dummy read)

(c) 24bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h7. DFM = *.

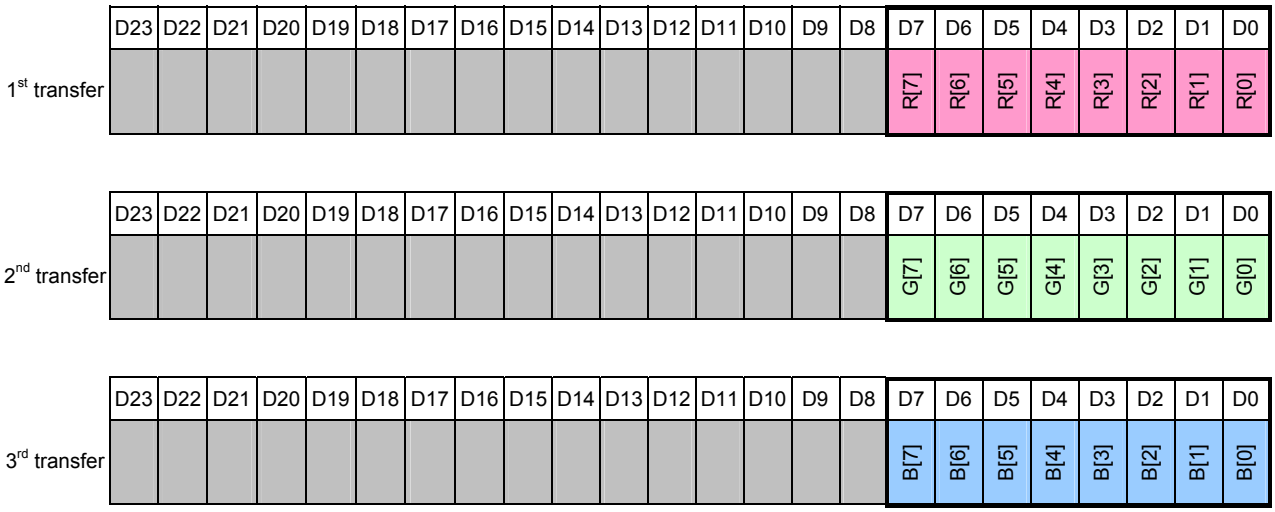


Figure 40

(d) 18bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h6. DFM = 0.

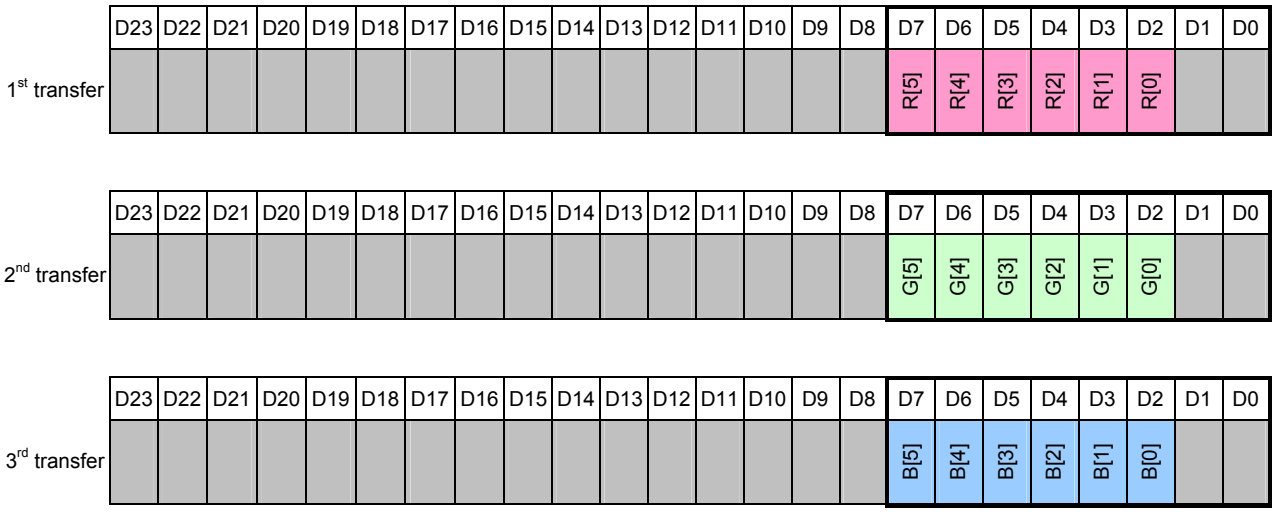


Figure 41

(e) 18bpp Frame Memory Write (Option 2)

set_pixel_format (3Ah) = 3'h6. DFM = 1.

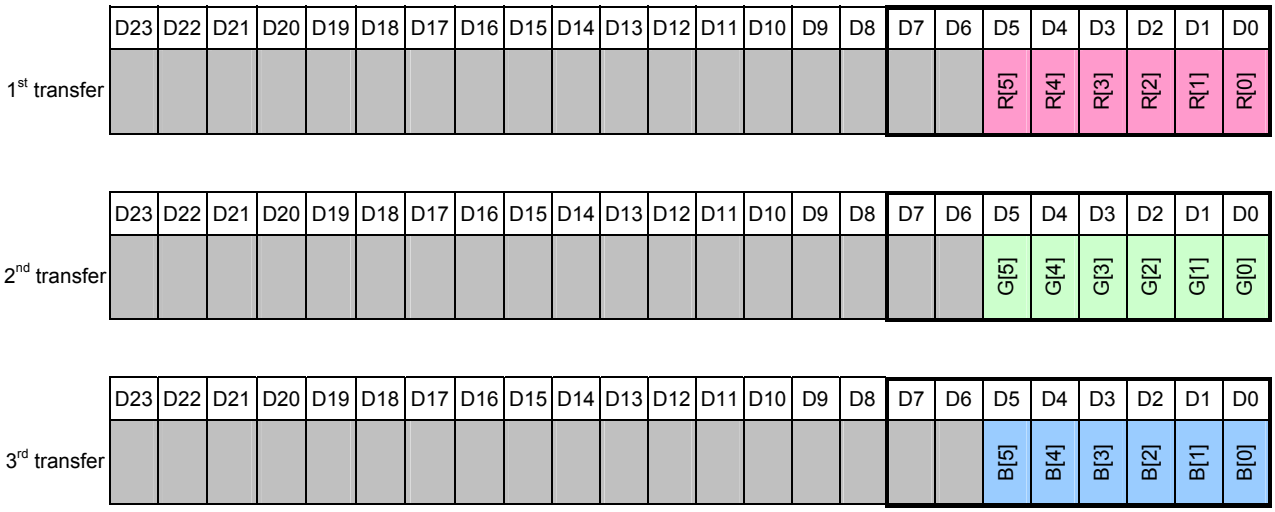


Figure 42

(f) 16bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h5. DFM = 0.

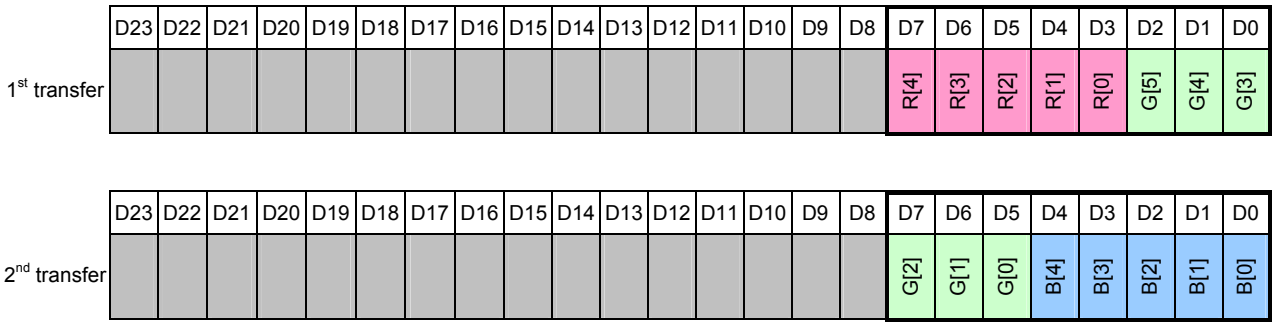


Figure 43

(g) 16bpp Frame Memory Write (Option 2)

set_pixel_format (3Ah) = 3'h5. DFM = 1.

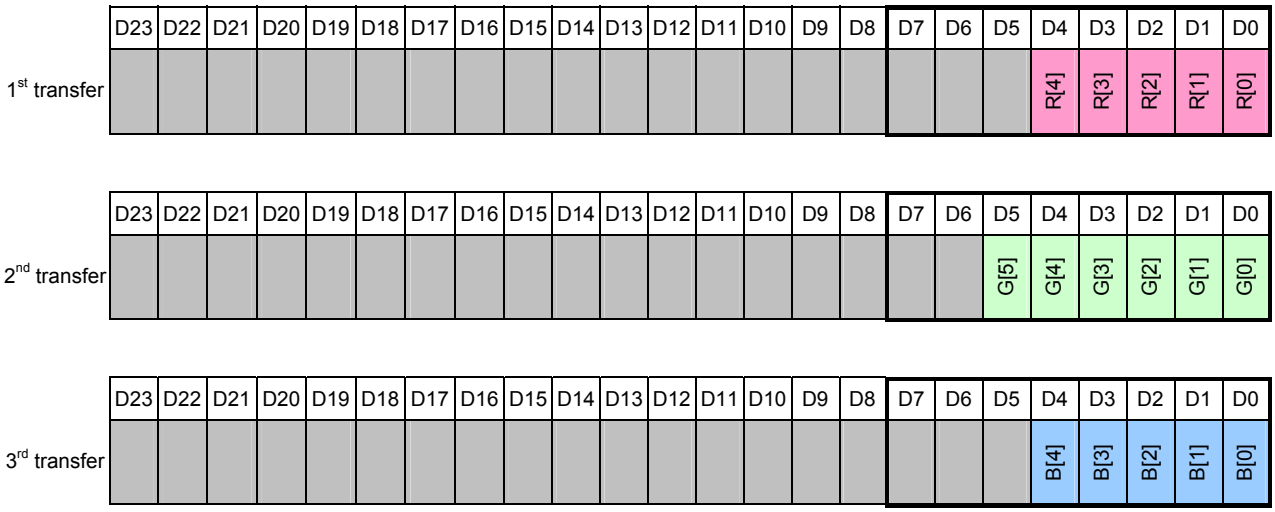


Figure 44

(h) 24bpp Frame Memory Read

set_pixel_format (3Ah) = 3'h*. DFM = *.

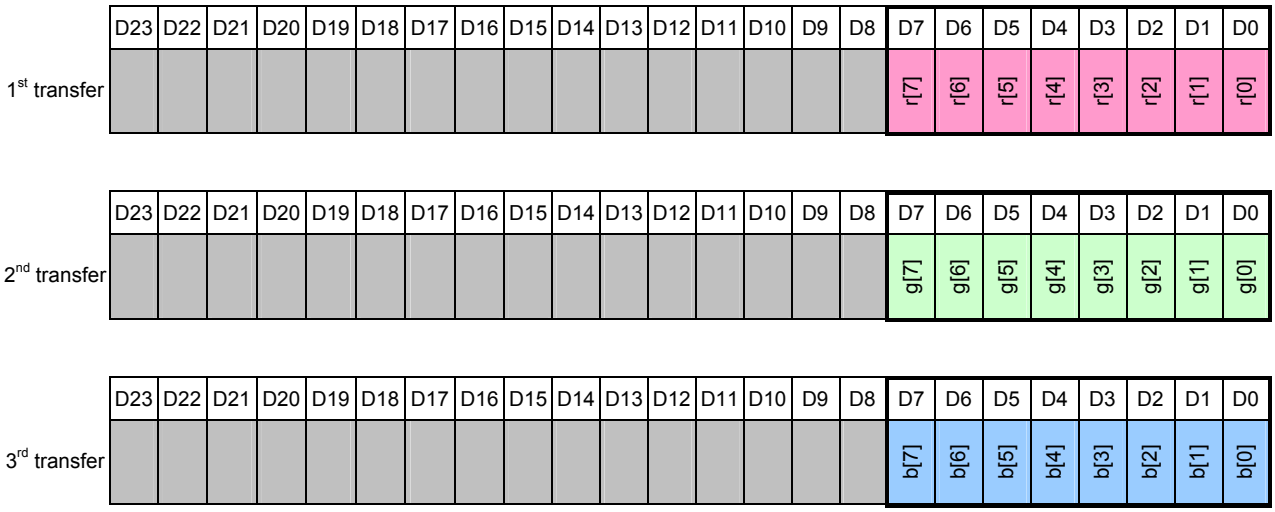


Figure 45

5. Extended Format for 24 Bits/Pixel Data in 16-/18-Bit Interface Operation

The R61529 supports a format extended from 16bpp or 18bpp to 24bpp as shown below. A method for extending a format is set by EPF.

	Frame memory data (24 bits)																					
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
24bpp	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
18bpp EPF=2'h0 (Note 1)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	0	0
18bpp EPF=2'h1 (Note 2)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1	1
18bpp EPF=2'h2	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	R[5]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	B[5]	B[4]
16bpp EPF=2'h0 (Note 3)	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[4]	B[3]	B[2]	B[1]	B[0]	0	0	0
16bpp EPF=2'h1 (Note 4)	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[4]	B[3]	B[2]	B[1]	B[0]	1	1	1
16bpp EPF=2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	R[3]	R[2]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]	B[3]	B[2]

Figure 46

Notes:
1. Special processing: R[5:0], G[5:0], B[5:0] = 6'h3F → 8'hFF
2. Special processing: R[5:0], G[5:0], B[5:0] = 6'h00 → 8'h00
3. Special processing: R[5:0], B[5:0] = 5'h1F → 8'hFF
   G[5:0] = 6'h3F → 8'hFF
4. Special processing: R[4:0], B[4:0] = 5'h00 → 8'h00
   G[5:0] = 6'h00 → 8'h00
5. Setting EPF to 2'h3 is prohibited.

6. BGR Register Setting and Write/Read Data in Frame Memory

Data is written by the host processor is stored in frame memory. When data is stored in frame memory, allocation of R and B in frame memory is swapped according to BGR register setting. Data written to frame memory corresponds to display data. The host processor outputs write and read data in the same RGB order. Examples of BGR register setting are as follows.

BGR = 0

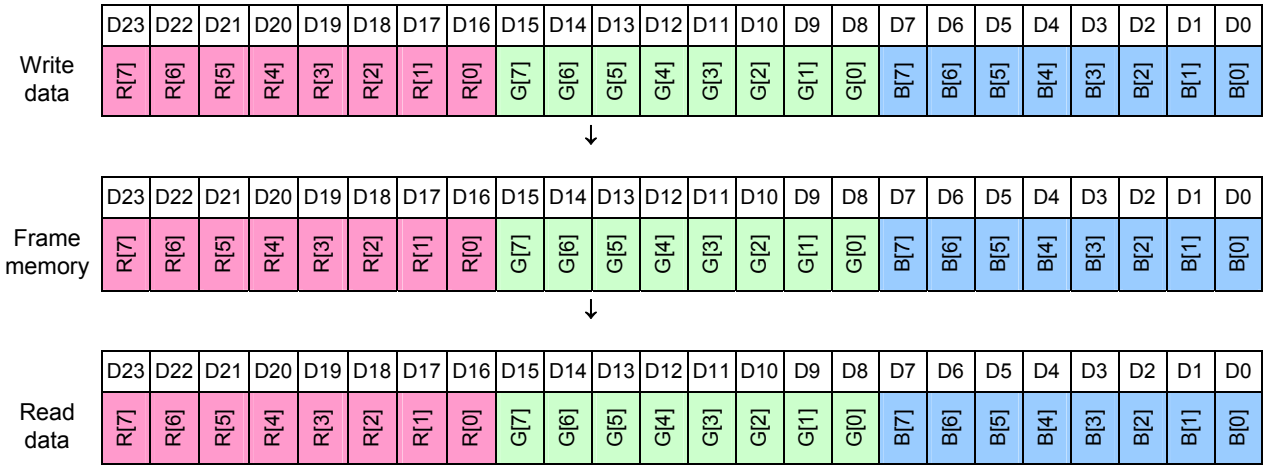


Figure 47

BGR = 1

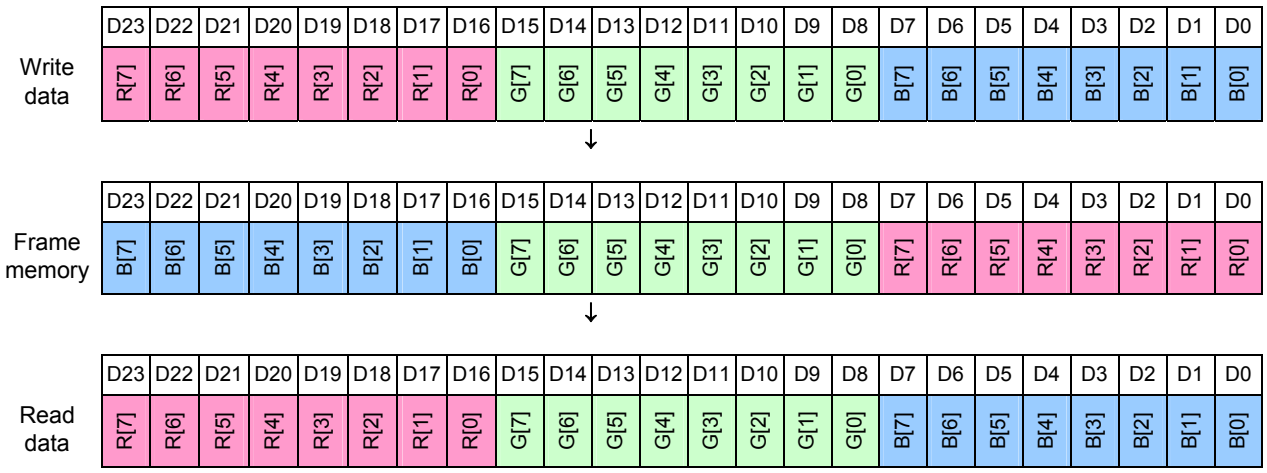


Figure 48

System Interface Configuration (MIPI DBI Type C)

Outline

The R61529 supports serial interface DBI Type C (Option 1 and Option 3). Nine/Eight bit data, transmitted from the R61529 to the host processor, is stored in command register (CDR) or parameter register (PR) to start internal operation which is determined by signals from the host processor.

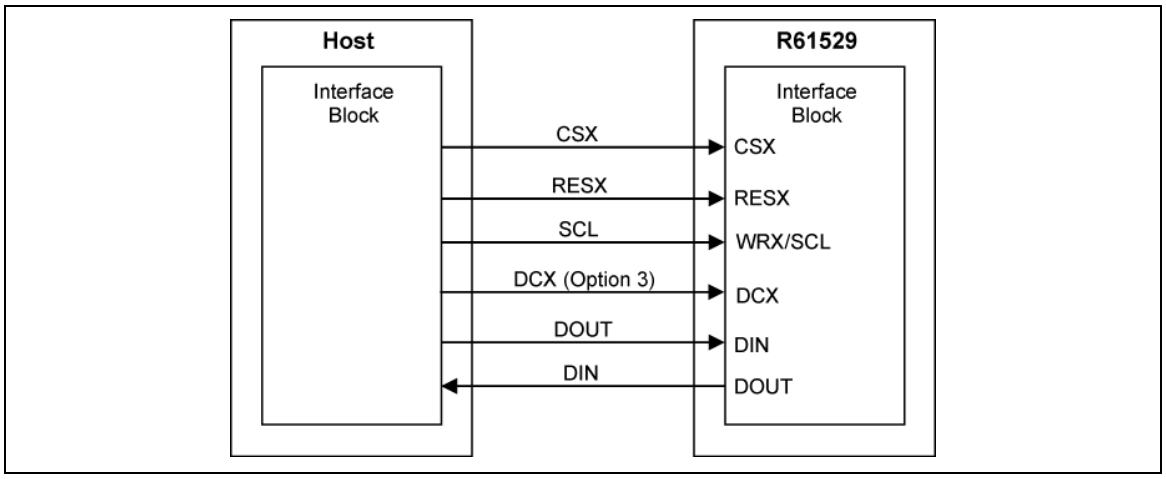
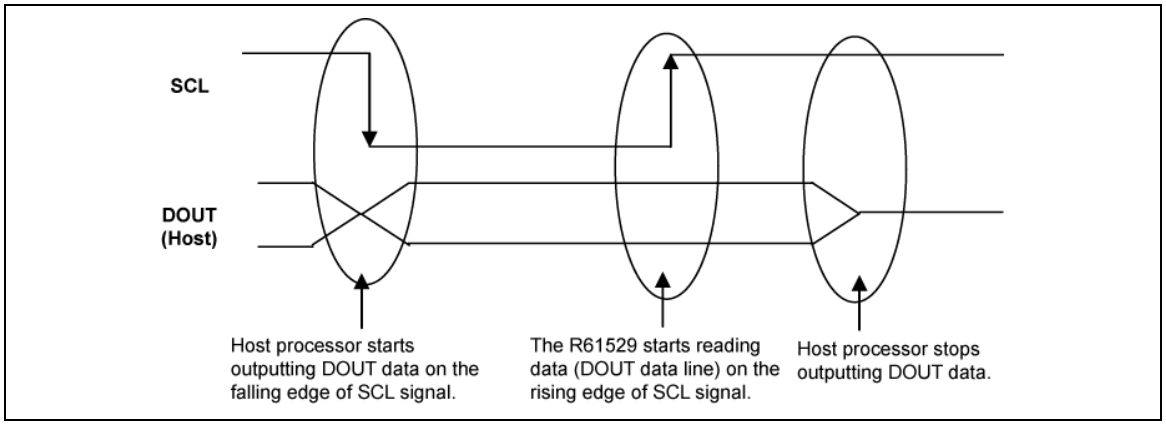


Figure 49 Example of DBI Type C

Write Cycle Sequence

In write cycle, data and/or command are written to the R61529 via the interface between the R61529 and the host processor. During Write Cycle Sequence, the host processor outputs data while the R61529 accepts data at the rising edge of SCL. See next figures for write cycle sequence.



Note: SCL is not a synchronous signal (can be halted).

Figure 50 Write Cycle Sequence

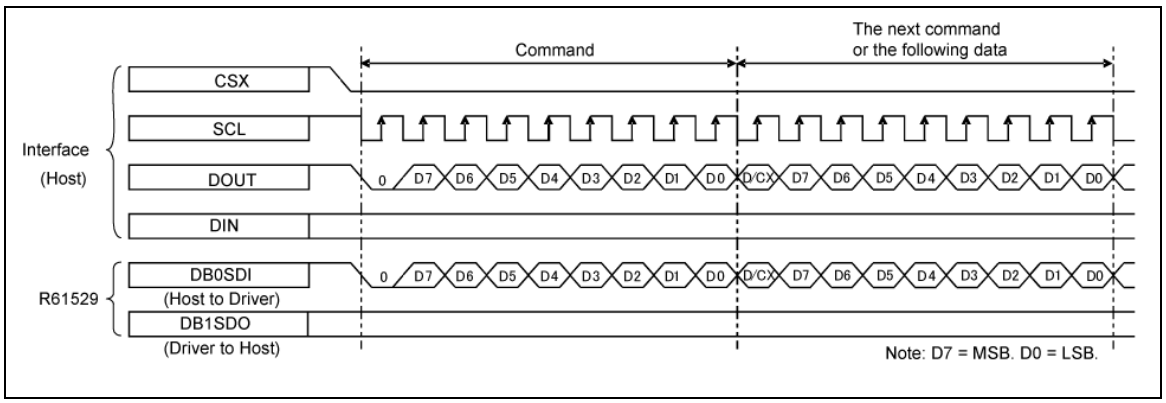


Figure 51 Example of MIPI DBI Type C Write Sequence (Option 1)

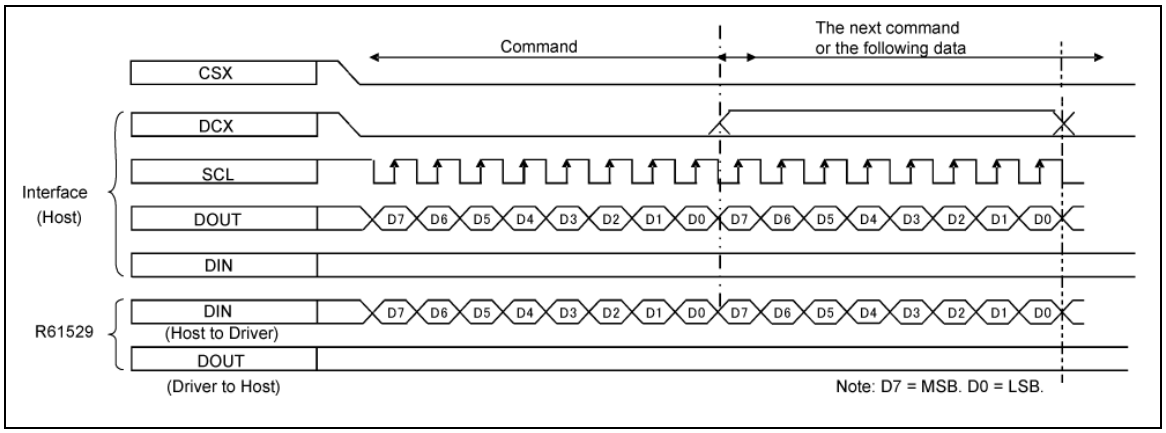
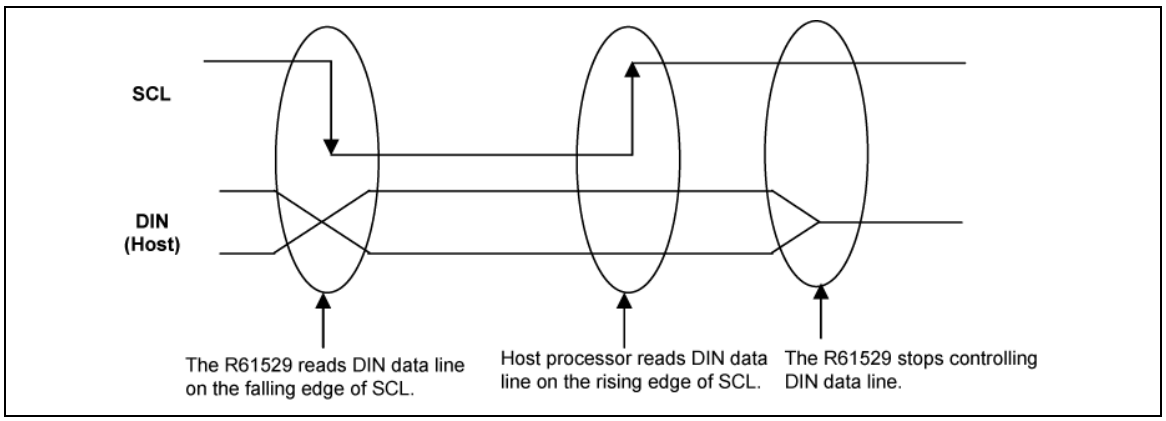


Figure 52 Example of MIPI DBI Type C Write Sequence (Option 3)

Read Cycle Sequence

In read cycle, data and/or commands are read from the R61529 via the interface between the R61529 and the host processor. Data are transmitted from the R61529 to the host processor via DIN on the falling edge of SCL. The host processor reads the data on the rising edge of SCL. See next figure for the read cycle sequence.



Note: SCL is not a synchronous signal (can be halted).

Figure 53 Read Cycle Sequence

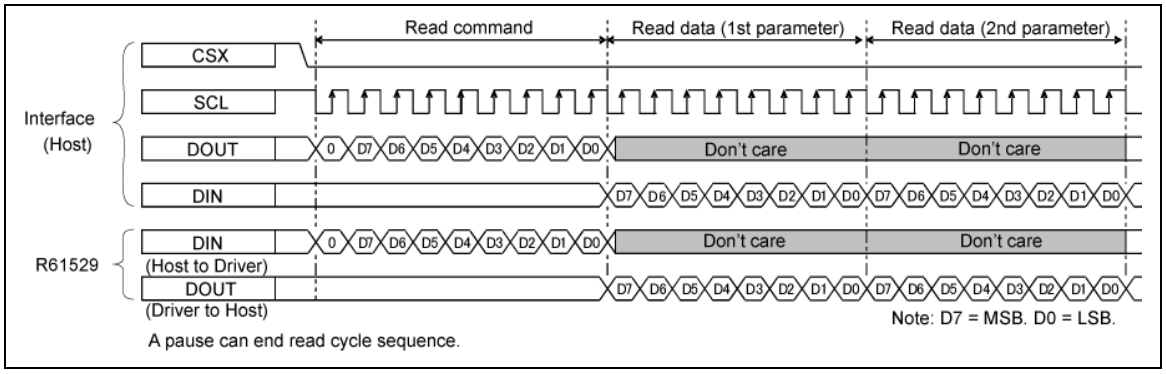


Figure 54 Example of MIPI DBI Type C Read Cycle Sequence (Option 1)

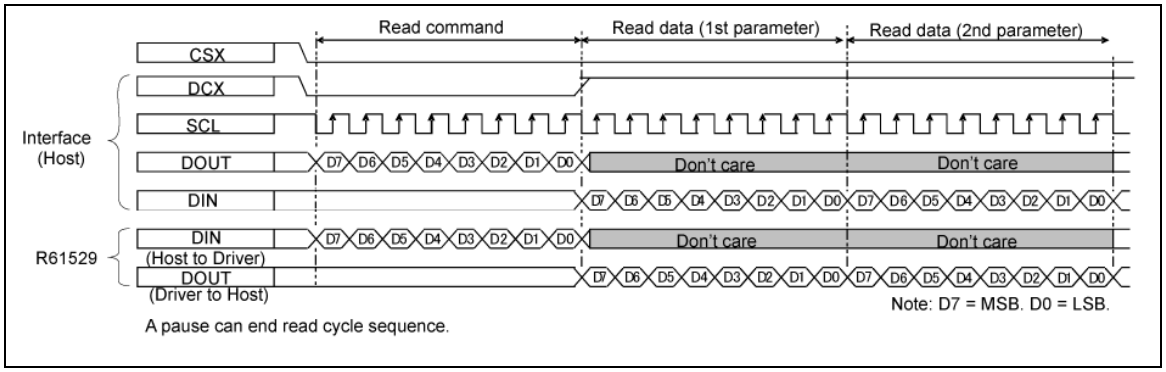


Figure 55 Example of MIPI DBI Type C Read Cycle Sequence (Option 3)

Example of MIPI DBI Type C Read Cycle Sequence (Option 1) Using Read Mode In Command.

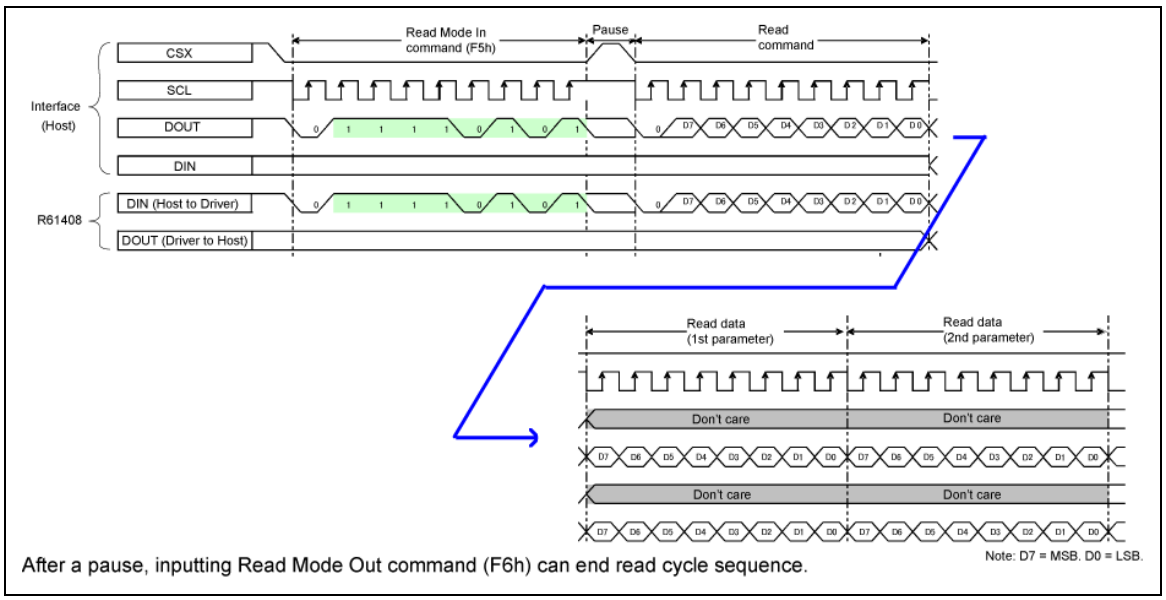


Figure 56

Example of MIPI DBI Type C Read Cycle Sequence (Option 3) Using Read Mode In Command

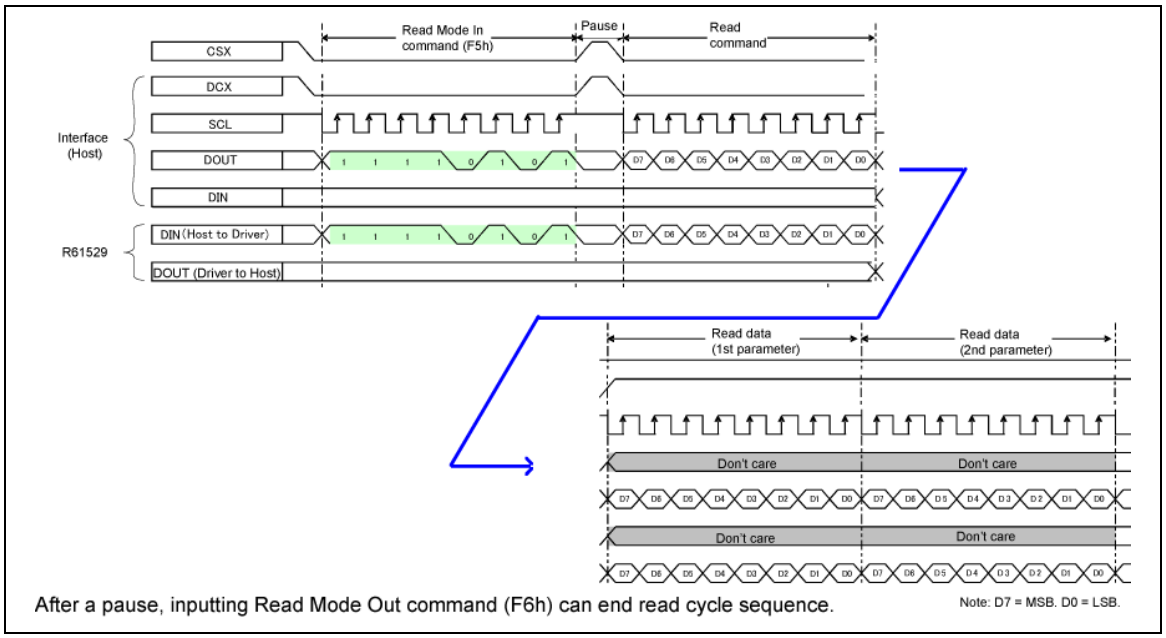


Figure 57

Data Transfer Break

In read cycle, data and/or commands are read from the R61529 via the interface between the R61529 and the host processor. As shown in the figure below, in the transmission of parameter for command from the host processor to the R61529, the command parameters sent to the R61529 before the break occurs are stored in the register of the R61529 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the R61529. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs. However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

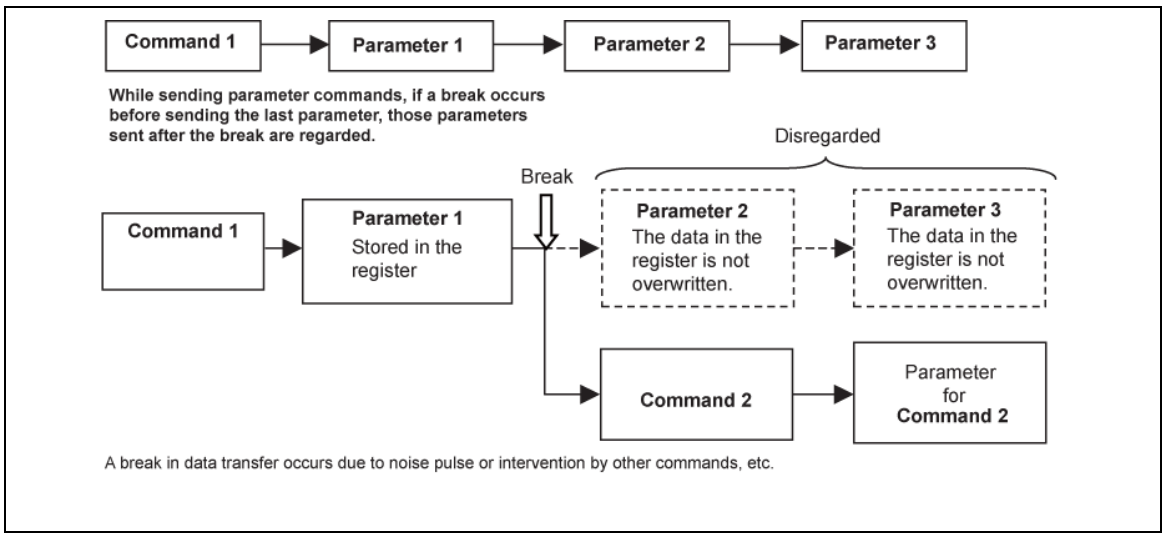


Figure 58

Data Transfer Pause

After transfer of command/parameter ends, write operation resumes from command/parameter right before a stop of transfer if transfer is stopped by setting CSX to “High.” Next transfer starts by setting CSX to “Low.”

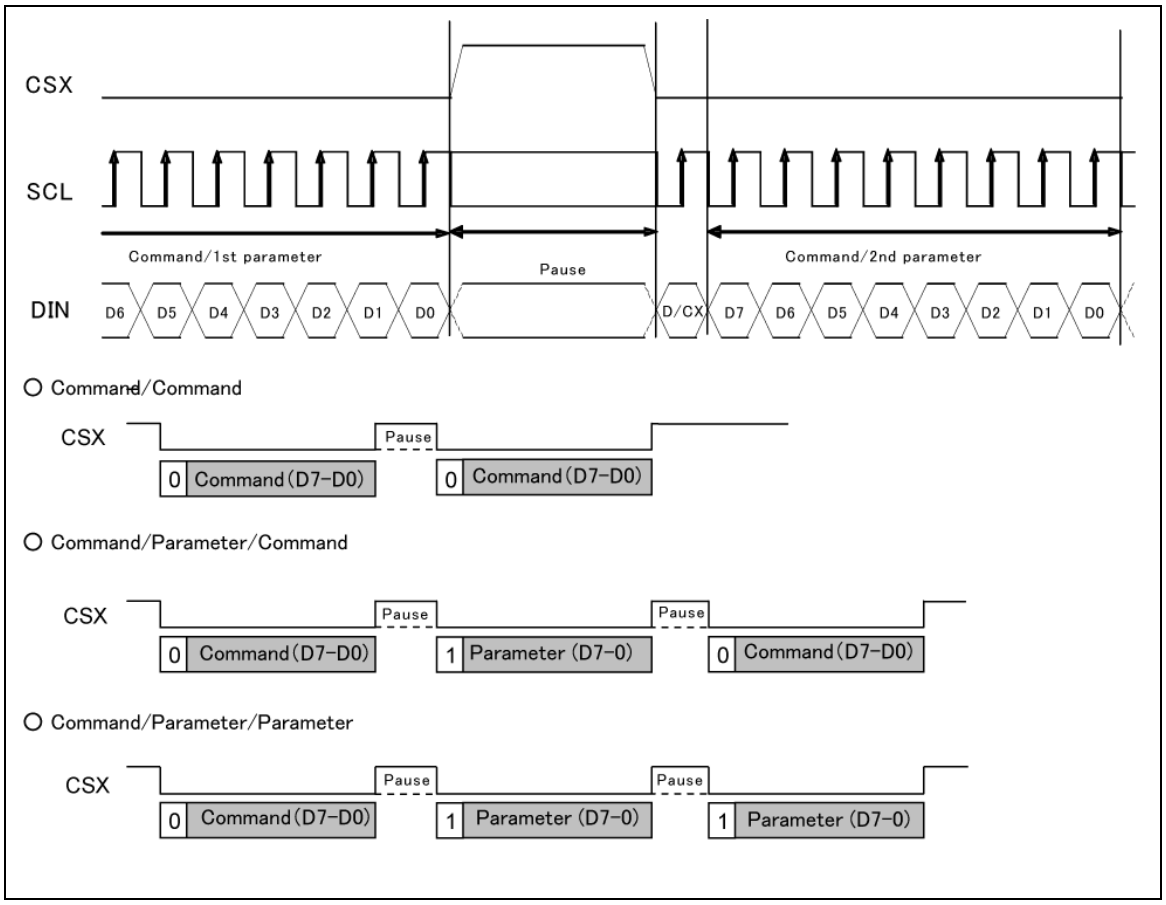


Figure 59

If a pause is invoked during read cycle sequence, transfer should be started with command. The R61529 supports color formats shown below.

DBI Type C Data Format

The R61529 does not support DCS (such as 2Ch, 2Eh, 3Ch, 3Eh) to write/read the data to/from the frame memory.

Table 14

Type	IM3-0	Data pin	Color format	MIPI Spec.	R61529 implementation
Type C (Option 1)	0001	DIN DOUT	3bpp (8-color Option 1)	Yes	No
			3bpp (8-color Option 2)	Yes	No
			16bpp (65,536-color Option 1)	No	No
			16bpp (65,536-color Option 2)	No	No
			18bpp (262,144-color Option1)	No	No
			18bpp (262,144-color Option2)	No	No
			24bpp	No	No
Type C (Option 3)	1001	DIN DOUT	3bpp (8-color Option 1)	Yes	No
			3bpp (8-color Option 2)	Yes	No
			16bpp (65,536-color Option 1)	No	No
			16bpp (65,536-color Option 2)	No	No
			18bpp (262,144-color Option1)	No	No
			18bpp (262,144-color Option2)	No	No
			24bpp	No	No

Yes: Supported
No: Unsupported

System Interface Configuration (I2C)

The R61529 supports I2C bus interface as serial interface. Data is transferred via serial transmit/receive data bus (DIN) and serial transfer clock line (SCL). In the I2C bus system, the R61529 is a bidirectional slave device.

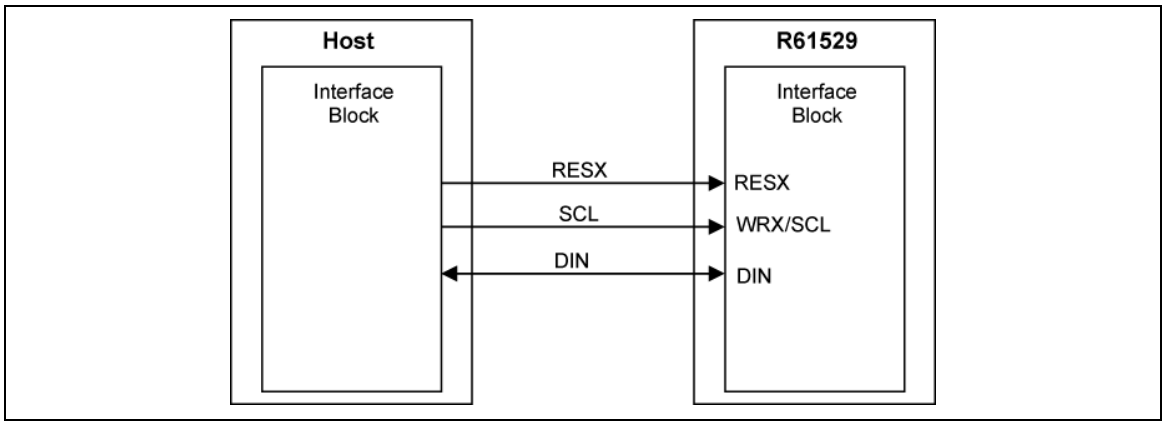


Figure 60 Example of I2C

Operation mode can be selected from Mode 1 or Mode 2 by setting the IM pins.

- Mode 1: Normal operation
  When the R61529 enters Mode 1, it starts data transfer according to a specified slave address.

- Mode 2: NVM Operation
  When the R61529 enters Mode 2, it always starts data transfer regardless of a slave address. Write data to NVM in this mode before a slave address is specified.

Note: To connect the interface bus to a device, start data transfer according to a slave address from one specified in other devices.

First Byte of I2C Bus

Table 15

First byte	Start	1	2	3	4	5	6	7	8	9
		I2C slave address							R/W	ACK
Mode 1 (normal operation)	Start	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	R/W	ACK/ NACK
Mode 2 (NVM operation)	Start	x	x	x	x	x	x	x	R/W	ACK/ NACK

Table 16

R/W	Function
0	Command write
1	Command read

Table 17

ACK	Function
0	ACK
Hi-Z	NACK

The 7-bit data after the start of transfer is treated as an I2C slave address. In Mode 1, an ID code (IFID[6:0]) stored in NVM beforehand is used as a slave address. If a slave address transferred by host corresponds to the ID code, the subsequent data transfer is treated as access to the R61529. The R61529 returns ACK to host by setting the ninth bit to “L” (ACK operation). If a slave address transferred by host does not correspond to the ID code, the R61529 does not set the ninth bit to “L”. The bit is set to “H” by an external pull-up resistor (NACK operation). In Mode 2, data transfer is treated as access to the R61529 regardless of a slave address.

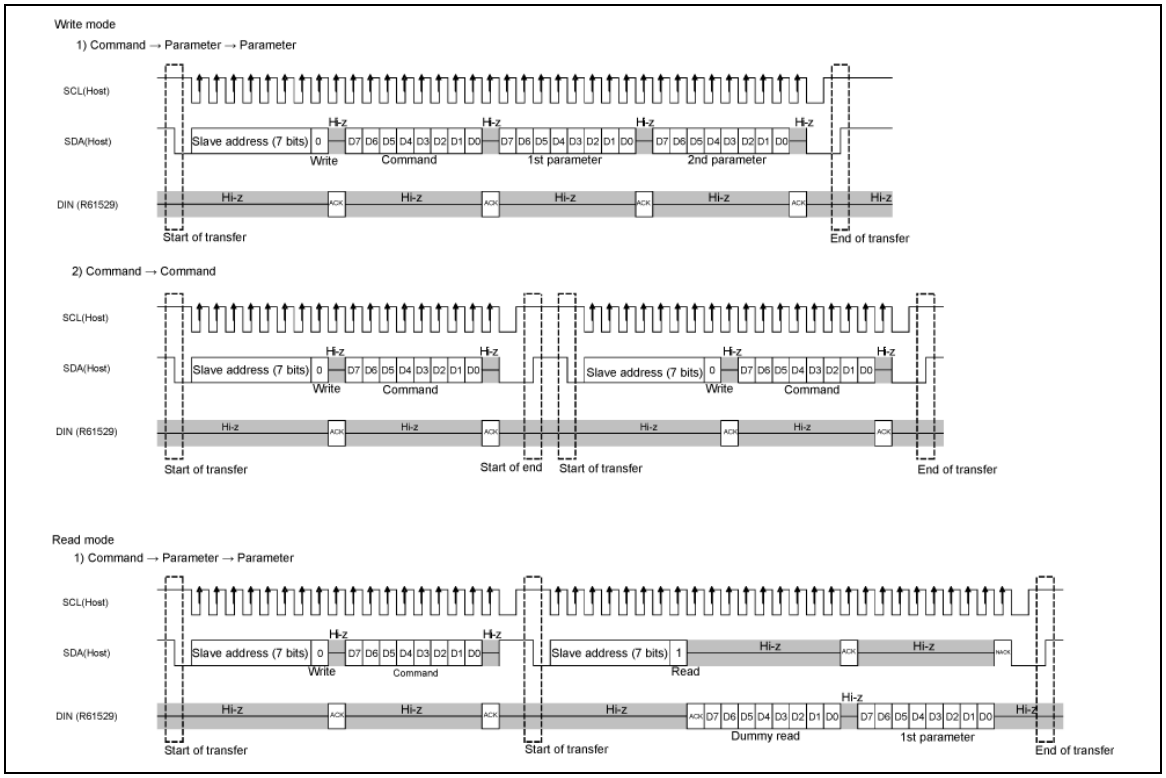


Figure 61 Serial Data Transfer via I2C Bus Interface

I2C Data Format

The R61529 does not support DCS (such as 2Ch, 2Eh, 3Ch, 3Eh) to write/read the data to/from the frame memory.

Table 18

Type	IM3-0	Data pin	Color format	R61529 implementation
I2C	0000	DIN	3bpp (8-color Option 1)	No
			3bpp (8-color Option 2)	No
			16bpp (65,536-color Option 1)	No
			16bpp (65,536-color Option 2)	No
			18bpp (262,144-color Option1)	No
			18bpp (262,144-color Option2)	No
			24bpp	No

Yes: Supported

No: Unsupported

System Interface Configuration (MIPI DSI)

The DSI incorporated in the R61529 complies with the following standards:

MIPI DSI: Version 1.01.00r11 21-Feb-2008
MIPI D-PHY: Version 0.90.00 8-Oct-2007
MIPI DCS: Version 1.01.00 B5 of set_address_mode command (36h): Setting to only 0 (horizontal direction) is supported

(1) Basic DSI Specification

- Number of data lanes: 1 data lane
- Maximum data rate: 380Mbps/lane @video mode
- Command Mode and Video Mode supported

  Video data received in Video Mode is directly output as display data without being written to internal RAM
- B5 of set_address_mode command (36h): Setting to 0 (horizontal direction) is supported
- RAM window address setting
  - set_column_address (2Ah)

    SC[9:0] = 2n (n = 0, 1, 2, …159)
    EC[9:0] = 2m – 1 (m = 1, 2, …160)
    EC – SC > 2 pixels

(2) DSI System Configuration

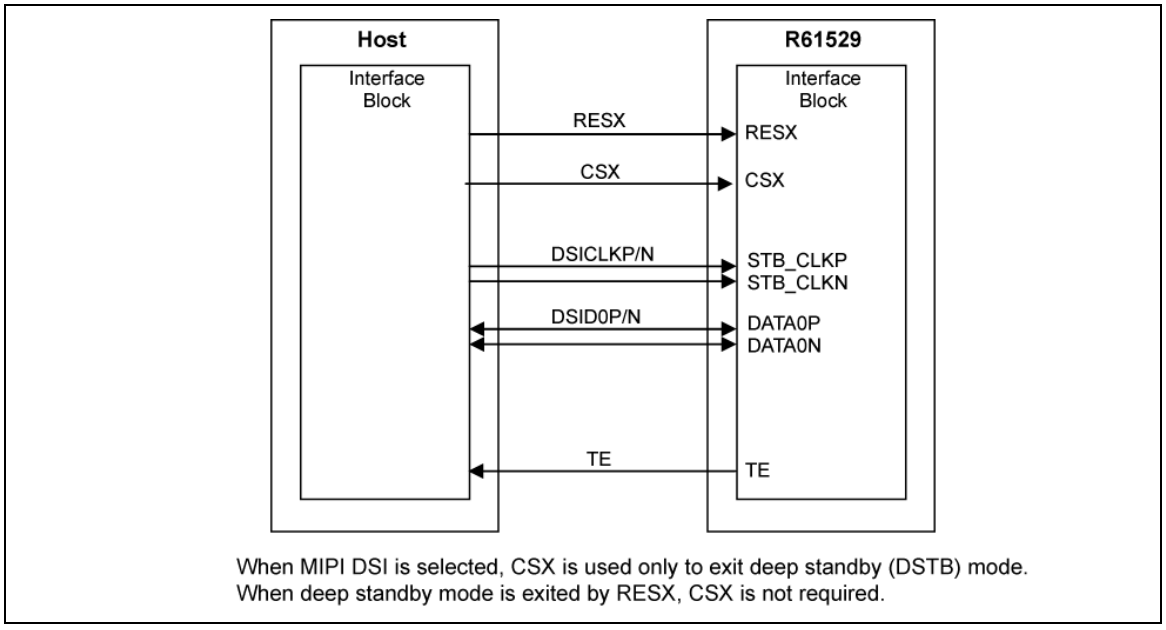


Figure 62 Example of DSI

(3) Lane State Definition

Table 19 Lane State Description

State code	Line voltage levels		High speed	Low power	
	Dp-line	Dn-line	Burst mode	Control mode	Escape mode
HS-0	HS Low	HS High	Differential-0	1	1
HS-1	HS High	HS Low	Differential-1	1	1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	2

Notes: 1. During high-speed transmission, the low power receivers observe LP-00 on the lines.
2. If LP-11 occurs during Escape mode, the lane returns to Stop state (Control mode LP-11).

(4) DSI-CLK Lane

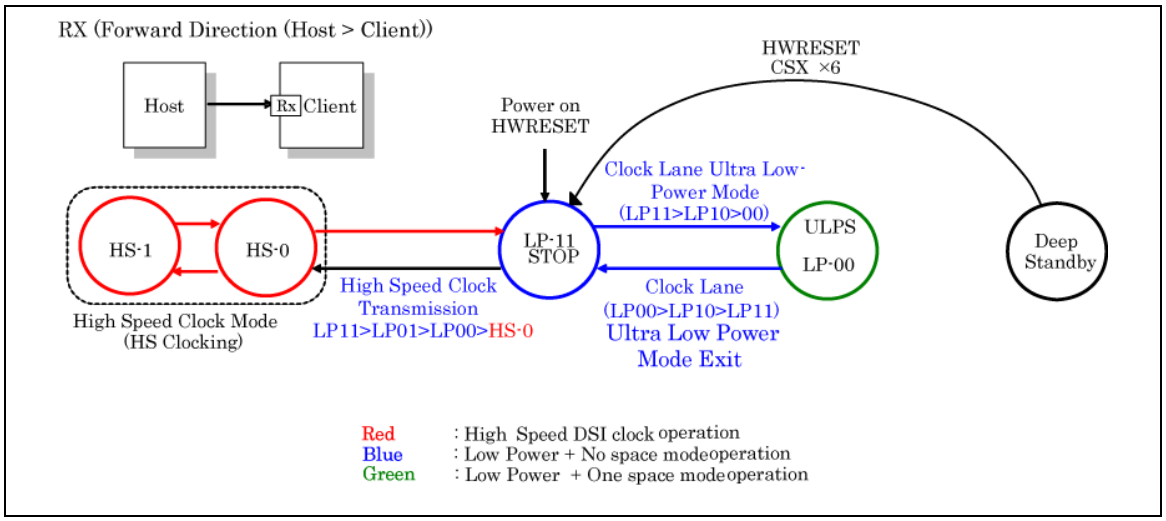


Figure 63 Clock Lane State Diagram

1) Low Power Mode (LP-11: STOP)

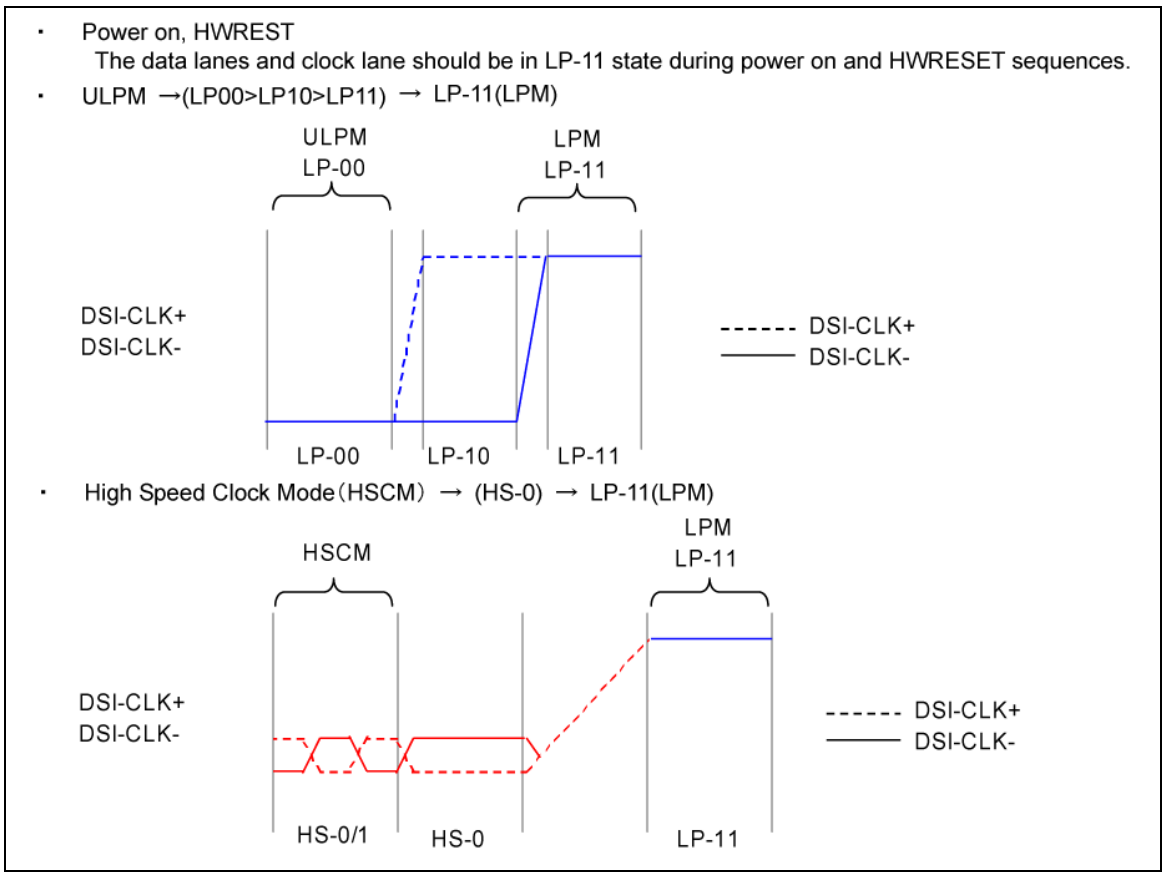


Figure 64 Switching the Clock Lane between Clock Transmission and Low Power Mode 1

2) Ultra Low Power Mode (LP-00: ULPM)

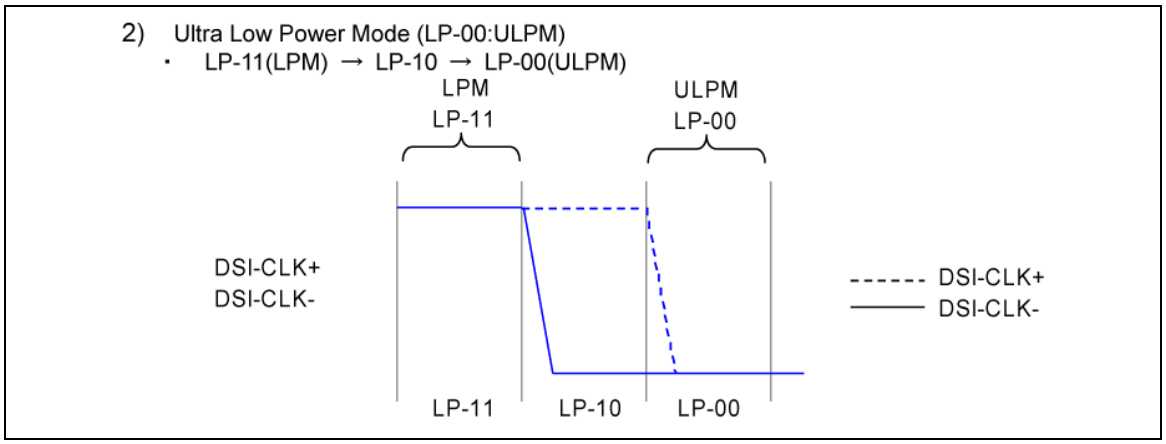


Figure 65 Switching the Clock Lane between Clock Transmission and Low Power Mode 2

3) High Speed Clock Mode

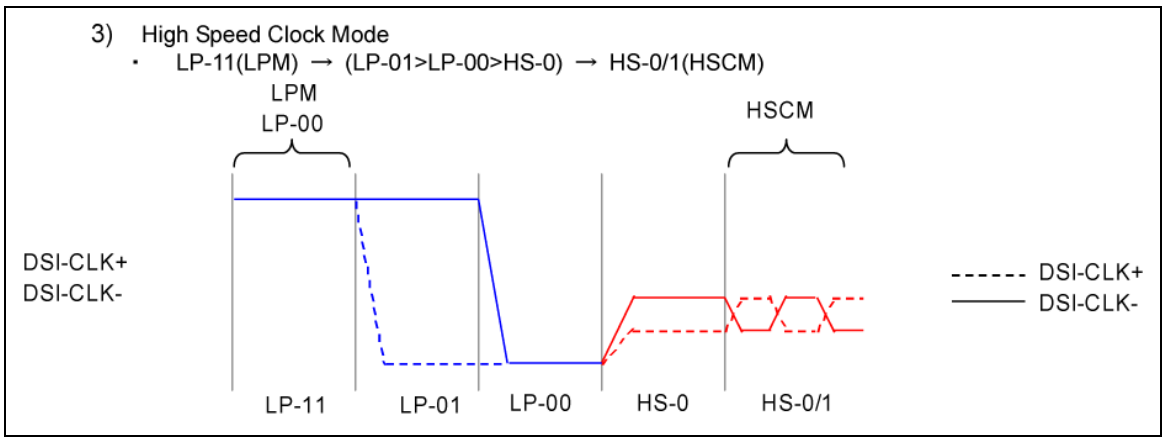


Figure 66 Switching the Clock Lane between Clock Transmission and Low Power Mode 3

4) High Speed Clock Burst

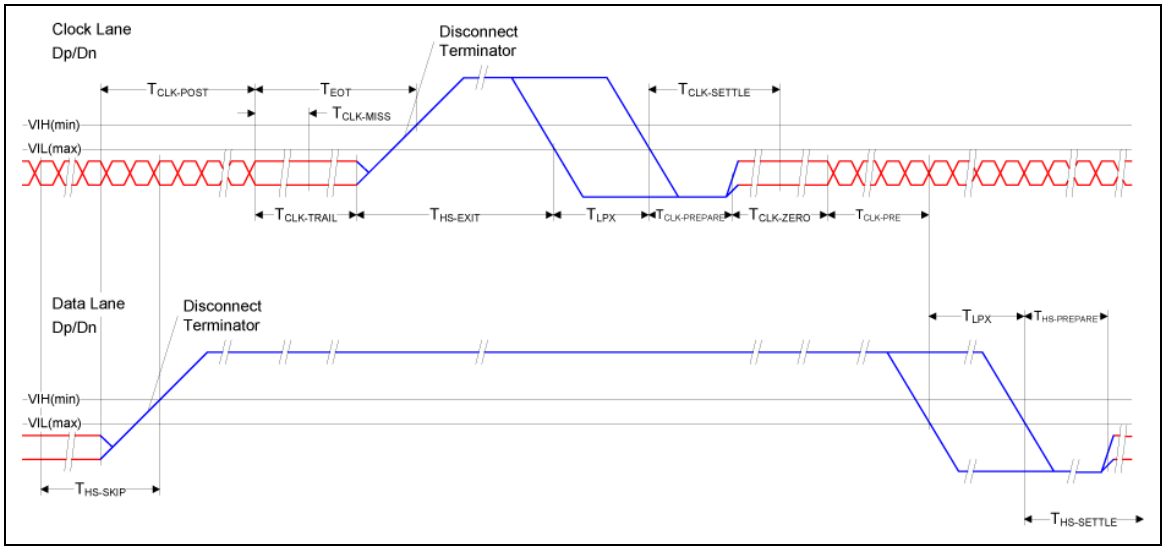


Figure 67 Switching the Clock Lane between Clock Transmission and Low Power Mode 4

(5) DSI-D0 Data Lane

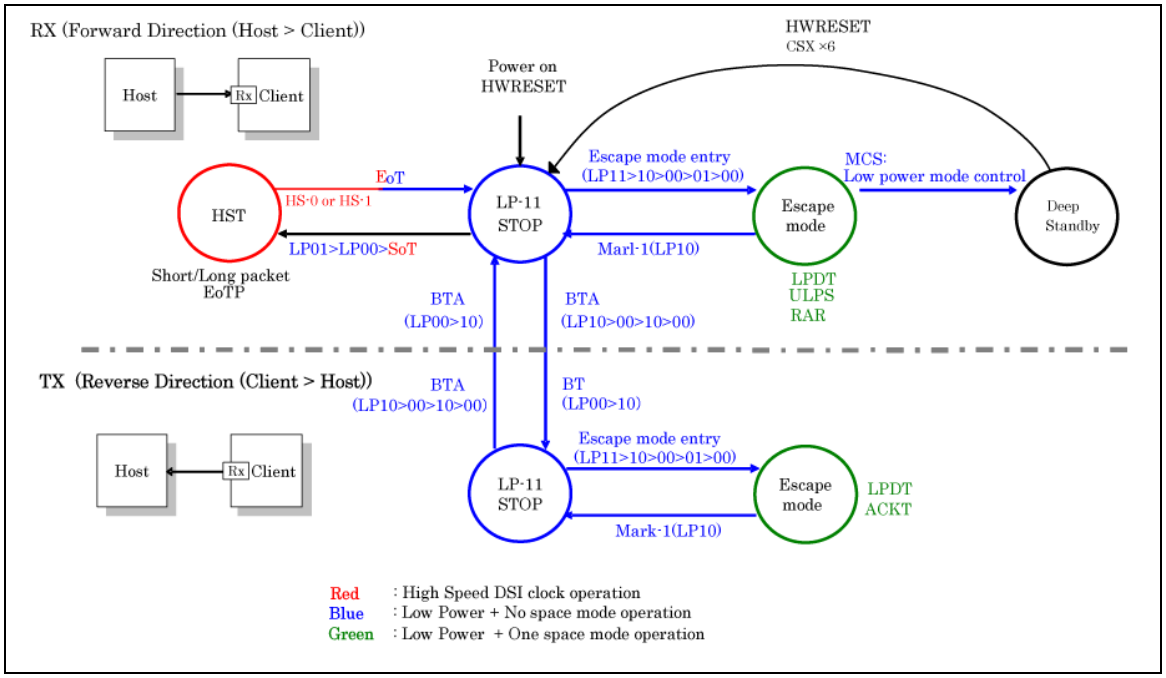


Figure 68 DSI-D0 Data Lane State Diagram

Table 20 Data Lane Operating Modes

No.	Description	Operation code	Note
1	High Speed Data Transmission Burst	LP-11 > L-P01 > LP-00	
2	Escape mode entry	LP-11 > LP-10 > LP-00 > LP-01 > LP-00	
3	Turnaround	LP-11 > LP-10 > LP-00 > LP-10 > LP-00	1
4	Exit Escape mode (Mark-1)	L-10	
5	Deep Standby Mode	DSTB=1	2
6	Exit Deep Standby Mode	CSX ×6	3

Note: 1. Before Turnaround operation, DBI Packet must be sent.
2. DSTB must be sent by Escape mode in Sleep mode.
3. After exiting from the Deep Standby Mode, all of commands are reset.

1) Power On, HWRESET → LP-11

The data lanes and clock lane should be in the LP-11 state during power-on and HWRESET sequences.

2) Escape Mode

- Escape mode entry
- Mark-1 (exit Escape mode)

Table 21 Escape Entry Code

No.	Symbol	Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)	R61529 implementation		Note
					LP-RX	LP-TX	
1	LPDT	Low Power Data Transmission	Mode	1110_0001	Yes	Yes	
2	ULPS	Ultra-Low Power State	Mode	0001_1110	Yes	No	
3	UDF1	Undefined-1	Mode	1001_1111	No	No	
4	UDF2	Undefined-2	Mode	1101_1110	No	No	
5	RAR	Remote Application Reset	Trigger	0110_0010	Yes	No	See note.
6	TER	TE-Report	Trigger	0101_1101	No	No	
7	ACKT	Unkown-4 (Acknowledge Trigger)	Trigger	0010_0001	No	Yes	
8	UNK5	Unknown-5	Trigger	1010_0000	No	No	

Note: DSI circuit is reset by Remote Application Reset.

3) Escape Mode (Host >Client): Low Power Data Transmission (LPDT)

An example of DSI read sequence by LPDT is shown below.

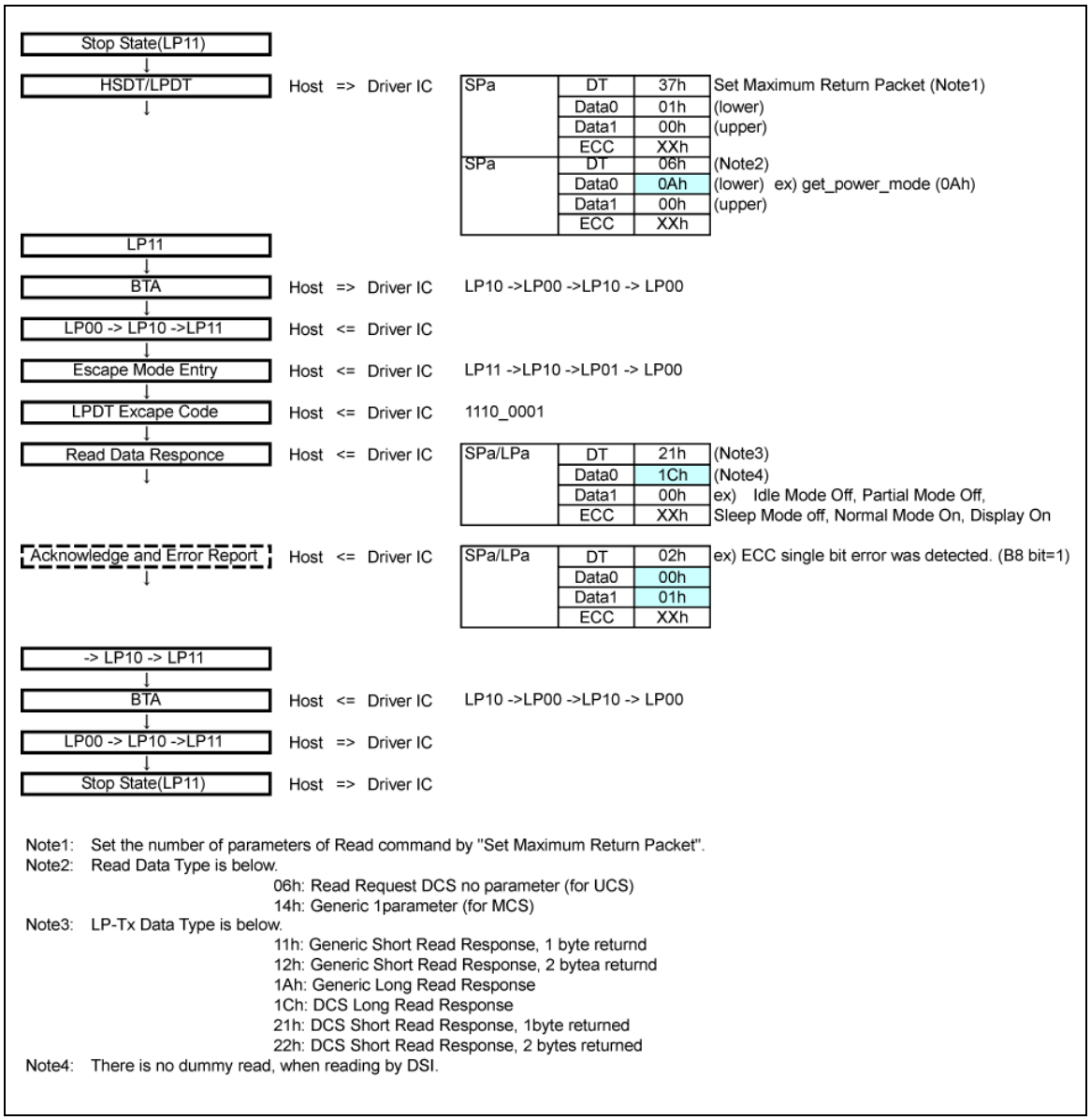


Figure 69

4) Escape Mode (Host>Client): Ultra Low Power State (ULPS)

5) Escape Mode (Host>Client): Remote Application Reset (RAR)

6) Escape Mode (Client > Host): Acknowledge Trigger (ACKT)

7) High Speed Data Transmission (HST)

8) Bus Turnaround (Host>Client) (BTA)

9) Bus Turnaround (Client>Host) (BTA)

(6) Packet Level Communication

1) Short Packet (SPa) Structure

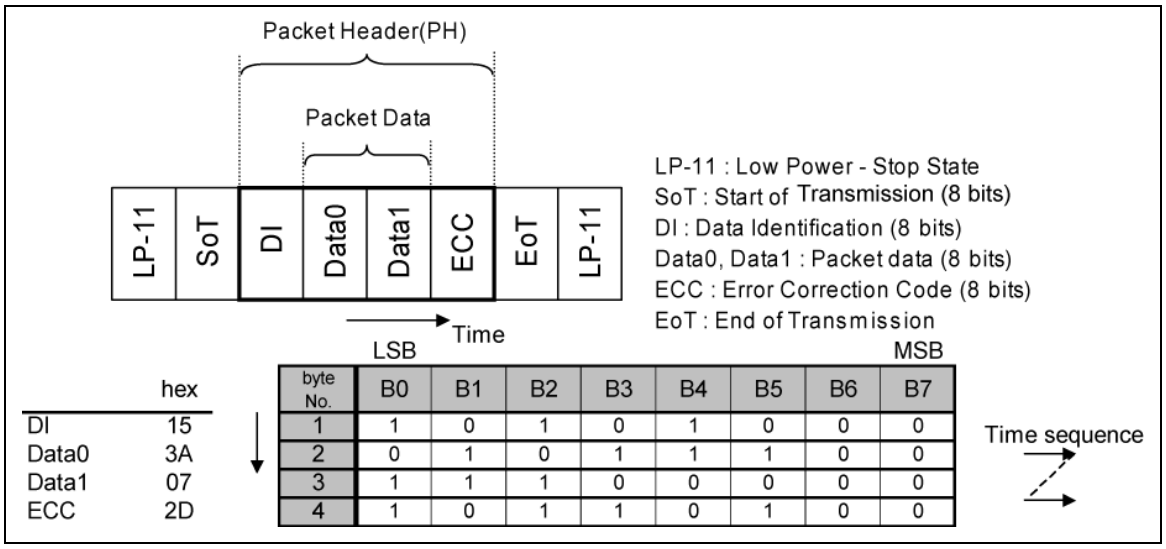
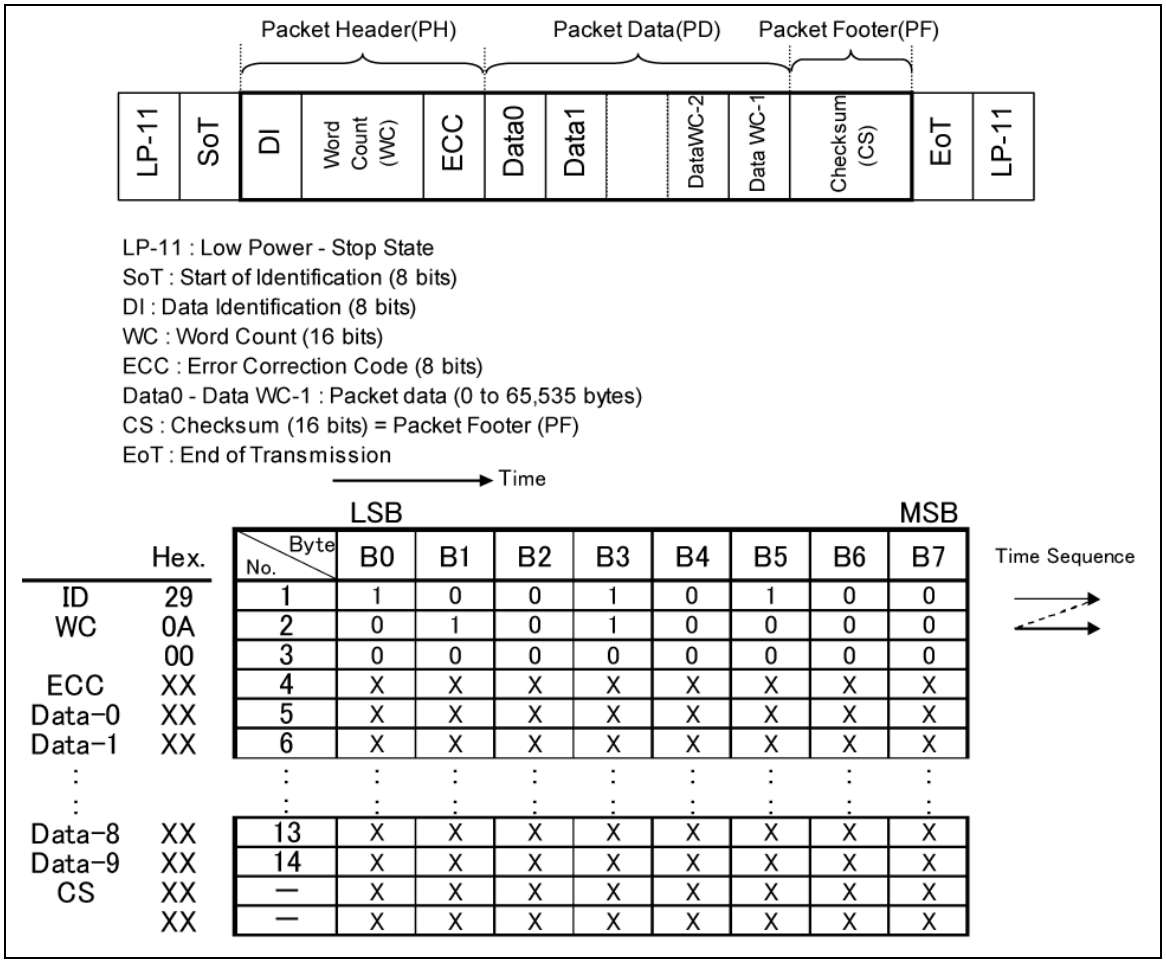


Figure 70 Example of Short Packet (SPa) (DCS WRITE, 1 Parameter)

2) Long Packet (LPa) Structure



	Hex.	Byte No.	B0	B1	B2	B3	B4	B5	B6	B7
ID	29	1	1	0	0	1	0	1	0	0
WC	0A	2	0	1	0	1	0	0	0	0
	00	3	0	0	0	0	0	0	0	0
ECC	XX	4	X	X	X	X	X	X	X	X
Data-0	XX	5	X	X	X	X	X	X	X	X
Data-1	XX	6	X	X	X	X	X	X	X	X
:		:	:	:	:	:	:	:	:	:
:		:	:	:	:	:	:	:	:	:
Data-8	XX	13	X	X	X	X	X	X	X	X
Data-9	XX	14	X	X	X	X	X	X	X	X
CS	XX	—	X	X	X	X	X	X	X	X
	XX	—	X	X	X	X	X	X	X	X

Figure 71

3) Multiple Packet Sending

In LP-11 state, multiple Short Packets (SPa) and Long Packets (LPa) can be received between SoT and EoT.

LP-11 → SoT → SPa → SPa → EoT

LP-11 → SoT → SPa → LPa → EoT

LP-11 → SoT → LPa → LPa → EoT

LP-11 → SoT → LPa → SPa → EoT

LP-11 → SoT → Combination of the above methods → EoT

(7) Data Identification (DI)

1) Virtual Channel (VC)

The R61529 supports Virtual Channel only when VC = 00. Set VC = 00 during packet transmission. If a packet is received when VC is other than 00, the packet is regarded as invalid. This result is reflected on an Error Report.

2) Data Type (DT)

If a Data Type undefined in the MIPI DSI specification is received, the subsequent data cannot be received. Transmit data again after checking that the R61529 is in LP-11 state by Error Report. If a Data Type unsupported in the R61529 is received, it is regarded as NOP, and the result is not reflected on the Error Report.

Table 22

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
B7 (0)	B6 (0)	B5	B4	B3	B2	B1	B0

Table 23 R61529 Rx Data Type List

Data Type	Description	Packet size	DBI packet	DPI packet	R61529 (Rx) implementation	Note
01h	Sync Event, V Sync Start	Short		Yes	Yes	
11h	Sync Event, V Sync End	Short		Yes	No	5
21h	Sync Event, H Sync Start	Short		Yes	Yes	
31h	Sync Event, H Sync End	Short		Yes	No	5
08h	End of Transmission packet (EoT)	Short			Yes	4
02h	Color Mode (CM) Off Command	Short		Yes	No	
12h	Color Mode (CM) On Command	Short		Yes	No	
22h	Shut Down Peripheral Command	Short		Yes	Yes	7
32h	Turn On Peripheral Command	Short		Yes	Yes	7
03h	Generic Short WRITE, no parameters	Short	Yes		No	5
13h	Generic Short WRITE, 1 parameter	Short	Yes		Yes	1, 2
23h	Generic Short WRITE, 2 parameters	Short	Yes		Yes	1, 2
04h	Generic READ, no parameters	Short	Yes		No	5
14h	Generic READ, 1 parameter	Short	Yes		Yes	
24h	Generic READ, 2 parameters	Short	Yes		Yes	1, 2
05h	DCS WRITE, no parameters	Short	Yes		Yes	1, 2
15h	DCS WRITE, 1 parameter	Short	Yes		Yes	1, 2
06h	DCS READ, no parameters	Short	Yes		Yes	1, 2
37h	Set Maximum Return Packet Size (default 0001h)	Short	Yes		Yes	6
09h	Null Packet, no data	Long			Yes	
19h	Blanking Packet, no data	Long		Yes	Yes	
29h	Generic Long Write	Long	Yes		Yes	
39h	DCS Long Write/write_LUT Command Packet	Long	Yes		Yes	
0Eh	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long		Yes	No	3
1Eh	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long		Yes	No	3
2Eh	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long		Yes	Yes	3
3Eh	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long		Yes	Yes	3
other	All unspecified codes are reserved	-	-	-	-	

Table 24 R61529 LP-Tx Data Type List

Data Type	Description	Packet size	R61529 (LP-Tx) implementation	Note
00h-01h	Reserved	—	—	
02h	Acknowledge with Error Report	Short	Yes	
03h-7h	Reserved	—	—	
08h	End of Transmission packet (EoT)	Short	No	
09h-10h	Reserved	—	—	
11h	Generic Short READ Response, 1 byte returned	Short	Yes	
12h	Generic Short READ Response, 2 bytes returned	Short	Yes	
13h-18h	Reserved	—	—	
1Ah	Generic Long READ Response	Long	Yes	
1Bh	Reserved	—	—	
1Ch	DCS Long READ Response	Long	Yes	
1Dh-20h	Reserved	—	—	
21h	DCS Short READ Response, 1 byte returned	Short	Yes	
22h	DCS Short READ Response, 2 bytes returned	Short	Yes	
23h-28h	Reserved	—	—	
29h-3Fh	Reserved	—	—	

Notes: 1. Generic Command is Manufacturer Command.
DCS Command is User Command.

2. Generic XXX 1 parameter is Manufacturer Command + 1 byte (all “0”).
Generic XXX 2 parameter is Manufacturer Command + 1 parameter.
DCS XXX no parameter is User Command + 1 byte (all “0”).
DCS XXX 1 parameter is User Command + 1 parameter.

3. Line data (320RGB) must be sent by one packet.

4. EoT packet (Data Type: 08h) is not defined in the MIPI Alliance Standard for Display Serial Interface Version 1.01.00 Release 11.

5. Any packet with data type that MIPI Specification defines and the R61529 doesn’t support is treated as NOP.

6. When the host processor requests a response from the R61529, the R61529 returns the data of the same number as the maximum packet size. Default value of the maximum packet size is 000Fh (15 bytes). If the number of the valid data which the R61529 returns is less than the maximum packet size, the R61529 returns the valid data and “00h” as dummy data.

7. Using Data Types 22h and 32h with 01h, 10h, 11h, 28h, or 29h command (DCS) is prohibited.

(8) Word Count (WC) on Long Packet (LPa)

Word Count (WC) = 2 bytes: The number of packet data on Long Packet (0 to 65,535 bytes)

(9) Error Correction Code (ECC)

ECC detects 1-bit errors or multiple-bit errors in each Packet Header. ECC is performed on the following:

- Short Packet: DI, Data0, Data1, and ECC
- Long Packet: DI, WC (2 bytes), and ECC

(10) Packet Footer on Long Packet (LPa)

In the Long Packet, Packet Footer is added after Packet Data. Packet footer includes CRC calculated from Packet Data as checksum.

- Checksum (2 bytes) = CRC (Packet Data): CRC = $X^{16} + X^{12} + X^5 + X^0$

(11) Video Mode

The R61529 supports Video Mode for moving pictures. There are three formats of transmission packet sequences. The R61529 supports two of these formats. See the following table.

Table 25

Transmission packet sequence in video mode	R61529 implementation
Non-burst mode with sync pulses	Not supported
Non-burst mode with sync events	Supported
Burst mode (Clock Lane/Data Lane)	Supported

1) Display Timing (Video Mode)

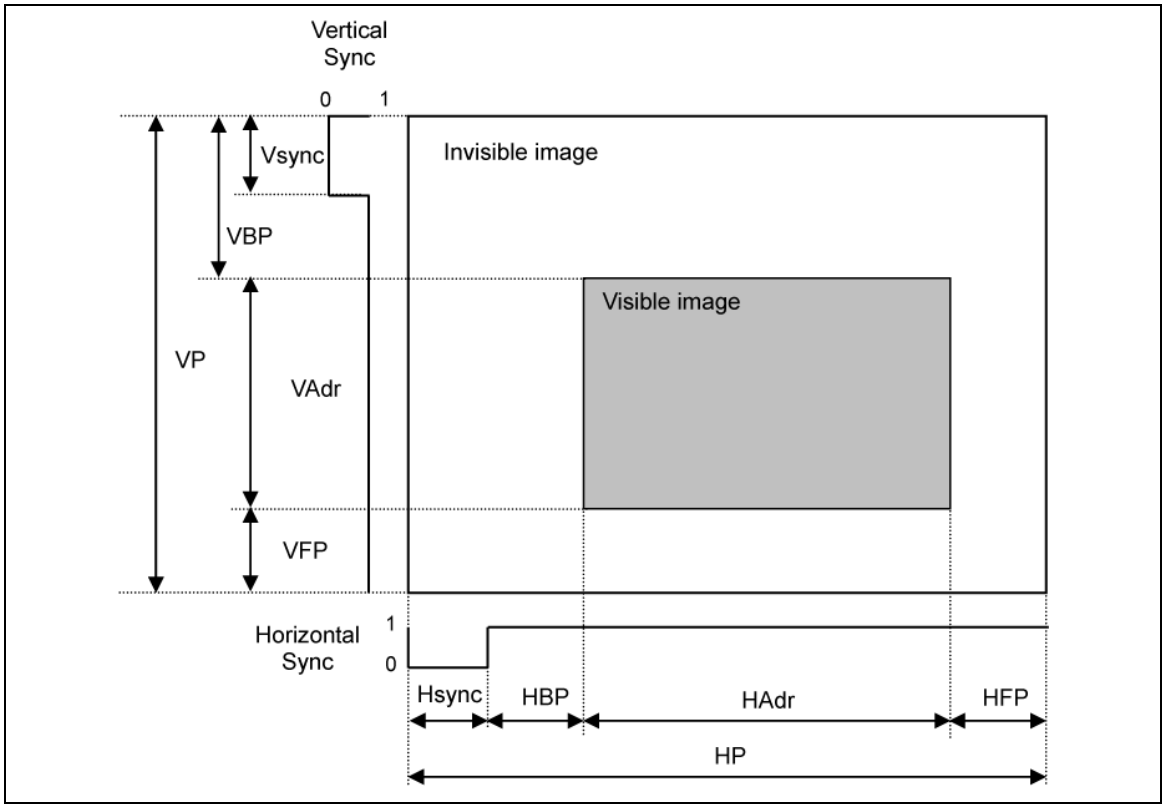


Figure 72

2) Vertical Display Timing (Video Mode)

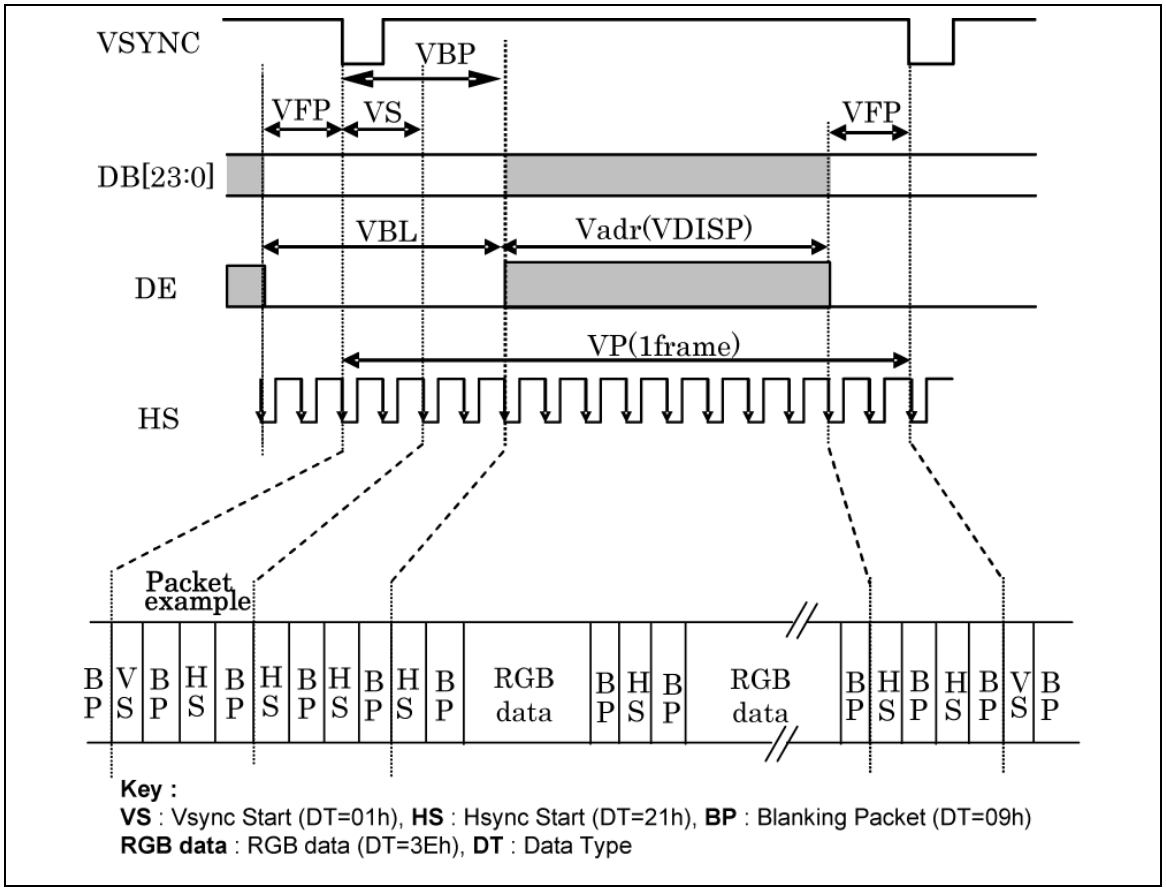


Figure 73

Table 26 Example of Vertical Display Timing Setting

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Vertical cycle	VP		Line	-	(TBD)	-	(1)
Vertical low pulse width	VS		Line	-	(TBD)	-	(1),(2)
Vertical front porch	VFP		Line	(TBD)	(TBD)	-	(1)
Vertical back porch	VBP		Line	(TBD)	(TBD)	-	(1),(2),(3)
Vertical data start point	-	VBP	Line	(TBD)	(TBD)	-	(1),(3)
Vertical blanking period	VBL	VBP+VFP	Line	(TBD)	(TBD)	-	(1),(3)
Vertical active area	Vadr		Line	(TBD)	480	(TBD)	(1)

Notes: 1. [VBP, VFP, Vadr=VD] is set by C1h (Panel Driving Setting 2) command.
2. The number of Hsync packet in 1 frame shall be the same as the total number of horizontal lines. Hsync packets shall be set during BP period.
3. The minimum number of VBL and VBP depends on GCM (C1h).

3) Horizontal Display Timing (MIPI-DSI)

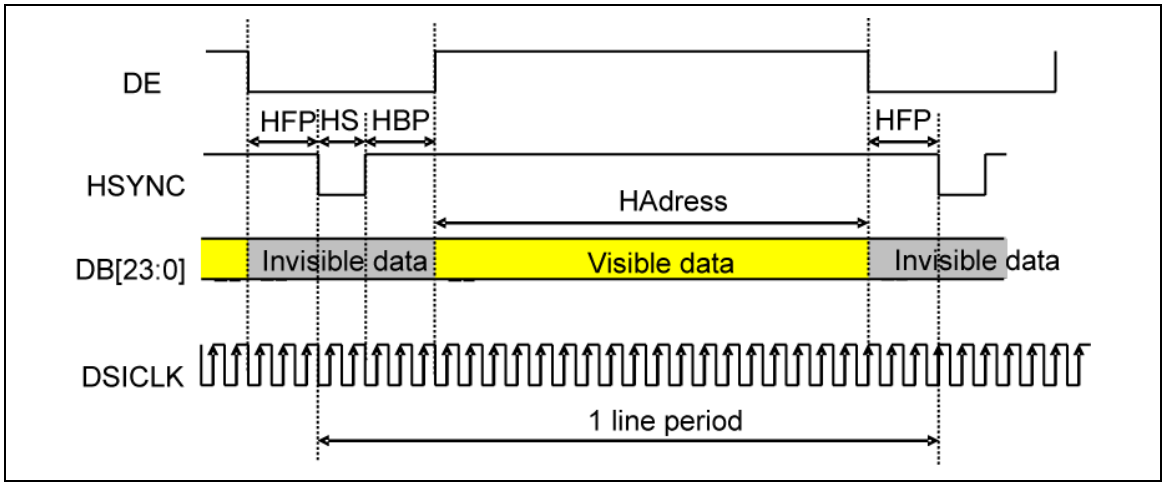


Figure 74

Table 27 Example of Horizontal Display Timing Setting

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Horizontal front porch	HFP		ByteClock	1lane: (TBD)	-	-	
Horizontal data start point	-	HS+HBP	ByteClock	DIV=0: (TBD) DIV=1: (TBD)	-	-	
Horizontal active area	HAdr		Pixel	(TBD)	320	320	

Note: fByteClock = (1/4)*fDSICLK. fByteClock is the frequency of ByteClock. In video mode, DSICLK is high-speed clock.

4) Burst Transfer

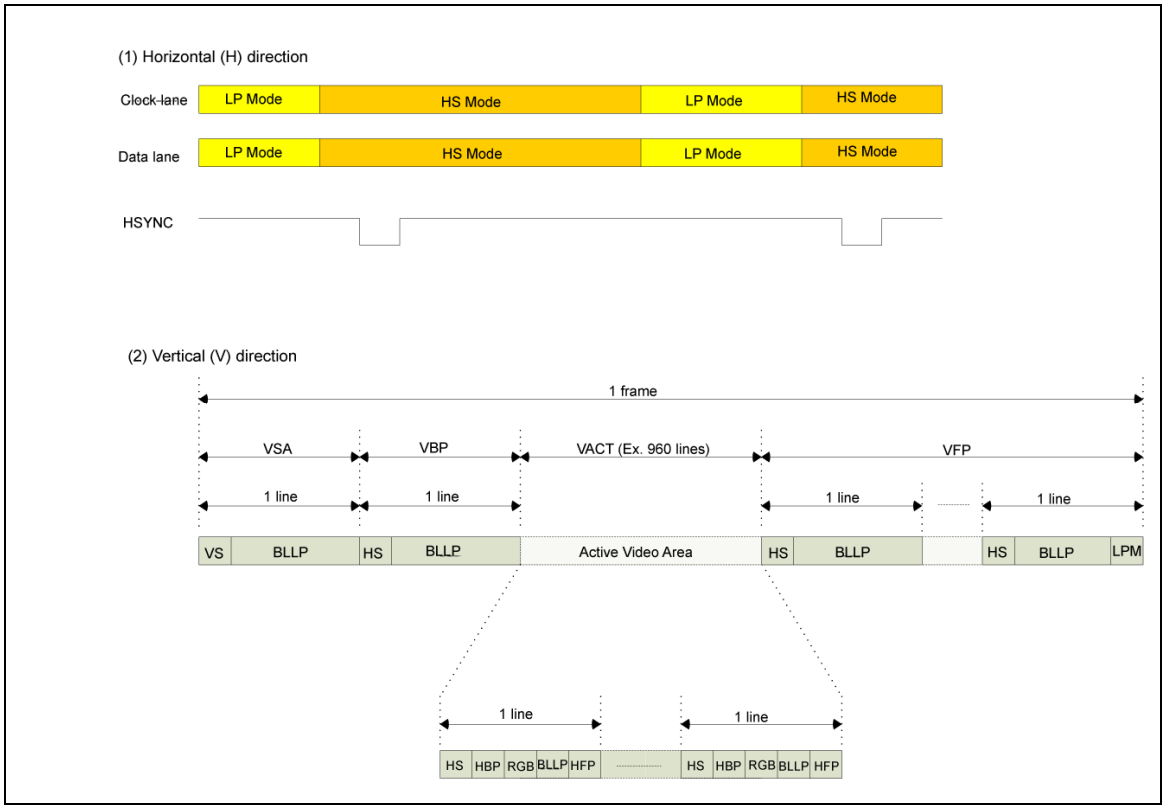


Figure 75

5) Packed Pixel Stream, 24-Bit Format, Long Packet, Data Type 11 1110 (3Eh)

Packet pixel stream of 24-bit format (packed) is a long packet. It is used to transmit image data formatted as 24-bit pixels to a display module in video mode. In this format, pixel boundaries are lined up with byte boundaries every three bytes.

This long packet shall be transmitted at a sufficient high rate (in HS mode) to avoid flickers or other visible artifacts.

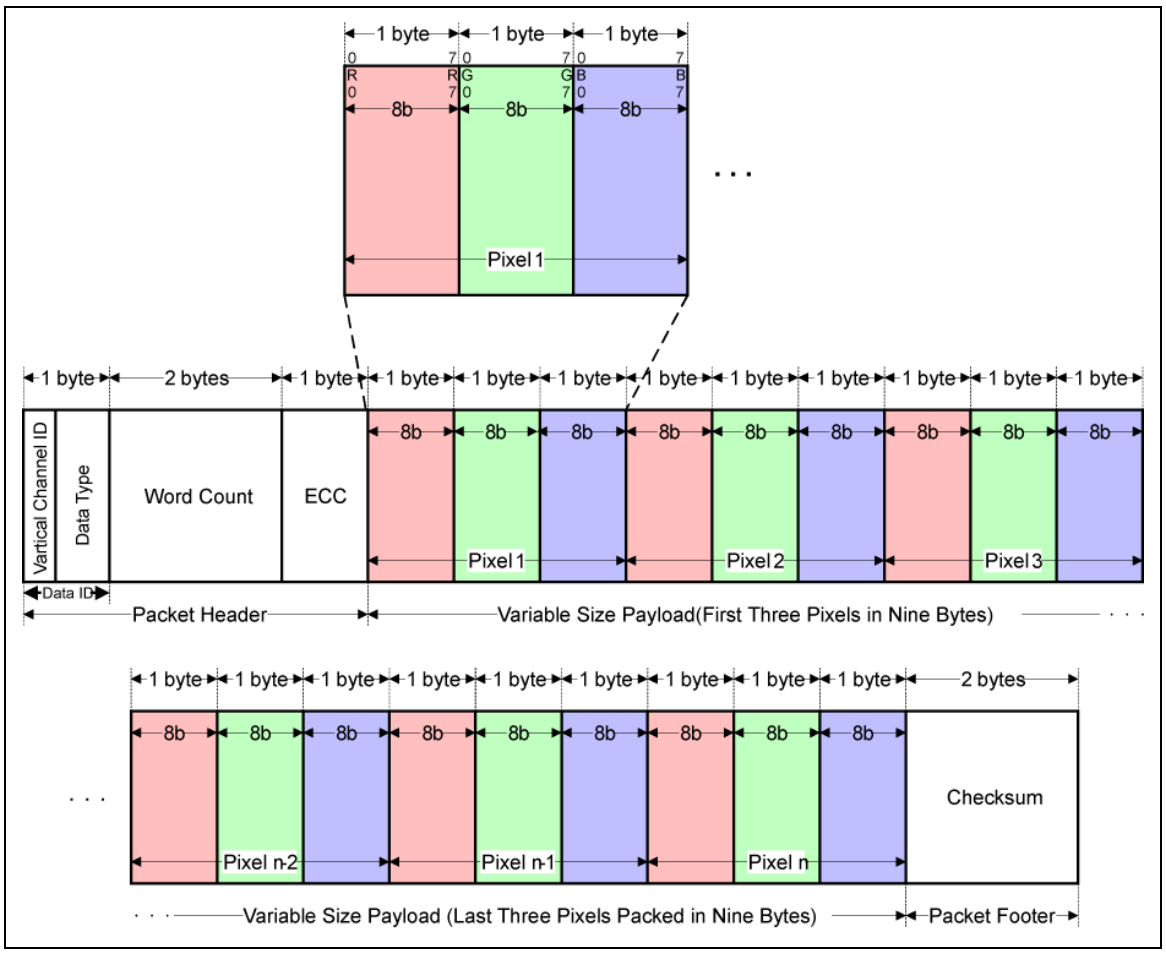


Figure 76 24bpp – RGB Color Format (Long Packet)

6) Pixel Stream, 18-Bit Format in Three Bytes, Long Packet, Data Type 10 1110 (2Eh)

Loosely packed pixel stream of 18-bit format is a long packet. It is used to transmit image data formatted as 18-bit pixels to a display module in video mode. In this format, pixel boundaries are lined up with byte boundaries every three bytes.

This long packet shall be transmitted at a sufficient high rate (in HS mode) to avoid flickers or other visible artifacts.

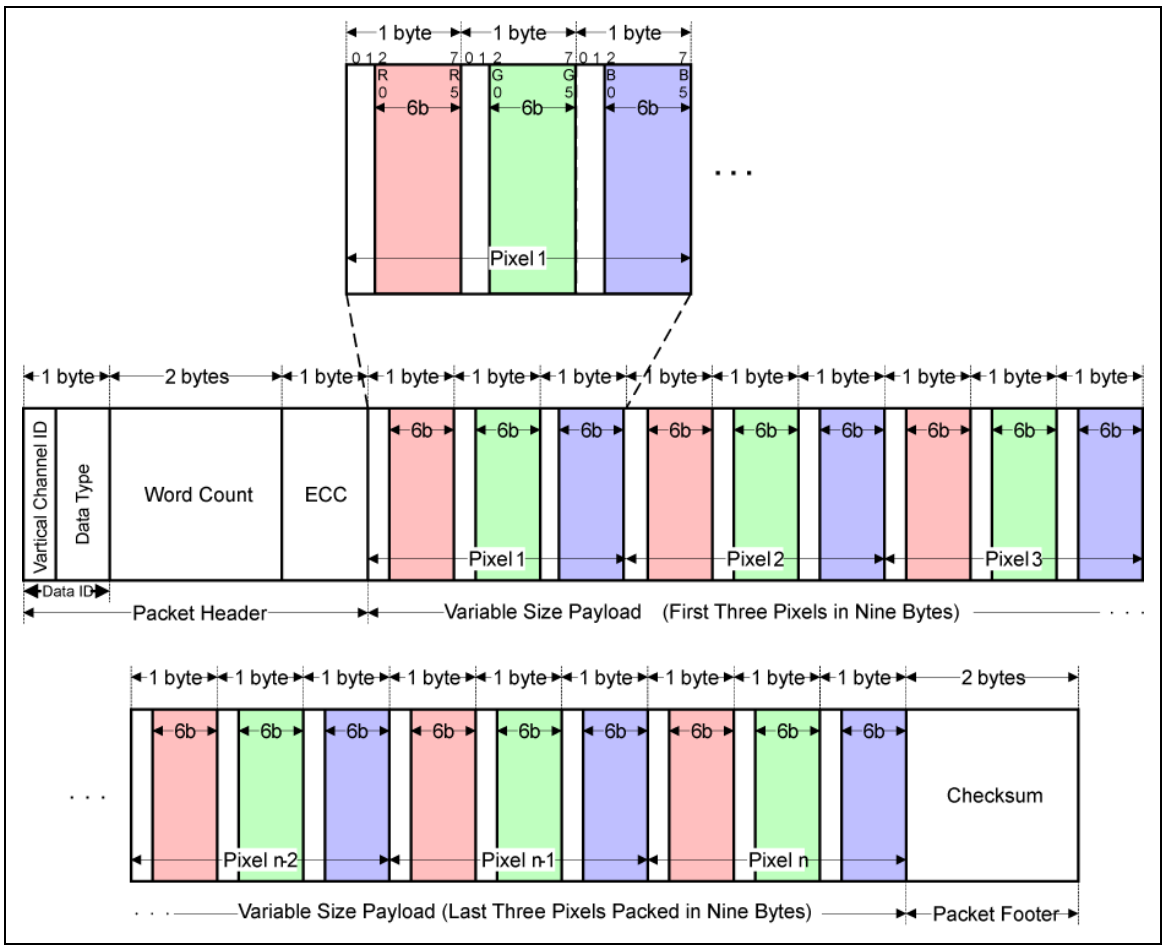


Figure 77 18bpp (Loosely Packed) – RGB Color Format (Long Packet)

7) Acknowledge with Error Report (AwER)

Table 28

Byte	Bit	Description		R61529 implementation	Note
Byte1 (Data0)	0	SoT Error	'0' fixed	No	
	1	SoT Sync Error	'0' fixed	No	
	2	EoT Sync Error	'0' fixed	No	
	3	Escape Mode Entry Command Error	1: Error, 0: No Error	Yes	
	4	Low-Power Transmit Sync Error	1: Error, 0: No Error	Yes	
	5	HS Receive Timeout Error	'0' fixed	No	
	6	False Control Error	'0' fixed	No	
	7	Reserved	'0' fixed	-	
Byte2 (Data1)	8	ECC Error, single-bit (detected, and corrected)	1: Error, 0: No Error	Yes	
	9	ECC Error, multi-bit (detected, not corrected)	1: Error, 0: No Error	Yes	
	10	Checksum Error (Long packet only)	1: Error, 0: No Error	Yes	
	11	DSI Data Type Not Recognized	1: Error, 0: No Error	Yes	
	12	DSI VC ID Invalid	1: Error, 0: No Error	Yes	
	13	Invalid Transmission Length	'0' fixed	No	
	14	Reserved	'0' fixed	-	
	15	DSI Protocol Violation	'0' fixed	No	

Note: Detailed error report condition is defined by R61529 (based on MIPI description).

8) DCS, MCS, and Data Type List

The following tables show available data type of each command (DCS and MCS).

Table 29 DCS and Data Type List

			Host to R61529 Data Type (RX)									
DCS Command/Parameter		W/R	Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
			DCS no para	DCS 1 para	DCS	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set max. return packet size
00h	nop	C	Yes	No	Yes	No	No	No	No	No	No	-
01h	soft_reset	C	Yes	No	Yes	No	No	No	No	No	No	-
04h	read_DDB_start	5	No	No	No	No	No	No	No	No	Yes	16'h5
0Ah	get_power_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Bh	get_address_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Ch	get_pixel_format	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Dh	get_display_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Eh	get_signal_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Fh	get_diagnostic_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
10h	enter_sleep_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
11h	exit_sleep_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
12h	enter_partial_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
13h	enter_normal_mode		Yes	No	Yes	No	No	No	No	No	No	-
20h	exit_invert_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
21h	enter_invert_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
28h	set_display_off	C	Yes	No	Yes	No	No	No	No	No	No	-
29h	set_display_on	C	Yes	No	Yes	No	No	No	No	No	No	-
2Ah	set_column_address	4	No	No	Yes	No	No	No	No	No	No	-
2Bh	set_page_address	4	No	No	Yes	No	No	No	No	No	No	-
2Ch	write_memory_start	N	No	No	Yes	No	No	No	No	No	No	-
2Eh	read_memory_start	N	No	No	No	No	No	No	No	No	Yes	N byte

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

Table 30 DCS and Data Type List (continued)

DCS Command/Parameter		W/R	Host to R61529 Data Type (RX)									
			Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
			DCS no para	DCS 1 para	DCS	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set max. return packet size
30h	set_partial_area	4	No	No	Yes	No	No	No	No	No	No	-
34h	set_tear_off	C	Yes	No	Yes	No	No	No	No	No	No	-
35h	set_tear_on (type 1)	1	No	Yes	Yes	No	No	No	No	No	No	-
36h	set_address_mode	1	No	Yes	Yes	No	No	No	No	No	No	-
38h	exit_idle_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
39h	enter_idle_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
3Ah	set_pixel_format	1	No	Yes	Yes	No	No	No	No	No	No	-
3Ch	write_memory_continue	N	No	No	Yes	No	No	No	No	No	No	-
3Eh	read_memory_continue	N	No	No	No	No	No	No	No	No	Yes	N byte
44h	set_tear_scanline	2	No	Yes	Yes	No	No	No	No	No	No	-
45h	get_scanline	2	No	No	No	No	No	No	No	No	Yes	16'h2
A1h	read_DDB_start	5	No	No	No	No	No	No	No	No	Yes	16'h5
A8h	read_DDB_continue	N	No	No	No	No	No	No	No	No	Yes	16'h5

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

Table 31 MCS and Data Type List

MCS Command / Parameter	W/R Data Type Packet	HOST→R61529 DataType（RX） Write Type 05'h Short DCS no para	15'h Short DCS 1para	39'h Long DCS -	13'h Short Generic 1para	23'h Short Generic 2para	29'h Long Generic -	Read Type 14'h Short Generic 1para	24'h Short Generic 2para	06'h Short DCS no para	Etc. 37'h Short set maximum return packet
B0h Manufacturer Command Access Protect	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
B1h Low Power Mode Control	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
B3h Frame Memory Access and Interface setting	2	No	No	No	No	No	Yes	Yes	No	No	16'h2
B5h Read Checksum and ECC Error Count	3	No	No	No	No	No	No	Yes	No	No	16'h3
B6h DSI Control	2	No	No	No	No	Yes	Yes	Yes	No	No	16'h2
B7h MDDI Control	4	No	No	No	No	Yes	Yes	Yes	No	No	16'h4
B8h Backlight Control(1)									No	No	16'h16
B9h Backlight Control(2)									No	No	16'h4
BAh Backlight Control(3)									No	No	16'h1
BDh RAM-SEG Control									?	?	16'h1
BFh Device code Read									No	No	16'h5
C0h Panel Driving Settin									No	No	16'h4
C1h Display V-Timing Se									No	No	16'h5
[redacted]									No	No	16'h13
C4h GIP Interface Mode	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
C5h Display H-Timing Setting	2	No	No	No	No	No	Yes	Yes	No	No	16'h2
C7h Display Control Setting	2	?	?	?	?	?	?	?	?	?	16'h2
C8h Gamma Setting A set	24	No	No	No	No	No	Yes	Yes	No	No	16'h18
C9h Gamma Setting B set	24	No	No	No	No	No	Yes	Yes	No	No	16'h18
CAh Gamma Setting C set	24	No	No	No	No	No	Yes	Yes	No	No	16'h18
D0h Power Setting (Charge Pump Setting)	12	No	No	No	No	No	Yes	Yes	No	No	16'hC
D3h Power Setting for Normal Mode	1	No	No	No	No	No	Yes	Yes	No	No	16'h1
D5h VCOM Setting	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
DAh Manual Sequence Control	1	?	?	?	?	?	?	?	?	?	16'h1
E0h											

TBD

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

(14) DSI Data Format

The R61529 supports color formats shown below.

Table 32

Type	IM3-0	Data pin	Color format	MIPI Spec.	R61529 implementation
DSI	0011/1011	DATA0P,DATA0N	16bpp	Yes	No
			18bpp (Loosely packed)	Yes	Yes
			18bpp (Packed)	Yes	No
			24bpp	Yes	Yes

Yes: Supported

No: Unsupported

MDDI (Mobile Display Digital Interface)

MDDI (Mobile Display Digital Interface) is a differential small amplitude serial interface for high-speed data transfer via Stb+/- (STB_CLKP and STB_CLKN) and Data0+/- (DATA0P and DATA0N). High-speed data can be also transferred via only by Stb+/- and Data0+/-. The specifications of MDDI supported by the R61529 are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following are the specifications particular to the R61529's MDDI. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

R61529's MDDI Specifications

- MDDI Type 1 (1 data lane)
- High-speed, differential, small-amplitude data transfer via Stb+/- and Data0+/- lines
- MDDI client: the R61529 enables direct connection to the base band (BB) chip without bridge chip
- Active Refresh Mode

  Video data received via MDDI is directly output as display data without being written to internal RAM.
- Cost-performance optimized interface for mobile display systems

1. Internal mode (one client), Forward Link (Type 1), and Reverse Link (Type 1) are supported
2. Hibernation mode to save power consumption
3. Tearing-free moving picture display via TE interface
4. Moving picture display with low power consumption, realized by the features 2 and 3
5. Shutdown mode for saving power consumption in the standby state
6. Providing one-chip solution for MDDI mobile display systems

Note: In the specification for MDDI, shutdown refers to DSTB (deep standby mode).

- B5 of set_address_mode command (36h): Setting to only 0 (horizontal direction) is supported
- RAM window address setting

  set_column_address (2Ah)

  SC[9:0] = 2n (n = 0, 1, 2, …159)
  EC[9:0] = 2m – 1 (m = 1, 2, …160)
  EC – SC > 2 pixels

Example of MDDI Connection of the R61529

The R61529 incorporates terminal resistors for differential input pins (DATA0P, DATA0N, STB_CLKP, and STB_CLKN).

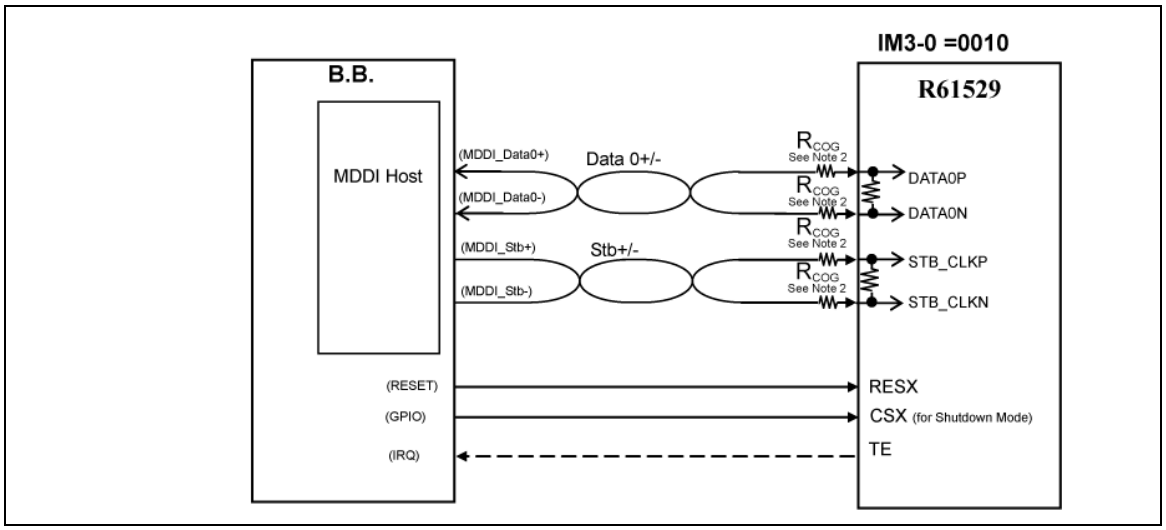


Figure 78

Note: Make the COG wiring resistances of Data0+/-, and Stb+/- lines as small as possible (R_{COG} < 10 ohm).

MDDI Link Protocol (Packets Supported by the R61529)

The MDDI packets supported by the R61529 are as follows. Do not send packets not supported by the R61529 in the system incorporating the R61529.

- Sub-Frame Header Packet
- Filler Packet
- Reverse Link Encapsulation Packet
- Link Shutdown Packet
- Round-Trip Delay Measurement Packet
- Forward Link Skew Calibration Packet
- Video Stream Packet
- Client Capability Packet
- Client Request and Status Packet
- Register Access Packet

Sub-Frame Header Packet

The Sub-Frame Header Packet is the first packet of every sub-frame. The Sub-Frame Header Packet is required for host-client synchronization.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2	(0x14)										
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x3bff)										
5	Unique Word								2 bytes	←	Specifies 32-bit Unique Word by the combination of Packet Type and Unique Word.
6	(0x5a)										
7	Reserved 1								2 bytes	←	Reserved for future use and must be set to 0x00.
8	(0x00)										
9	Sub-frame Length								4 bytes	←	Specifies the number of bytes per sub-frame.
10											
11											
12											
13	Protocol Version								2 bytes	←	Specifies the protocol version used by the host.
14											
15	Sub-frame Count								2 bytes	←	Specifies the number of sub-frames that have been transmitted. (0 ~ +1)
16											
17	Media-frame Count								4 bytes	←	Specifies the number of media-frames that have been transmitted. (0 ~ +1)
18											
19											
20											
21	CRC								2 bytes	←	CRC. Used to detect errors.
22											

Figure 79 Sub-Frame Header Packet

Protocol Version[15:0]

[15:2] – Reserved for future use. These should be set to 0x0.

[1:0] – Specifies Sub-frame length

00 – Sub-frame length strictly followed.

01 – Sub-frame length is flexible. Sub-frame length specified by Sub-Frame Header Packet is enabled.

10 – Sub-frame length is unlimited. No more Sub-Frame Header Packets are required to be transmitted following the first Sub-Frame Header Packet after an exit from a hibernation state.

Filler Packet

The Filler Packet is sent when no other information is available to be sent on the forward or reverse link. It is recommended to send Filler Packets with minimum length to allow maximum flexibility to send other packets when required.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2											
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x00)										
5	Filler Bytes (All zero)								x bytes	←	Specifies the number of all zero bytes only as needed. Filler Packet with minimum length can be transmitted without Filler Bytes by setting this field to 0 bytes.
:	(Packet Length – 4 bytes)										
n-2											
n-1	CRC								2 bytes	←	CRC. Used to detect errors.
n											

Figure 80 Filler Packet

Link Shutdown Packet

The Link Shutdown Packet is sent from the host to the client to indicate that the MDDI data and strobe will be shut down and go into a hibernation state. Normal operation is resumed when the link is restarted and the host sends packets to the client that is in a hibernation state.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2	(0x14)										
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x45)										
5	CRC								2 bytes	←	Used to detect byte errors in the Packet Length to the Packet Type.
6											
7	All zero								16 bytes	←	The number of all zero bytes.
:	(0x00)										
22											

Figure 81 Link Shutdown Packet

Round-Trip Delay Measurement Packet

The Round-Trip Delay Measurement Packet is used to measure the propagation delay from the host to the client plus the delay from the client back to the host. This measurement inherently includes all of the delays that exist in the line drivers and receivers and the interconnect subsystem. This measurement is used to set the turnaround delay and reverse link rate divisor parameters in the Reverse Link Encapsulation Packet.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2	(0xC8)										
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x52)										
5	hClient ID								2 bytes	←	Reserved for the Client ID. Must be set to 0x00.
6	(0x00)										
7	Parameter CRC								2 bytes	←	Used to detect byte errors in the Packet Length to the Client ID.
8											
9	Guard Time 1								64bytes		
:											
72											
73	Measurement Period								64bytes	←	Enables MDDI_Data line drivers when bits are set to 0.
:											
136											
137	All Zero								2 bytes	←	Identifies the round trip delay of the link plus logic delay after the first bit of Measurement Period.
138	(0x00)										
139	Guard Time 2								64bytes		
:											
202											

Figure 82 Round-Trip Delay Measurement Packet

Forward Link Skew Calibration Packet

This packet allows the client to calibrate itself for differences in the propagation delay of the MDDI_Data signals with respect to the MDDI_Stb signal.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2	(0x56)										
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x53)										
5	hClient ID								2 bytes	←	Reserved for the Client ID. Must be set to 0x00.
6	(0x00)										
7	Parameter CRC								2 bytes	←	Used to detect byte errors in the Packet Length to the Client ID.
8											
9	All Zero 1								8 bytes		
10	(0x00)										
11											
12											
13											
14											
15											
16											
17	Calibration Data Sequence (0xAA or 0x55)								64 bytes		
80											
81	All Zero 2								8 bytes		
:	(0x00)										
:											
88											

Figure 83 Forward Link Skew Calibration Packet

Reverse Link Encapsulation Packet

Data is transferred in the reverse direction using the Reverse Link Encapsulation Packet. When a forward link packet is sent, MDDI link is turned around in the middle of this packet so that packets can be sent in the reverse direction.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2											
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x41)										
5	hClient ID								2 bytes	←	Reserved for the Client ID. Must be set to 0x00.
6	(0x00)										
7	Reverse Link Flags								1 byte	←	Specifies kinds of data output to the Reverse Link Data Packets field.
8	Reverse Rate Divisor								1 byte	←	Specifies Reverse Link Data transfer rate.
9	Turn-Around 1 Length								1 byte	←	Specifies the total number of bytes that are allocated for Turn-Around 1 (X).
10	Turn-Around 2 Length								1 byte	←	Specifies the total number of bytes that are allocated for Turn-Around 2 (Y).
11	Parameter CRC								2 bytes	←	Used to detect byte errors in the Packet Length to the Turn-Around 2.
12											
13	All Zero 1								8 bytes	←	Ensures that all MDDI_Data signals are at a logic-zero level for a sufficient time to allow the client to begin recovering clock using only MDDI_Stb.
14											
15											
16											
17											
18											
19											
20											
	Turn-Around 1 (X byte)								x bytes	←	First turnaround period. The number of bytes specified by the Turn-Around 1 Length parameter is allocated to allow the MDDI_Data line drivers in the client to enable before the line drivers in the host are disabled.
	Reverse Data Packets (Packet Length - X - Y - 26 bytes)								x bytes	←	A series of data packets transferred from the client to host. The client sends Filler Packets as if it drove MDDI_Data lines at a logic-zero level when it has no data to send to the host.

Figure 84 Reverse Link Encapsulation Packet

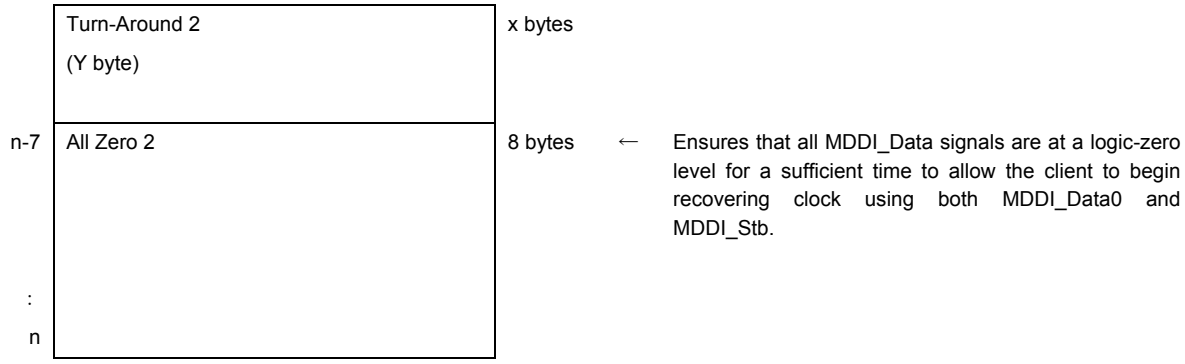


Figure 85 Reverse Link Encapsulation Packet (continued)

Reverse Link Flags[7:0]

[7:2]: Reserved for future use. These should be set to 0x0.

[1:0]: The host requests the client to transfer Client Request and Status Packet or Client Capability Packet via Reverse Data Packets Field.

00: Register Read Response.

01: Client Request and Status Packet.

10: Client Capability Packet.

11: Client Capability Packet + Client Request and Status Packet

Reverse Rate Divisor[7:0]

Specifies the number of MDDI_Stb cycles per Reverse Link Data Clock. This number is twice as much as a value set by Reverse Rate Divisor[7:0]. Unlike Forward Link, Reverse Link Data Clock operates at Single Data Rate (SDR: used only on a rising edge). Select a value from 02h (Forward Link data transfer rate / 4), 04h (Forward Link data transfer rate / 8), 08h (Forward Link data transfer rate / 16), or 10h (Forward Link data transfer rate / 32).

Turn-Around 1 Length[7:0]

Specify the number of bytes required for the MDDI_Data drivers in the host to disable their outputs.

Turn-Around 2 Length[7:0]

Specify the number of bytes required for the MDDI_Data drivers in the host to disable their outputs.

Register Access Packet

Client registers in the client are accessed via the Register Access Packet.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2											
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x92)										
5	hClient ID								2 bytes	←	Reserved for the Client ID. Must be set to 0x00.
6	(0x00)										
7	Read/Write Info								2 bytes	←	Specifies the specific packet as either a write, or a read, or a response to a read.
8											
9	Register Address								4 bytes	←	Register address.
10											
11											
12											
13	Parameter CRC								2 bytes	←	CRC. Used to detect errors.
14											
	Register Data List (Packet Length - 14bytes)								x bytes	←	4-byte data that are written to or read from client registers.
	Register Data CRC								2 bytes	←	CRC. Used to detect errors.

Figure 86 Register Access Packet

Read/Wrote Info[15:0]

Specifies the specific packet as either a write, or a read, or a response to a read.

[13:0]: Specifies the number of 32-bit Register Data List items to be transferred in the Register Data List field.

[15:14]:

00: Writes Register Data List field value (32 bits) to registers specified by Register Address field. Bits[13:0] specify the number of 32-bit register data items that are contained in the Register Data List field to be written to registers starting at the register specified by the Register Address field.

10: Requests registers of addresses specified by Register Address field. Bits[13:0] indicate the number of items register read is requested according to Register Address field. Register Data List field should be set to 0 bytes.

11: Indicates that the packet is data read according to request that [15:14] = 0. The Register Data List field contains addresses and read data of registers corresponding to the first Register Data List item. Bits[13:0] indicate the number of 32-bit register data items that have been read from registers specified by the Register Address field.

01: Reserved for future use. Setting inhibited.

Video Stream Packet

The R61529 writes image data to Frame memory via Video Stream Packet. The window and Frame memory addresses are set via Video Stream Packet.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2											
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x10)										
5	hClient ID								2 bytes	←	Reserved for the Client ID. Must be set to 0x00.
6	(0x00)										
7	Video Data Format Descriptor								2 bytes	←	Specifies the format of each pixel in the Pixel Data in the present stream in the present data.
8											
9	Pixel Data Attributes								2 bytes	←	Specifies where pixel data is transferred.
10											
11	X Left Edge								2 bytes	←	Specifies a column start address in frame memory access area.
12											
13	Y TOP Edge								2 bytes	←	Specifies a row start address in frame memory access area.
14											
15	X Right Edge								2 bytes	←	Specifies a column end address in frame memory access area.
16											
17	Y Bottom Edge								2 bytes	←	Specifies a row end address in frame memory access area.
18											
19	X Start								2 bytes	←	Specifies a column start address that Pixel Data is written.
20											
21	Y Start								2 bytes	←	Specifies a row start address that Pixel Data is written.
22											
23	Pixel Count								2 bytes	←	Specifies the number of pixels in the Pixel Data Field.
24											
25	Parameter CRC								2 bytes	←	Used to detect byte errors in Packet Length to Pixel Count.
26											
27	Pixel Data								x bytes	←	Pixel Data
:	(Packet Length - 26 bytes)										
n-2											
n-1	Pixel Data CRC								2 bytes	←	CRC. Used to detect errors.
n											

Figure 87 Video Stream Packet

Video Data Format Descriptor[15:0]

[15:13]: Specifies the format of each Pixel Data.

[12]: Specifies whether the Pixel Data is packed or unpacked (how redundant bits are packed in bytes in Pixel Data transfer)..

0: Each pixel in the Pixel Data field is byte-aligned with an MDDI byte boundary. (The Pixel Data is unpacked)

1: Each pixel in the Pixel Data is packed up against the previous pixel leaving no unused.

[11:0]: Specifies the number of bits per pixel in the Pixel Data.

Table 33

[15:13]	[12]	[11:8]	[7:4]	[3:0]	Format
000		—	—	—	Monochrome format (Setting inhibited)
001		—	—	—	Color map format (Setting inhibited)
010	1	0x5	0x6	0x5	16bpp (Packed) RGB format (R:G:B=5:6:5)
	1	0x6	0x6	0x6	18bpp (Packed) RGB format （R:G:B=6:6:6）
	1	0x8	0x8	0x8	24bpp RGB format (R:G:B=8:8:8)
011		—	—	—	YUV422 format (Setting inhibited)
100		—	—	—	Bayer format (Setting inhibited)

Note: Video Stream Packet of the R61529 supports Forward Link, not Reverse Link. Read data from frame memory via Register Access Packet.

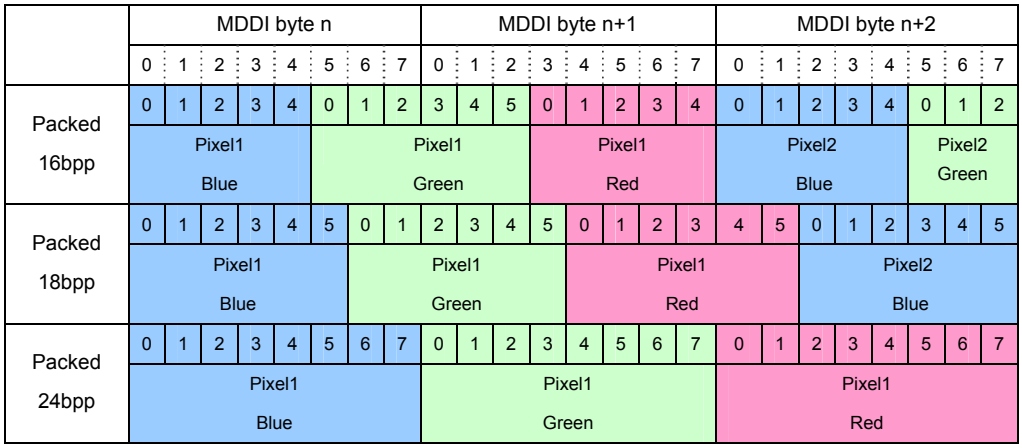


Figure 88

Pixel Data Attributes[15:0]

[15]: Indicates that the row of pixels in the Pixel Data field is the last row of pixels in a frame of data when bit 15 is set to 1.

[14]: Reserved for future use and must be set to 0.

[13:12]: Specifies how transparent data is written to the destination locations. (Transparent data is not used. Set to 00)

[11:8]: Specifies the alternate display number. (The number is not used. Set to 00)

[7:6]: Specifies the destination locations to which the Pixel Data is written. (The data is written to frame memory. Set to 0)

[5]: Specifies whether the Pixel Data is consecutive Frame Data of the Pixel Data that has been transferred.

0: Settings of X Left Edge, Y Top Edge, X Right Edge, Y Bottom Edge, X Start and Y Start are enabled.

1: Settings of X Left Edge, Y Top Edge, X Right Edge, Y Bottom Edge, X Start and Y Start are disregarded.

[4]: Specifies whether the Pixel Data is camera data or display data. (Data is display data. Set to 0)

[3]: Specifies whether the Pixel Data is Alternate Pixel Format or not. (Usual format is used. Set to 0)

[2]: Specifies whether the Pixel Data supports an interlace format or not. (Interlace format is not supported. Set to 0)

[1:0]: Specifies how the Pixel Data of stereo image is transferred. (Stereo image is not supported. Set to 11)

X Left Edge: X Left Edge represents addresses at a start of the window address area in horizontal direction. SC setting is updated.
Y Top Edge: Y Top Edge represents addresses at a top of the window address area in vertical direction. SP setting is updated.
X Right Edge: X Right Edge represents addresses at an end of the window address area in horizontal direction. EC setting is updated.
Y Bottom Edge: Y Bottom Edge represents addresses at a bottom of the window address area in vertical direction. EP setting is updated.

Client Capability Packet

The Client Capability Packet informs the host of the capabilities of the client so it can configure the host-to-client link in an optimum manner. The host can request the client to transmit this packet to the host client via the Reverse Link Flags in the Reverse Link Encapsulation Packet.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2	(0x4A)										
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x42)										
5	hClient ID								2 bytes	←	Reserved for the Client ID. Returns 0x00.
6	(0x00)										
7	Protocol Version								2 bytes	←	Specifies the protocol version used by the client. Set to 1 or more.
8	(0x01)										
9	Min Protocol Version								2 bytes	←	Specifies the minimum protocol version used by the client.
10	(0x01)										
11	Pre-calibration Data Rate Capability								2 bytes	←	Specifies the maximum data rate the client can receive on each data pair on the forward MDDI link prior to performing forward link skew calibration. The rate is specified as the number of million bits per second (Mbps).
12	(0x17C) (TBD)										
13	Interface Type Capability (0x00)								1 byte	←	Specifies the interface types that are supported on the forward and reverse links.
14	Number of All Displays (0x00)								1 byte	←	Specifies the number of alternate displays supported by the client. Unused. Returns 0x00.
15	Post-calibration Data Rate Capability								2 bytes	←	Specifies the maximum data rate the client can receive on each data pair on the forward MDDI link after performing forward link skew calibration. The rate is specified as the number of million bits per second (Mbps).
16	(0x17C) (TBD)										
17	Bitmap Width								2 bytes	←	Specifies the width of the bitmap of frame memory in the client expressed as the number of pixels.
18	(0x13F)										
19	Bitmap Height								2 bytes	←	Specifies the height of the bitmap of frame memory in the client expressed as the number of pixels.
20	(0x1DF)										
21	Display Window Width								2 bytes	←	Specifies the width of the display window in the client as the number of pixels.
22	(0x13F)										
23	Display Window Height								2 bytes	←	Specifies the height of the display window in the client expressed as the number of pixels.
24	(0x1DF)										
25	Color Map Size								4 bytes	←	Specifies the number of available color map tables in the client. Not used. Set to 0x00.
26	(0x0000)										

Figure 89 Client Capability Packet

27				
28				
29	Color Map RGB Width	2 bytes	←	Specifies the number of bits of the red, green, and blue color components that is used in the color map display mode. Unused. Returns 0x00.
30	(0x00)			
31	RGB Capability	2 bytes	←	Specifies the number of bits of resolution that can be displayed in RGB format.
32	(0x8888)			
33	Monochrome Capability (0x00)	1 byte	←	Specifies the number of bits of resolution that can be displayed in monochrome format. Unused. Returns 0x00.
34	Reserved 1(0x00)	1 byte	←	Reserved for future use. Returns 0x00.
35	Y Cb Cr Capability	2 bytes	←	Specifies the number of bits of resolution that can be displayed in Y Cb Cr format. Unused. Returns 0x00.
36	(0x00)			
37	Bayer Capability	2 bytes	←	Specifies the number of bits of resolution, pixel group, and pixel order that can be transferred in Bayer format. Unused. Returns 0x00.
38	(0x00)			
39	Reserved 2	2 bytes	←	Reserved for future use. Returns 0x00.
40	(0x00)			
41	Client Feature Capability (TBD.)	4 bytes	←	Capabilities supported by the client.
42				
43				
44				
45	Max Video Frame Rate (0x3C) (TBD.)	1 byte	←	Specifies the maximum video frame update capability of the client in frames per second. The host needs to update the image at a rate less than or equal to the value specified in this field. .
46	Min Video Frame Rate (0x00)	1 byte	←	Specifies the minimum video frame update capability of the client in frames per second. The host needs to update the image at a rate greater than or equal to the value specified in this field. .
47	Min Sub-frame Rate	2 bytes	←	Specifies the minimum sub-frame rate in frames per second.
48	(0x01)			
49	Audio Buffer Depth	2 bytes	←	Specifies the depth of the elastic buffer in the client dedicated to each audio stream. Unused. Returns 0x00.
50	(0x00)			
51	Audio Channel Capability	2 bytes	←	Contains a group of flags that indicate which audio channels are supported by the client. Unused. Returns 0x00.
52	(0x00)			

Figure 90 Client Capability Packet (continued)

53	Audio Sample Rate Capability	2 bytes	←	Contains a set of flags that indicate the audio sample rate capability of the client. Unused. Returns 0x00.
54	(0x00)			
55	Audio Sample Resolution (0x00)	1 byte	←	Specifies the number of bits per audio sample that must be sent to the client in an Audio Stream Packet. Unused. Returns 0x00.
56	Mic Audio Sample Resolution (0x00)	1 byte	←	Specifies the number of bits per audio sample that the Mic must send to the host in an Audio Stream Packet. Unused. Returns 0x00.
57	Mic Sample Rate Capability	2 bytes	←	Contains a set of flags that indicate the audio sample rate capability of the microphone in the client. Unused. Returns 0x00.
	(0x00)			
58				
59	Keyboard Data Format (0x00)	1 byte	←	Specifies whether a keyboard is connected to the client system and the type of keyboard that is connected. Unused. Returns 0x00.
60	Pointing Device Data Format (0x00)	1 byte	←	Specifies whether a pointing device is connected to the client system and the type of pointing device that is connected. Unused. Returns 0x00.
61	Content Protection Type	2 bytes	←	A set of flags to indicate the type of digital content protection that is supported by the client. Unused. Returns 0x00.
	(0x00)			
62				
63	Mfr Name	2 bytes	←	3-character ID of manufacturer. Unused. Returns 0x00.
64	(0x00)			
65	Product Code	2 bytes	←	Product code assigned by the display manufacturer.
66	(0x1529)			
67	Reserved 3	2 bytes	←	Reserved for future use. Returns 0x00.
68	(0x00)			
69	Serial Number	4 bytes	←	Specifies the serial number of the display. Unused. Returns 0x00.
70	(0x0000)			
71				
72				
73	Week of Mfr (0x00)	1 byte	←	Defines the week of manufacture of the display. Unused. Returns 0x00.
74	Year of Mfr (0x00)	1 byte	←	Defines the year of manufacture of the display. Unused. Returns 0x00.
75	CRC	2 bytes	←	CRC. Used to detect errors.
76				

Figure 91 Client Capability Packet (continued)

Interface Type Capability[7:0]

A bit set to 1 indicates that the specified interface type is supported, and a bit set to 0 indicates that the specified interface type is not supported. All hosts and clients must support at least Type 1 on the forward and reverse links.

[0]: Type 2 is supported on the forward link. (This bit is not used. 0 is returned)

[1]: Type 3 is supported on the forward link. (This bit is not used. 0 is returned)

[2]: Type 4 is supported on the forward link. (This bit is not used. 0 is returned)

[3]: Type 2 is supported on the reverse link. (This bit is not used. 0 is returned)

[4]: Type 3 is supported on the reverse link. (This bit is not used. 0 is returned)

[5]: Type 4 is supported on the reverse link. (This bit is not used. 0 is returned).

[7:6]: Reserved for future use. 0 is returned.

RGB Capability[15:0]

The number of bits of resolution that can be displayed in RGB format is specified. A bit set to 1 indicates that the specified resolution is supported, and a bit set to 0 indicates that the specified resolution is not supported.

[3:0]: Specifies the maximum number of bits of blue (the blue intensity) in each pixel.

[7:4]: Specifies the maximum number of bits of green (the green intensity) in each pixel.

[11:8]: Specifies the maximum number of bits of red (the red intensity) in each pixel.

[13:12]: Reserved for future use. 0x0 is returned.

[14]: Specifies whether the client supports unpacked RGB format.

1: The client supports unpacked RGB format.

0: The client does not support unpacked RGB format.

[15]: Specifies whether the client supports packed RGB format.

1: The client supports packed RGB format.

0: The client does not support packed RGB format.

In unpacked format, pixel data is transferred with bits unpacked into space within a byte in the data. In packed format, pixel data is transferred with bits packed into space within a byte in the data.

Client Feature Capability[31:0]

Whether specific features in the client are supported is specified. A bit set to 1 indicates the capability is supported, and a bit set to 0 indicates the capability is not supported.

[0]: The Bitmap Block Transfer Packet. (This bit is not used. 0 is returned)

[1]: The Bitmap Area Fill Packet. (This bit is not used. 0 is returned)

[2]: The Bitmap Pattern Fill Packet. (This bit is not used. 0 is returned)

[3]: The Read Frame Buffer Packet. (This bit is not used. 0 is returned)

[4]: The Transparent Color and Mask Setup Packet. (This bit is not used. 0 is returned)

[5]: Audio data in unpacked format. (This bit is not used. 0 is returned)

[6]: Audio data in packed format. (This bit is not used. 0 is returned)

[7]: Reverse-link video stream data from a camera. (This bit is not used. 0 is returned)

[8]: The client has the ability to receive a full line of pixel data and ignore display addressing as specified by bit 5 of the Pixel Data Attributes field of the Video Stream Packet, and the client can also detect frame sync or end of video frame data via bit 15 of the Pixel Data Attributes field.

[9]: The Display Power State Packet. (This bit is not used. 0 is returned)

[10]: Display power state 01 defined by the Power State field of the Display Power State Packet. (This bit is not used. 0 is returned)

[11]: Communication with a point device to send and receive Pointing Device Data Packets. (This bit is not used. 0 is returned)

[12]: Communicating with a keyboard to send and receive Keyboard Data Packets. (This bit is not used. 0 is returned)

[13]: Audio or video parameters supported by the VCP Feature Packets. (This bit is not used. 0 is returned)

[14]: Writing pixel data into the offline display frame buffer. (This bit is not used. 0 is returned)

[15]: Writing pixel data into only the display frame buffer currently being used to refresh the display image. (This bit is not used. 0 is returned)

[16]: Writing pixel data from a single Video Stream Packet into all display frame buffers. (This bit is not used. 0 is returned)

[17]: The Request Specific Status Packet. (This bit is not used. 0 is returned)

[18]: The Round-Trip Delay Measurement Packet. (This bit can be used. 1 is returned)

[19]: The Forward Link Skew Calibration Packet. (This bit can be used. 1 is returned)

[20]: Response to Valid Status Reply List Packet according to Request Specific Status Packet. (This bit is not used. 0 is returned)

[21]: The Bitmap Block Transfer Packet, Bitmap Area Fill Packet, and Bitmap Pattern Fill Packet. (This bit is not used. 0 is returned)

[22]: The Register Access Packet. (This bit can be used. 1 is returned)

[23]: Decoding enhanced Video Stream Packets. (This bits is not used. 0 is returned) This packet includes the Windowless Video Packet as well as the Flexible Video Stream Packet.

[24]: The Enhanced Reverse Encapsulation Packet. (This bit is not used. 0 is returned)

[25]: Freezing the state. (This bit is not used. 0 is returned)

[31:26]: Reserved for future use. 0x0 is returned.

Client Request and Status Packet

This packet is the minimum information including error and status needed so that the host can configure the host-to-client link in an optimum manner. The client sends this packet as the first packet when the host requests the Reverse Link Encapsulation Packet or Enhanced Reverse Link Encapsulation Packet. This packet is required by the host via the Reverse Link Flags n the Reverse Link Encapsulation Packet.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2											
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x46)										
5	hClient ID								2 bytes	←	Reserved for the Client ID. Returns 0x00.
6	(0x00)										
7	Reverse Link Request								2 bytes	←	Specifies the number of bytes the client needs in the reverse link in the next sub-frame to send information to the host.
8											
9	CRC Error Count								1bytes	←	Indicates the number of CRC errors that have occurred since the last Client Request and Status Packet is sent. The number is reset to 0 each time this packet is sent. If the number of CRC errors exceeds 255, 255 is returned.
10	Client Status (0x00)								1bytes	←	A group of flags that indicates the current status of the client device. Not used. Returns 0x00.
11	Client Busy Flags (0xFFFF)								2 bytes	←	A set of busy flags to indicate that the client is performing a specific function and is not ready to accept another packet related to that function. Not used. Returns 0xFFFF.
12											
13	CRC								2 bytes	←	CRC. Used to detect errors.
14											

Figure 92

Client Status[7:0]

[0]: Indicates that there has been a change in the capability of the client. This could be due to the user connecting a peripheral device such as a microphone, keyboard, or display, or some other reason.

1: Capability has changed. Examine the Client Capability Packet to determine the new client characteristics.

0: Capability has not changed since the last Client Capability Packet was sent.

[1]: Indicates that the client device has detected an error in processing a packet since the last Client Capability Packet was sent.

[7:2]: Reserved for future use. 0x0 is returned.

Client Busy Flags[15:0]

A set of busy flags to indicate that the client is performing a specific function and is not ready to accept another packet related to that function. A bit set to 1 indicates that the particular function is currently being performed by the client and the related function in the client is busy and returns 1. A bit set to 0 indicates that the related function in the client is ready and returns 0. The client must always return a busy status (bit set to 1) for all functions that are not supported in the client.

[0]: Bitmap block transfer function is busy.

[1]: Bitmap area fill function is busy.

[2]: Bitmap pattern fill function is busy.

[3]: The graphic subsystem is busy performing an operation that requires use of the frame buffer in the client.

[15:4]: Reserved for future use. 0x00 is returned.

MDDI Command Setting

When MIPI command is issued, set a parameter to 00h. When transferring a multiple number of command sets, they must be transferred in the same number of Register Access Packets.

Table 34

Register Access Packet Parameter	Register Setting
Read/Write Info[15:0]	0 x 0000
Register Address[31:0]	24'h000000+CMD[7:0]
Register Data (1)[31:0]	32'h00000000

Table 35

Register Access Packet Parameter	Register Setting
Read/Write Info[15:0]	0 x 000n
Register Address[31:0]	24'h000000+CMD[7:0]
Register Data(1)[31:0]	24'h000000+PRM(1)[7:0]
:	:
Register Data(n)[31:0]	24'h000000+PRM(n)[7:0]

Shutdown Mode Setting

The R61529's Client MDDI supports Shutdown setting to bring the R61529 to the standby state to save power consumption during Hibernation.

By setting DSTB = 1 and sending Shutdown Packet, MDDI enters the Hibernation state. The Client MDDI's standby power requirement can be reduced while MDDI Link is maintained in the Hibernation state.

In Shutdown mode, the R61529 halts operation other than maintaining Hibernation state. In canceling Shutdown mode, execute HWRESET or input "Low" pulse 6 times from CSX pin. After canceling Shutdown mode, cancel the Hibernation state by Host-initiated Wake up.

For Shutdown Mode setting sequence, see "Deep Standby Mode / Shutdown Mode (MDDI) On/Off Sequence."

In Shutdown mode, command setting and Frame memory data are not retained and they must be reset after canceling the Hibernation state.

When setting and canceling the Hibernation state, follow the sequence as specified in the MDDI specifications by VESA.

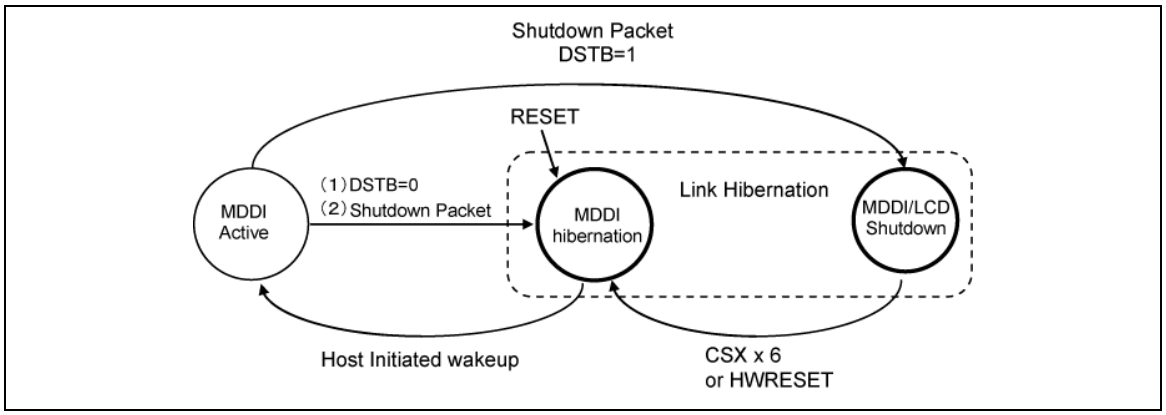


Figure 93 State Transitions in Shutdown Mode

CRC Error Detection Mode Setting

CRC error detection mode can be set by command. When this mode is set, CRC error is detected and an output level of the DIN pin is set to “High.”

Table 36 CRC Error Detection Mode Setting

Command	Description
MDCRC	Enables CRC error detection mode.
CRCSTP	Detection is temporarily halted. Setting CRCSTP sets an output level of the DIN pin to “Low”. CRCSTP is used to clear detection signal.

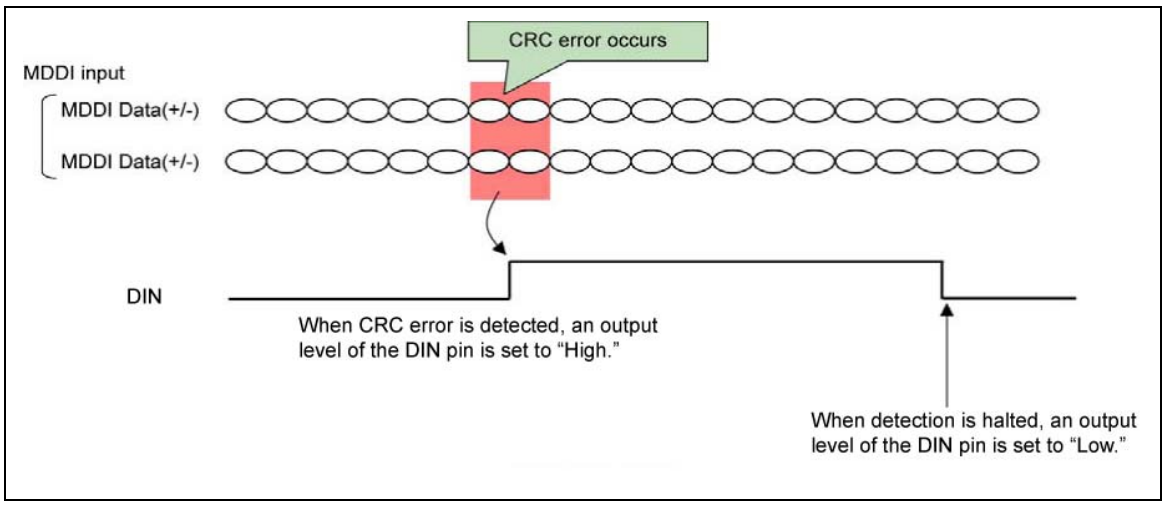


Figure 94

MDDI Moving Picture Interface

The R61529 supports TE interface to display moving picture in MDDI operation. Select either one according to the configuration of the system. By transferring data according to the following sequences, the R61529 can display moving picture via MDDI without tearing.

The Client MDDI supported by the R61529 adopts 2-frame data transfer format when writing moving picture data. By synchronizing the moving picture data rewrite operation via MDDI with the frame mark signal from the R61529 (TE), the R61529 can display moving picture via MDDI without tearing.

The output position of TE signal can be changed in units of lines. The output cycle of TE signal can also be changed in units of frames. Make these settings according to the MDDI transfer speed and data rewrite cycle.

In combination with the Hibernation setting, moving picture can be displayed via MDDI-TE with low power consumption.

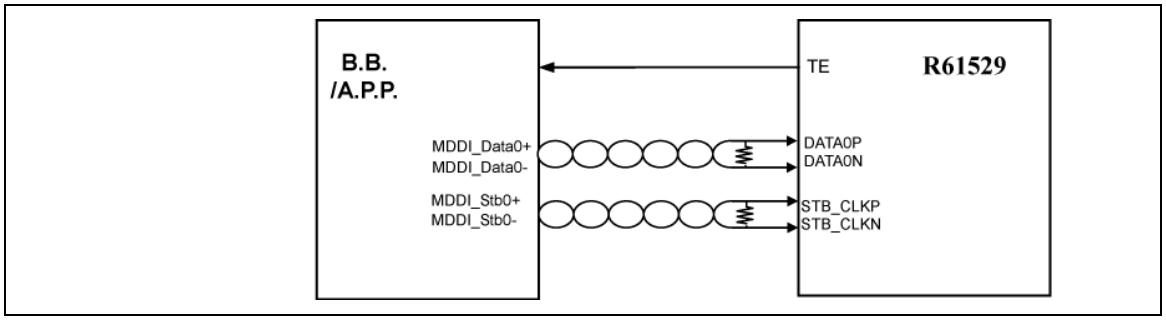


Figure 95

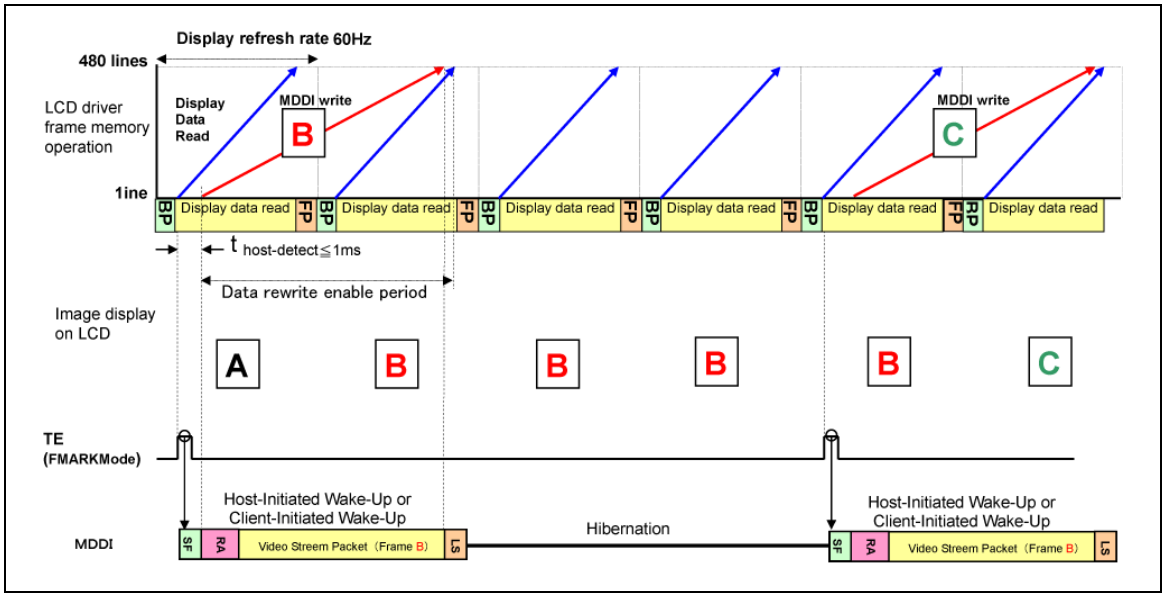


Figure 96

MDDI Mobile Display System

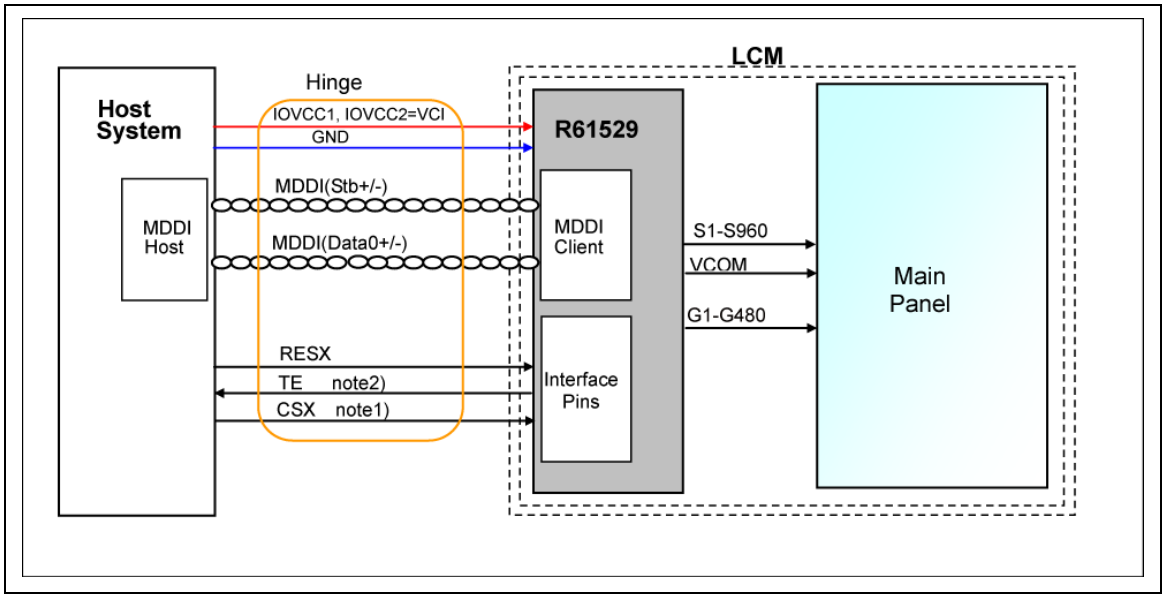


Figure 97 R61529 MDDI Mobile Display System Configuration Example

Notes: 1. The CSX pin is used exclusively for the signal to cancel shutdown mode in MDDI operation. While not using Shutdown mode, the CSX pin does not have to be connected to the Host System.

2. Use TE signal as the reference signal for moving picture display according to the configuration of system.

3. The R61529 does not support the logic output ports to control peripheral devices and sub-display interface.

Method for Switching between MDDI and System Interface

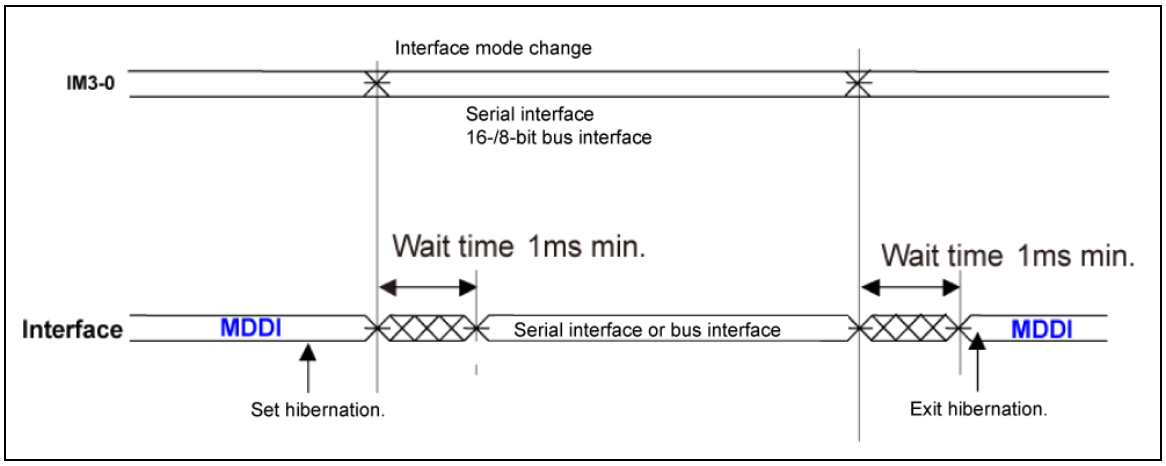


Figure 98

Display Pixel Interface (DPI)

DPI

In Display Pixel Interface (DPI) operation, display operation is in synchronization with synchronous signals VSYNC, HSYNC, and PCLK. Video data is directly output as display data without being written to frame memory. In DPI operation, back porch period (BP) and display period (NL) must be made. Command must be transferred via DBI Type C serial interface. DPI and DSI/MDDI cannot be selected simultaneously.

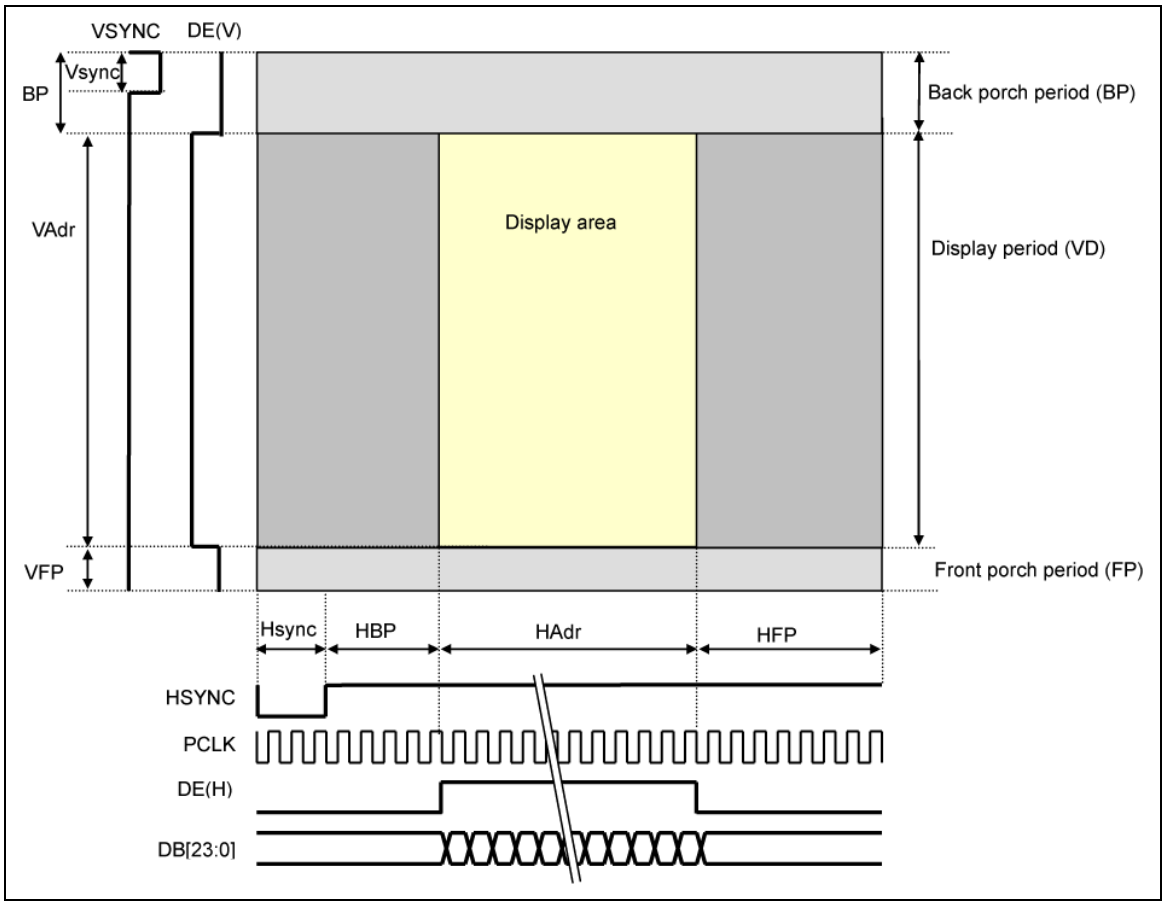


Figure 99

Table 37 Display Timing Setting Example

Parameters	Symbols	Min.	Typ.	Max.	Step	Unit
Horizontal Synchronization	Hsync	(TBD)	-	(TBD)	1	PCLKCYC
Horizontal Back Porch	HBP	DIV=0: (TBD) DIV=1: (TBD)	-	-	1	PCLKCYC
Horizontal Address	HAdr	320	320	(TBD)	1	PCLKCYC
Horizontal Front Porch	HFP	(TBD)	(TBD)	-	1	PCLKCYC
Vertical Synchronization	Vsync	(TBD)	(TBD)	(TBD)	1	Line
Vertical Back Porch	BP	(TBD)	(TBD)	(TBD)	1	Line
Vertical Address	VAdr	480	480	480	1	Line
Vertical Front Porch	VFP	(TBD)	-	(TBD)	1	Line

Note: Typical values are setting example when used with panel resolution QVGA (320RGB x 480), clock frequency (TBD) MHz and frame frequency about 60Hz.

16-Bit DPI

16-bit DPI can be used when set_pixel_format (3Ah) D[6:4]=2'h5. Images are displayed in synchronization with synchronous signals VSYNC, HSYNC, and PCLK. 16-bit RGB data (DB[20:16], DB[13:8], and DB[4:0]) are transferred in synchronization with data enable signal (DE) and display operation. Only system interface (DBI Type C or I2C) can be used to set commands.

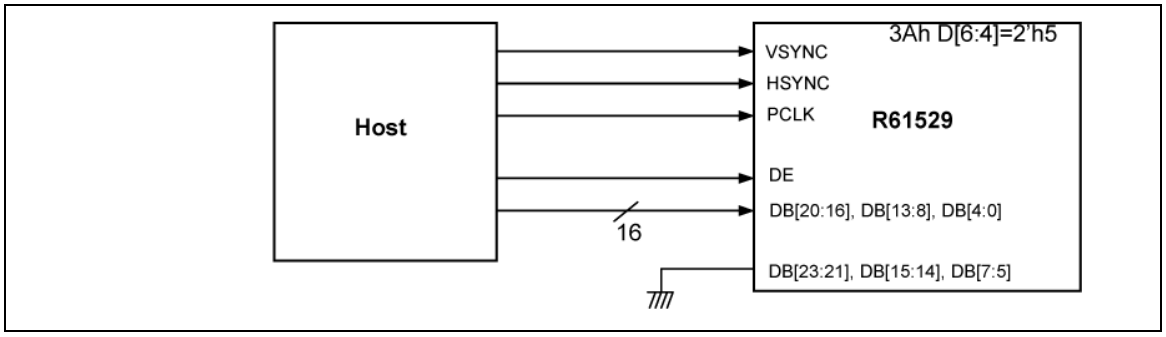


Figure 100

18-Bit DPI

18-bit DPI can be used when set_pixel_format (3Ah) D[6:4]=2'h6. Images are displayed in synchronization with synchronous signals VSYNC, HSYNC, and PCLK. 18-bit RGB data (DB[21:16], DB[13:8], and DB[5:0]) are transferred in synchronization with data enable signal (DE) and display operation. Only system interface (DBI Type C or I2C) can be used to set commands.

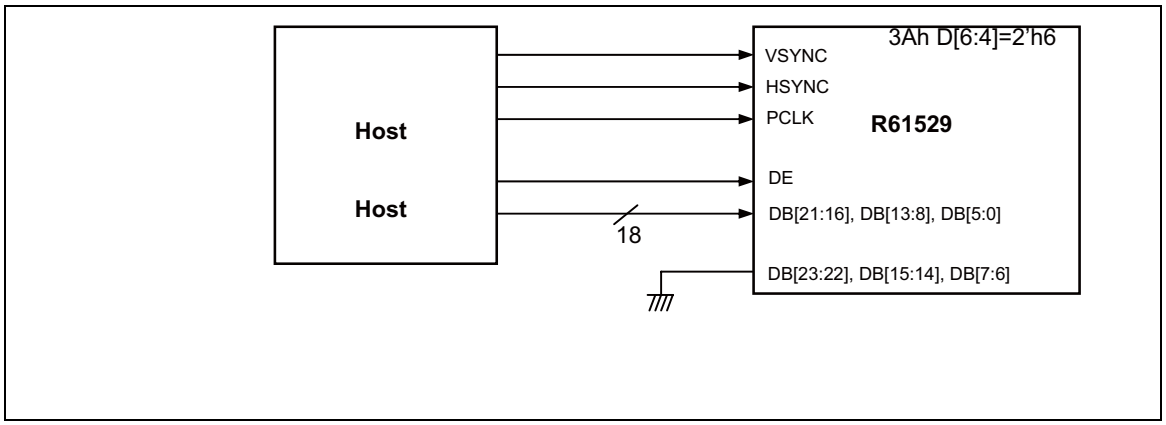


Figure 101

24-Bit DPI

24-bit DPI can be used when set_pixel_format (3Ah) D[6:4]=2'h7. Images are displayed in synchronization with synchronous signals VSYNC, HSYNC, and PCLK. 24-bit RGB data (DB[23:0]) are transferred in synchronization with data enable signal (DE) and display operation. Only system interface (DBI Type C or I2C) can be used to set commands.

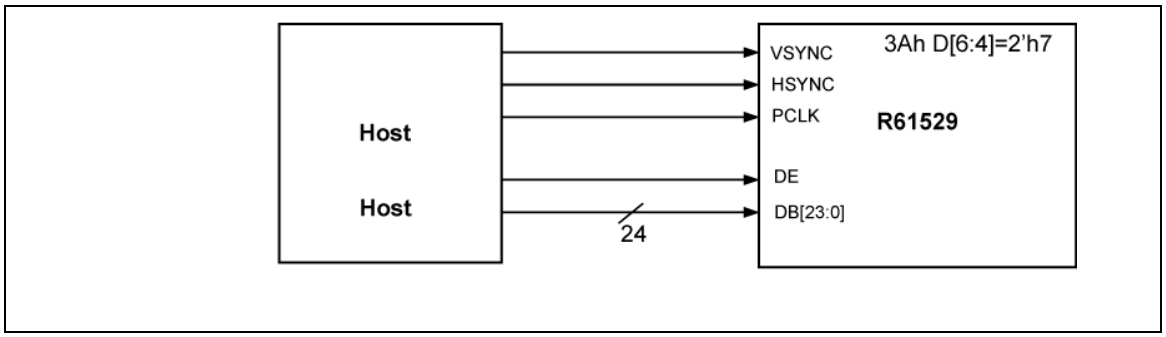


Figure 102

DPI Data Format

The R61529 supports color formats shown below.

Table 38

DPI color format	MIPI Spec.	R61529	3Ah (set_pixel_format) D[6:4]
24bpp (16,777,216-color)	Yes	Yes	3'h7
18bpp (262,144-color Configuration 1)	Yes	No	-
18bpp (262,144-color Configuration 2)	Yes	Yes	3'h6
16bpp (65,536-color Configuration 1)	Yes	No	-
16bpp (65,536-color Configuration 2)	Yes	Yes	3'h5
16bpp (65,536-color Configuration 3)	Yes	No	-

Yes: Supported

No: Unsupported

(a) 24-Bit Interface

When 24bpp format is selected by set_pixel_format (3Ah), connection between host pins and the R61529's pins is shown below.

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
R61529 pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Figure 103

(b) 18-Bit Interface

When 18bpp format is selected by set_pixel_format (3Ah), connection between host pins and the R61529's pins is shown below.

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0
			↓	↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓
R61529 pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Not used		R5	R4	R3	R2	R1	R0	Not used		G5	G4	G3	G2	G1	G0	Not used		B5	B4	B3	B2	B1	B0

Figure 104

(c) 16-Bit Interface

When 16bpp format is selected by set_pixel_format (3Ah), connection between host pins and the R61529's pins is shown below.

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0				B4	B3	B2	B1	B0
				↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓
R61529 pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Not used			R4	R3	R2	R1	R0	Not used		G5	G4	G3	G2	G1	G0	Not used			B4	B3	B2	B1	B0

Figure 105

Extended Format for 24 Bits/Pixel Data in 16-/18-Bit Interface Operation

The R61529 supports a format extended from 16bpp or 18bpp to 24bpp as shown below. A method for extending a format is set by EPF.

	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
24bpp	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
18bpp EPF=2'h0 (Note 1)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	0	0
18bpp EPF=2'h1 (Note 2)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1	1
18bpp EPF=2'h2	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	R[5]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	B[5]	B[4]
16bpp EPF=2'h0 (Note 3)	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[4]	B[3]	B[2]	B[1]	B[0]	0	0	0
16bpp EPF=2'h1 (Note 4)	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[4]	B[3]	B[2]	B[1]	B[0]	1	1	1
16bpp EPF=2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	R[3]	R[2]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]	B[3]	B[2]

Figure 106

Notes:
1. Special processing: R[5:0], G[5:0], B[5:0] = 6'h3F → 8'hFF
2. Special processing: R[5:0], G[5:0], B[5:0] = 6'h00 → 8'h00
3. Special processing: R[4:0], B[4:0] = 5'h1F → 8'hFF
   G[5:0] = 6'h3F → 8'hFF
4. Special processing: R[4:0], B[4:0] = 5'h00 → 8'h00
   G[5:0] = 6'h00 → 8'h00
5. Setting EPF to 2'h3 is prohibited.

VSYNC Interface

The R61529 supports VSYNC interface, which enables displaying a moving picture without tearing by synchronizing MIPI DBI Type B interface (8/16/18/24 bits) with frame synchronous signal (VSYNC).

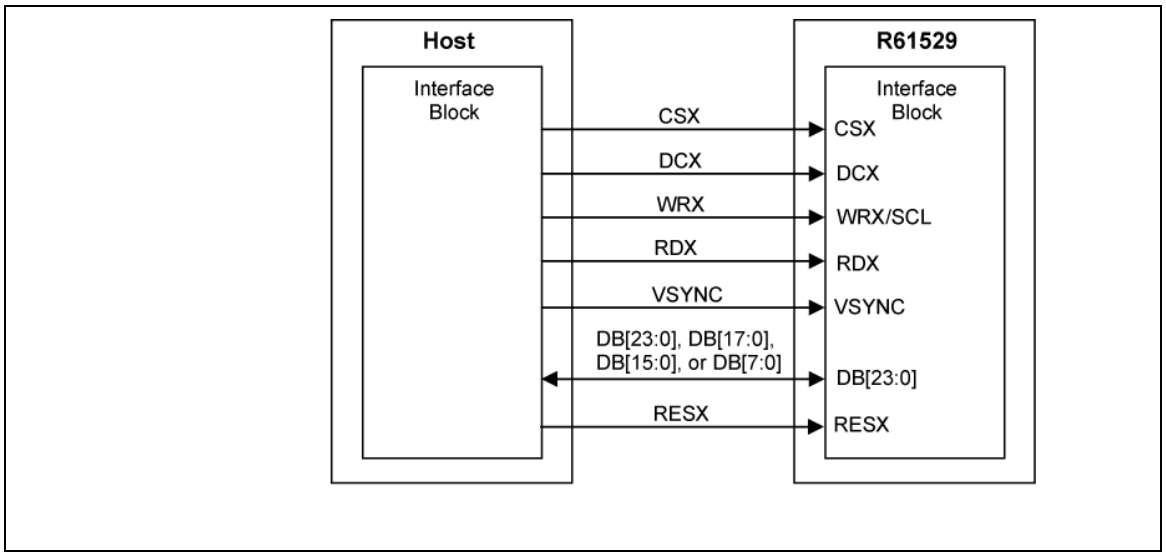


Figure 107

The VSYNC interface is selected by setting DM[1:0] = 10. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed, it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via MIPI DBI Type B interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the R61529 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display.

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

OSC clock frequency (fosc) [Hz]
= Frame frequency × (Display lines (NL) + Front porch (FP) + Back porch (BP)) × 26 clocks × variance

Minimum speed for RAM writing [Hz]
> 320 × (display lines (NL) / {((Back porch (BP) + Display lines (NL) – margin) × 26 clocks) × 1/OSC clock frequency}

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]: Base video image display via VSYNC interface

Panel size	320 RGB × 480 lines (NL = 6'h3B: 480 lines)
Total number of lines (NL)	480 lines
Back/front porch	12/4 lines (BP = 4'hC, FP = 4'h4)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz]
= 60Hz × (480 + 12 + 4) lines × 26 clocks × 1.1 / 0.9 = 945.7kHz

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one VSYNC cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz]
> 320 × 480 / {((12 + 480 - 2) lines × 26 clocks) × 1/945.7MHz} = 11.4MHz

Notes: 1. In this example, it is assumed that the R61529 starts writing data in the internal RAM on the falling edge of VSYNC.
2. There must be at least a margin of 2 lines between the line to which the R61529 has just written data and the line where display operation on the LCD is performed.

In this example, the RAM write operation at a speed of 11.4MHz or more, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the R61529 starts the display operation of the data written in that line and can write video image data without causing flicker on the display.

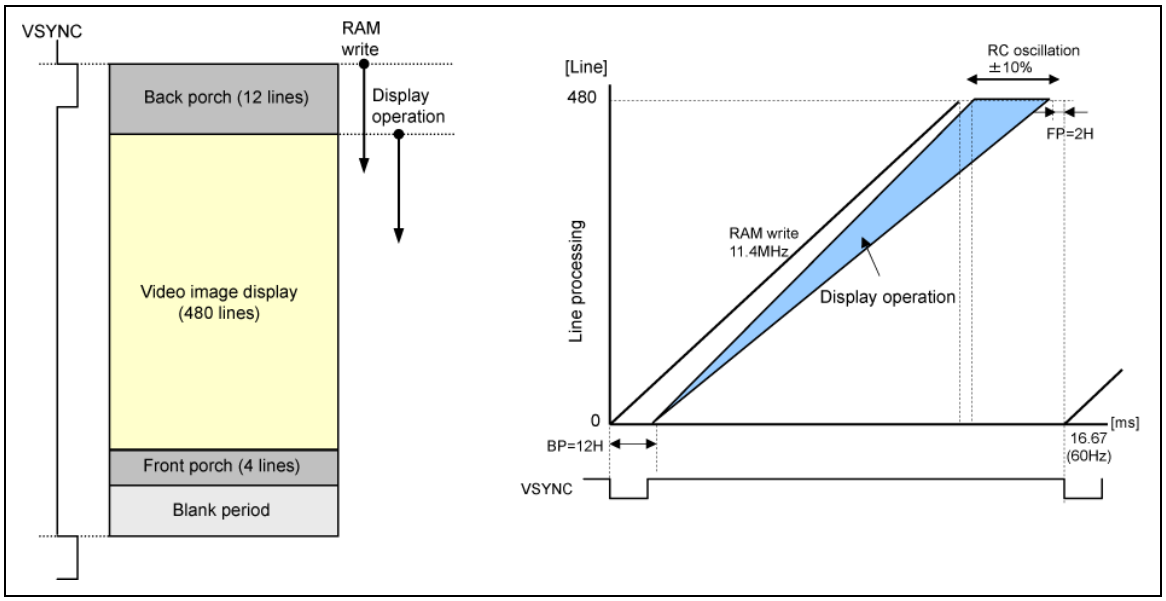


Figure 108 Write Operation via VSYNC Interface

Command List

Table 39 User Command

Operational Code (Hex)	Command	Command (C) /Read (R) /Write(W)	Number Of Parameter	MIPI DCS Type 1 Requirement	R61529 Implementation	Note
00h	nop	C	0	Yes	Yes	
01h	soft_reset	C	0	Yes	Yes	
04h	read_DDB_start	R	5	No	Yes	
06h	get_red_channel	R	1	No	No	
07h	get_green_channel	R	1	No	No	
08h	get_blue_channel	R	1	No	No	
0Ah	get_power_mode	R	1	Yes	Yes (Bits 6/5/4/3/2 Only)	
0Bh	get_address_mode	R	1	Yes	Yes (Bits 7/6/5/3/0 Only)	
0Ch	get_pixel_format	R	1	Yes	Yes	
0Dh	get_display_mode	R	1	Yes	Yes (Bits 5/2/1 Only)	
0Eh	get_signal_mode	R	1	Yes	Yes	
0Fh	get_diagnostic _result	R	1	Bits 7/6: Yes Bits 5/4: Optional	Yes (Bit6 Only)	
10h	enter_sleep_mode	C	0	Yes	Yes	
11h	exit_sleep_mode	C	0	Yes	Yes	
12h	enter_partial_mode	C	0	Yes	Yes	
13h	enter_normal_mode	C	0	Yes	Yes	
20h	exit_invert_mode	C	0	Yes	Yes	
21h	enter_invert_mode	C	0	Yes	Yes	
26h	set_gamma_curve	W	1	Yes	No	
28h	set_display_off	C	0	Yes	Yes	
29h	set_display_on	C	0	Yes	Yes	
2Ah	set_column_address	W	4	Yes	Yes	
2Bh	set_page_address	W	4	Yes	Yes	
2Ch	write_memory_start	W	Variable	Yes	Yes	
2Dh	wite_LUT	W	Variable	Optional	No	
2Eh	read_memory_start	R	Variable	Yes	Yes	

Table 40 User Command (Continued)

Operational Code (Hex)	Command	Command (C) /Read (R) /Write(W)	Number Of Parameter	MIPI DCS Type 1 Requirement	R61529 Implementation	Note
30h	set_partial_area	W	4	Yes	Yes	
33h	set_scroll_area	W	6	Yes	No	
34h	set_tear_off	C	0	Yes	Yes	
35h	set_tear_on	W	1	Yes	Yes	
36h	set_address_mode	W	1	Yes (Bits 7-0)	Yes (Bits 7/6/5/3/0 Only)	
37h	set_scroll_start	W	2	Yes	No	
38h	exit_idle_mode	C	0	Yes	Yes	
39h	enter_idle_mode	C	0	Yes	Yes	
3Ah	set_pixel_format	W	1	Yes	Yes	
3Ch	write_memory _continue	W	Variable	Yes	Yes	
3Eh	read_memory _continue	R	Variable	Yes	Yes	
44h	set_tear_scanline	W	2	Yes	Yes	
45h	get_scanline	R	2	Yes	Yes	
A1h	read_DDB_start	R	5	Yes	Yes (5^{th} parameters)	
A8h	read_DDB_continue	R	Variable	Yes	Yes (5^{th} parameters)	

Table 41 Manufacturer Command (TBD)

Operational Code (Hex)	Function	Command(C) /Read(R) /Write(W)	Number Of Parameter	Category
B0h	Manufacturer Command Access Protect	W/R	1	Additional User Command
B1h	Low Power Mode Control	W/R	1	Additional User Command
B3h	Frame Memory Access and Interface setting	W/R	2	Additional User Command
B5h	Read Checksum and ECC Error Count	R	3	
B6h	DSI Control	W/R	2	
B7h	MDDI Control	W/R	4	
B8h	Backlight Control (1)	W/R	16	
B9h	Backlight Control (2)	W/R	4	
BAh	Backlight Control (3)	R	1	
BFh	Device code Read	R	5	
C0h	Panel Driving Setting	W/R	7	
C1h	Display V-Timing Setting for Normal Mode	W/R	6	
C2h	Display V-Timing Setting for No Partial Mode	W/R	4	
C3h	Display V-Timing Setting for Idle Mode	W/R	4	
C4h	Source / Gate Driving Timing Control	W/R	5	
C6h	DPI polarity Control	W/R	1	
C7h	Display Control Setting	W/R	2	
C8h	Gamma Setting A set	W/R	24	
C9h	Gamma Setting B set	W/R	24	
CAh	Gamma Setting C set	W/R	24	
D0h	Power Setting	W/R	12	
D3h	Power Setting for Normal Mode	W/R	1	
D5h	VCOM Setting	W/R	4	
E0h	NV Memory Access Control	W/R	4	
E1h	set_write_DDB_control	W/R	1	
E2h	NV Memory Load Control	W/R	1	
F5h	Read Mode In for DBI only	C	0	
F6h	Read Mode Out for DBI only	C	0	

Command Accessibility

In the default status, only User Commands and Manufacturer Command Access Protect (B0h) can be accessed. Other commands are recognized as “nop”.

Manufacturer Commands except B0h command are accessible by releasing Access Protect. See Command B0h description for details.

Table 42 User Command

Operational Code(Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
00h	nop	Yes	Yes	Yes	Yes	Yes
01h	soft_reset	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
04h	read_DDB_start	Yes	Yes	Yes	Yes	Yes
0Ah	get_power_mode	Yes	Yes	Yes	Yes	Yes
0Bh	get_address_mode	Yes	Yes	Yes	Yes	Yes
0Ch	get_pixel_format	Yes	Yes	Yes	Yes	Yes
0Dh	get_display_mode	Yes	Yes	Yes	Yes	Yes
0Eh	get_signal_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
0Fh	get_diagnostic _result	Yes	Yes	Yes	Yes	Yes
10h	enter_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
11h	exit_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
12h	enter_partial_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
13h	enter_normal_mode	Yes	Yes	Yes	Yes	Yes
20h	exit_invert_mode	Yes	Yes	Yes	Yes	Yes
21h	enter_invert_mode	Yes	Yes	Yes	Yes	Yes
28h	set_display_off	Yes	Yes	Yes	Yes	Yes
29h	set_display_on	Yes	Yes	Yes	Yes	Yes
2Ah	set_column_address	Yes	Yes	Yes	Yes	Yes
2Bh	set_page_address	Yes	Yes	Yes	Yes	Yes
2Ch	write_memory_start	Yes	Yes	Yes	Yes	Yes
2Eh	read_memory_start	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
30h	set_partial_area	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
34h	set_tear_off	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
35h	set_tear_on	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
36h	set_address_mode	Yes	Yes	Yes	Yes	Yes
38h	exit_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
39h	enter_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Ah	set_pixel_format	Yes	Yes	Yes	Yes	Yes
3Ch	write_memory_continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Eh	read_memory_continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
44h	set_tear_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
45h	get_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	No
A1h	read_DDB_start	Yes	Yes	Yes	Yes	Yes

Table 43 User Command (continued)

Operational Code (Hex) Command		Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
A8h	read_DDB_continue	Yes	Yes	Yes	Yes	Yes

Notes: 1. Command may be accessed only when DM = 0 (display operation is in synchronization with internal oscillation clock). To access these commands is disabled when DM = 1 and DPI is selected.

2. Read Mode In command (EFh) can be used only in DBI Type C operation.

Table 44 Manufacturer Command (TBD)

Operational Code(Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
B0h	Manufacturer Command Access Protect	Yes	Yes	Yes	Yes	Yes
B1h	Low Power Mode Control	No	No	No	No	Yes
B3h	Frame Memory Access and Interface setting	Yes	Yes	Yes	Yes	Yes
B5h	Read Checksum and ECC Error Count	Yes	Yes	Yes	Yes	Yes
B6h	DSI Control	Yes	Yes	Yes	Yes	Yes
B7h	MDDI Control	Yes	Yes	Yes	Yes	Yes
B8h	Backlight Control (1)	Yes	Yes	Yes	Yes	Yes
B9h	Backlight Control (2)	Yes	Yes	Yes	Yes	Yes
BAh	Backlight Control (3)	Yes	Yes	Yes	Yes	No
BFh	Device code Read	Yes	Yes	Yes	Yes	Yes
C0h	Panel Driving Setting	Yes	Yes	Yes	Yes	Yes
C1h	Display V-Timing Setting for Normal Mode	Yes	Yes	Yes	Yes	Yes
C2h	Display V-Timing Setting for No Partial Mode	Yes	Yes	Yes	Yes	Yes
C3h	Display V-Timing Setting for Idle Mode	Yes	Yes	Yes	Yes	Yes
C4h	Source / Gate Driving Timing Control	Yes	Yes	Yes	Yes	Yes
C6h	DPI polarity Control	Yes	Yes	Yes	Yes	Yes
C7h	Display Control Setting	Yes	Yes	Yes	Yes	Yes
C8h	Gamma Setting A set	Yes	Yes	Yes	Yes	Yes
C9h	Gamma Setting B set	Yes	Yes	Yes	Yes	Yes
CAh	Gamma Setting C set	Yes	Yes	Yes	Yes	Yes
D0h	Power Setting	Yes	Yes	Yes	Yes	Yes
D3h	Power Setting for Normal Mode	Yes	Yes	Yes	Yes	Yes
D5h	VCOM Setting	Yes	Yes	Yes	Yes	Yes
E0h	NV Memory Access Control	Yes	Yes	Yes	Yes	No
E1h	set_write_DDB_control	Yes	Yes	Yes	Yes	Yes
E2h	NV Memory Load Control	Yes	Yes	Yes	Yes	Yes

Table 45 Manufacturer Command (TBD) (continued)

Operational Code (Hex) Command		Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
F5h	Read Mode In for DBI only	Yes	Yes	Yes	Yes	Yes
F6h	Read Mode Out for DBI only	Yes	Yes	Yes	Yes	Yes

Default Modes and Values

Table 46 User Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values(Hex)		
			After Power-on	After SW Reset	After HW Reset
00h	Nop	None	N/A	N/A	N/A
01h	soft_reset	None	N/A	N/A	N/A
04h	Read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		5th	FFh	FFh	FFh
0Ah	get_power_mode	1st	08h	08h	08h
0Bh	get_address_mode	1st	00h	No Change (Note1)	00h
0Ch	get_pixel_format	1st	77h	77h	77h
0Dh	get_display_mode	1st	00h	00h	00h
0Eh	get_signal_mode	1st	00h	00h	00h
0Fh	get_diagnostic_result	1st	00h	00h	00h
10h	enter_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
11h	exit_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
12h	enter_partial_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
13h	enter_normal_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
20h	exit_invert_mode	None	Invert Mode Off	Invert Mode Off	Invert Mode Off
21h	enter_invert_mode	None	Invert Mode Off	Invert Mode Off	Invert Mode Off
28h	set_display_off	None	Display Off	Display Off	Display Off
29h	set_display_on	None	Display Off	Display Off	Display Off
2Ah	set_column_address	1st/2nd SC[9:0]	000h	000h	000h
		3rd/4th EC[9:0]	13F	If set_address_mode B5=0: 13F B5=1: 1DF	13F

Table 47 User Command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values(Hex)		
			After Power-on	After SW Reset	After HW Reset
2Bh	set_page_address	1st/2nd SP[9:0]	000h	000h	000h
		3rd/4th EP[9:0]	1DF	If set_address_mode B5=0 : 1DF B5=1 : 13F	1DF
2Ch	write_memory_start	All	Random Values	Not Cleared	Not Cleared
2Eh	read_memory_start	All	Random Values	Not Cleared	Not Cleared
30h	set_partial_area	1st/2nd SR[9:0]	000h	000h	000h
		3rd/4th ER[9:0]	1DF	1DF	1DF
34h	set_tear_off	6	TE line output Off	TE line output Off	TE line output Off
35h	set_tear_on	1st	TE line output Off	TE line output Off	TE line output Off
36h	set_address_mode	1st	00h	No Change (Note1)	00h
38h	exit_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
39h	enter_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
3Ah	set_pixel_format	1st	77h	77h	77h
3Ch	write_memory_ continue	All	Random Values	Not Cleared	Not Cleared
3Eh	read_memory_ continue	All	Random Values	Not Cleared	Not Cleared
44h	set_tear_scanline	1st/2nd STS[9:0]	000h	000h	000h
45h	get_scanline	1st/2nd GTS[9:0]	000h (invalid)	000h (invalid)	000h (invalid)

Table 48 User Command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values(Hex)		
			After Power-on	After SW Reset	After HW Reset
A1h	Read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		5th	FFh	FFh	FFh
A8h	read_DDB_continue	Variable	See read_DDB_start.	See read_DDB_start.	See read_DDB_start.

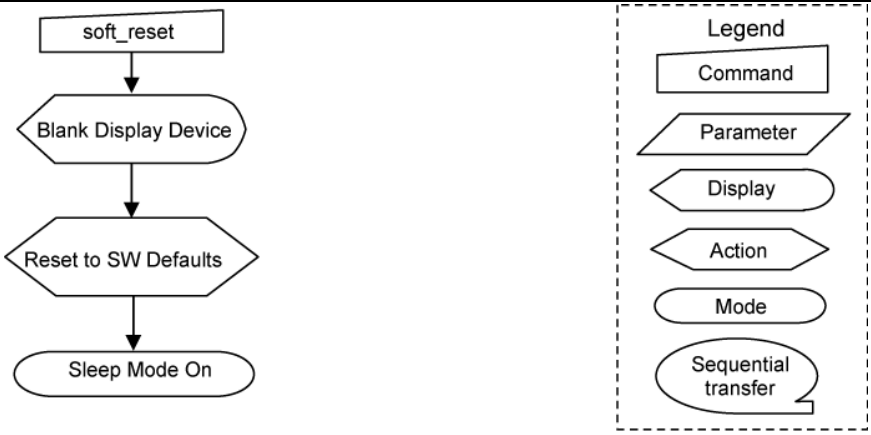
Notes: 1. No change from the value before soft_reset command.
2. Data are loaded from internal NVM. If user writes VCM register value, Supplier ID, and Supplier Elective Data to the NVM, the values are set to default.

User Command

nop: 00h

00h	nop											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	0	0	0	0	0	00h
Parameter	None											
Description	This command is an empty command. It has no effect on the display module. X = Don't care											
Restriction	-											
Flow Chart	-											

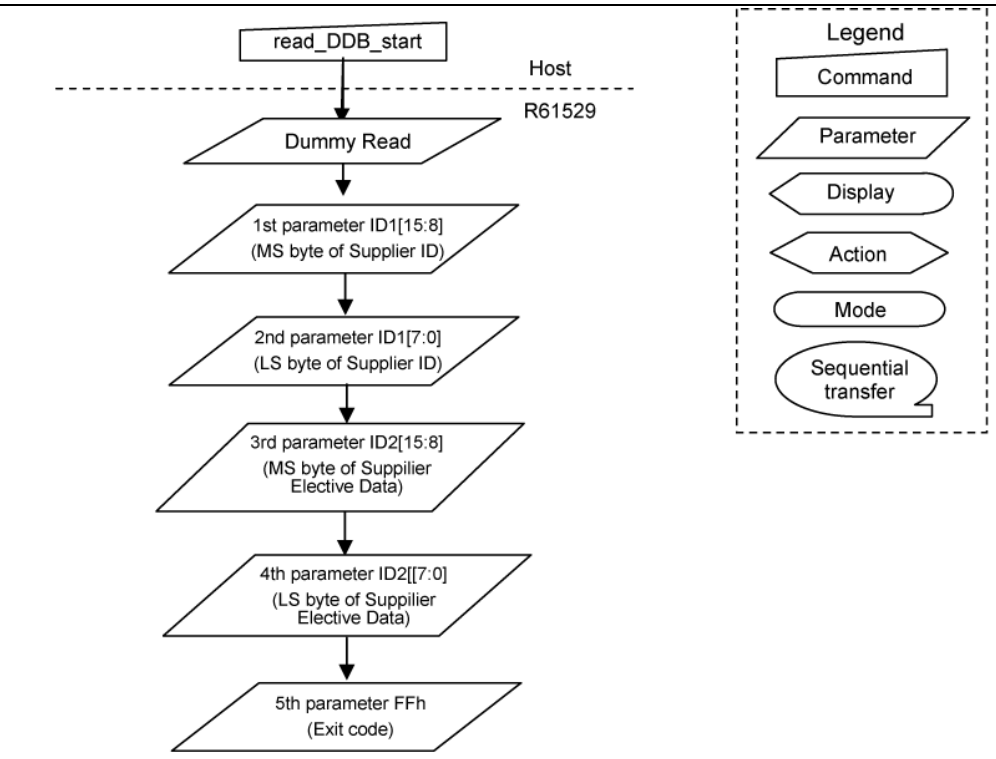
soft_reset: 01h

01h	soft_reset											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	0	0	0	0	1	01h
Parameter	None											
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values (See “Default Modes and Values”) X = Don’t care											
Restriction	If a soft_reset is sent when the display module is not in Sleep Mode, the host processor must wait 5 frames before sending an exit_sleep_mode command. soft_reset shall not be sent during exit_sleep_mode sequence. No new command setting is allowed until the R61529 enters the Sleep Mode. See “State & Command sequence” for the sequence to enter Sleep Mode.											
Flow Chart												

read_DDB_start: 04h

04h	read_DDB_start											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	0	0	1	0	0	04h
Dummy parameter	D→H	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
1st parameter	D→H	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
2nd parameter	D→H	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
3rd parameter	D→H	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
4th parameter	D→H	1	X	1	1	1	1	1	1	1	1	FFh
Parameter	None											
Description	The command returns information from the display module as follows: 1st parameter: upper byte (ID1[15:8]) of Supplier ID 2nd parameter: lower byte (ID[7:0]) of Supplier ID 3rd parameter: Supplier Elective Data (ID2[15:8]) 4th parameter: Supplier Elective Data (ID2[7:0]) 5th parameter: Exit Code (FFh) Supplier ID and Supplier Elective Data stored in internal NVM are read. X=Don't care											
Restriction	-											

Flow Chart



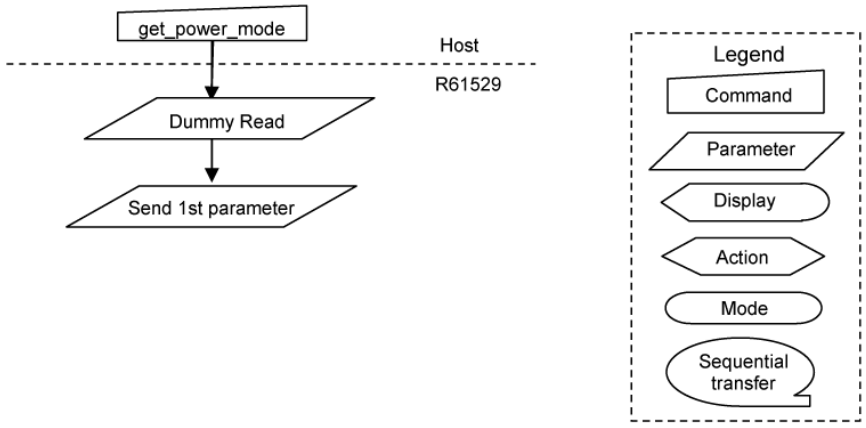
Note : When reading by DSI, there is no dummy read.

get_power_mode: 0Ah

<table>
<tr><th>0Ah</th><th colspan="12">get_power_mode</th></tr>
<tr><td></td><td>Direction</td><td>DCX</td><td>DB23-DB8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>H→D</td><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0Ah</td></tr>
<tr><td>Dummy parameter</td><td>D→H</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XXh</td></tr>
<tr><td>1st parameter</td><td>D→H</td><td>1</td><td>X</td><td>0</td><td>IDMON</td><td>PLTON</td><td>SLPOUT</td><td>1</td><td>DSPON</td><td>0</td><td>0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="12">The display module returns the current power mode as listed below.
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Reserved</td><td>Set to ‘0’.</td><td>—</td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td>-</td><td>IDMON</td></tr>
<tr><td>D5</td><td>Partial Mode On/Off</td><td>-</td><td>PLTON</td></tr>
<tr><td>D4</td><td>Sleep Mode On/Off</td><td>-</td><td>SLPOUT</td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td>Set to ‘1’.</td><td>—</td></tr>
<tr><td>D2</td><td>Display On/Off</td><td>-</td><td>DSPON</td></tr>
<tr><td>D1</td><td>Reserved</td><td>Set to ‘0’.</td><td>—</td></tr>
<tr><td>D0</td><td>Reserved</td><td>Set to ‘0’.</td><td>—</td></tr>
</table>

Bit D7 – Reserved
This bit is not applicable. Set to ‘0’. (Not supported)
Bit D6 – Idle Mode On/Off
‘0’ = Idle Mode Off
‘1’ = Idle Mode On
Bit D5 – Partial Mode On/Off
‘0’ = Partial Mode Off
‘1’ = Partial Mode On
Bit D4 – Sleep Mode On/Off
‘0’ = Sleep Mode On
‘1’ = Sleep Mode Off
Bit D3 – Display Normal Mode On/Off
This bit is not applicable. Set to ‘1’. (Not supported)
Bit D2 – Display On/Off
‘0’ = Display is Off.
‘1’ = Display is On.
Bit D1 – Reserved
This bit is not applicable. Set to ‘0’. (Not supported)
Bit D0 – Reserved
This bit is not applicable. Set to ‘0’. (Not supported)

X = Don’t care</td></tr>
</table>

Restriction	-
Flow Chart	 Note : When reading by DSI, there is no dummy read.

get_address_mode: 0Bh

0Bh	get_address_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	0	1	0	1	1	0Bh
Dummy parameter	D→H	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	D→H	1	X	B7	B6	B5	0	B3	0	0	B0	XXh

Description

The display module returns the current status of the display as described in the table below. This command setting depends on set_address_mode (36h).

Bit	Description	Comment	Command list symbol
D7	Page Address Order	-	B7
D6	Column Address Order	-	B6
D5	Page/Column Order	-	B5
D4	Line Address Order	Set to ‘0’.	-
D3	RGB/BGR Order	-	B3
D2	Display Data Latch Order	Set to ‘0’.	-
D1	Flip Horizontal	Set to ‘0’.	-
D0	Flip Vertical	-	B0

- Bit D7 – Page Address Order

‘0’ = Top to Bottom (When set_address_mode D7 = ‘0’)
‘1’ = Bottom to Top (When set_address_mode D7 = ‘1’)

- Bit D6 – Column Address Order

‘0’ = Left to Right (When set_address_mode D6 = ’0’)
‘1’ = Right to Left (When set_address_mode D6 = ‘1’)

- Bit D5 – Page/Column Order

‘0’ = Normal Mode
‘1’ = Reverse Mode

- Bit D4 – Line Address Order

This bit is not applicable. Set to ‘0’. (Not supported)

- Bit D3 – RGB/BGR Order

‘0’ = RGB (When set_address_mode D3 = ‘0’)
‘1’ = BGR (When set_address_mode D3 = ‘1’)

- Bit D2 – Display Data Latch Order

This bit is not applicable. Set to ’0’. (Not supported)

- Bit D1 – Flip Horizontal

This bit is not applicable. Set to ‘0’. (Not supported)

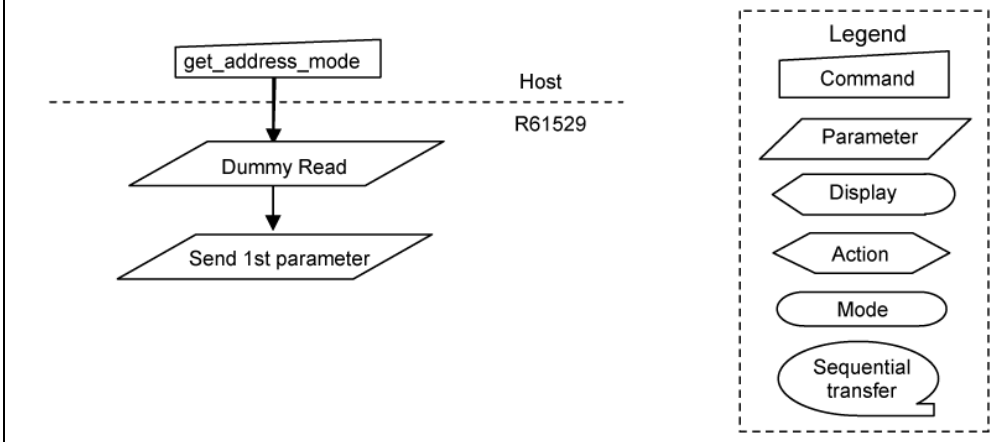
- Bit D0 – Flip Vertical

‘0’ = Normal (When set_address_mode D0 = ‘0’)
‘1’ = Flipped (When set_address_mode D0 = ‘1’)

X = Don’t care

Restriction

-

Flow Chart	 Note : When reading by DSI, there is no dummy read.

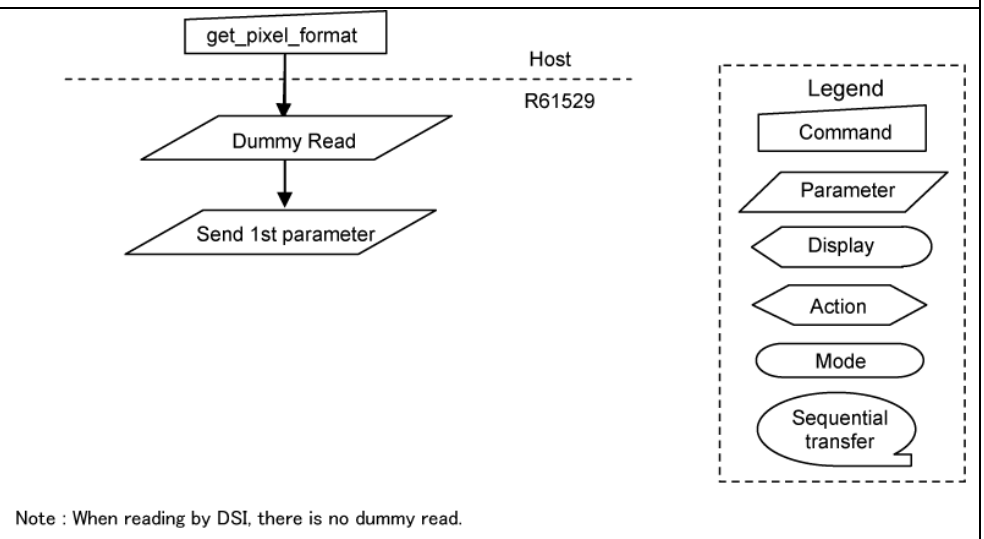
Note: See “”State Transition Diagram” for display mode transition.

get_pixel_format: 0Ch

<table>
<tr><th>0Ch</th><th colspan="12">get_pixel_format</th></tr>
<tr><td></td><td>Direction</td><td>DCX</td><td>DB23-DB8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>H→D</td><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0Ch</td></tr>
<tr><td>Dummy parameter</td><td>D→H</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XXh</td></tr>
<tr><td>1st parameter</td><td>D→H</td><td>1</td><td>X</td><td>0</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>D2</td><td>D1</td><td>D0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below. This command setting depends on set_pixel_format (3Ah).
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td rowspan="4">DPI Pixel Format
(DPI/ DSI-Video/ MDDI-Video)</td><td>Set to ’0’.</td></tr>
<tr><td>D6</td><td>D6</td></tr>
<tr><td>D5</td><td>D5</td></tr>
<tr><td>D4</td><td>D4</td></tr>
<tr><td>D3</td><td rowspan="4">DBI Pixel Format
(DBI/ DSI-Command/ MDDI-Command/ I2C)</td><td>Set to ’0’.</td></tr>
<tr><td>D2</td><td>D2</td></tr>
<tr><td>D1</td><td>D1</td></tr>
<tr><td>D0</td><td>D0</td></tr>
</table>

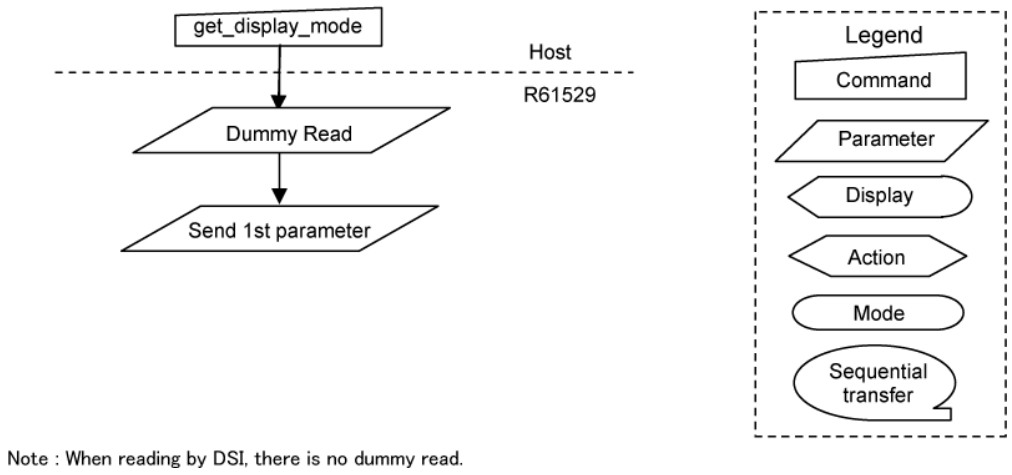
Bit D7
This bit is not applicable. Set to ‘0’. (Not supported)
Bit D[6:4] – DPI Pixel Format (Control Interface Color Format Selection)
See the table below.
Bit D3
This bit is not applicable. Set to ‘0’. (Not supported)
Bit D[2:0] – DBI Pixel Format (Control Interface Color Format Selection)

Note: See “set_pixel_format (3Ah).”
<table>
<tr><th>Control Interface Color Format</th><th>D6/D2</th><th>D5/D1</th><th>D4/D0</th></tr>
<tr><td>Setting inhibited</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Setting inhibited</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Setting inhibited</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Setting inhibited</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Setting inhibited</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 bits/pixel (65,536 colors)</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 bits/pixel (262,144 colors)</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>24 bits/pixel (16,777,216 colors)</td><td>1</td><td>1</td><td>1</td></tr>
</table>
X = Don’t care</td></tr>
</table>

Restriction	
Flow Chart	 Note : When reading by DSI, there is no dummy read.

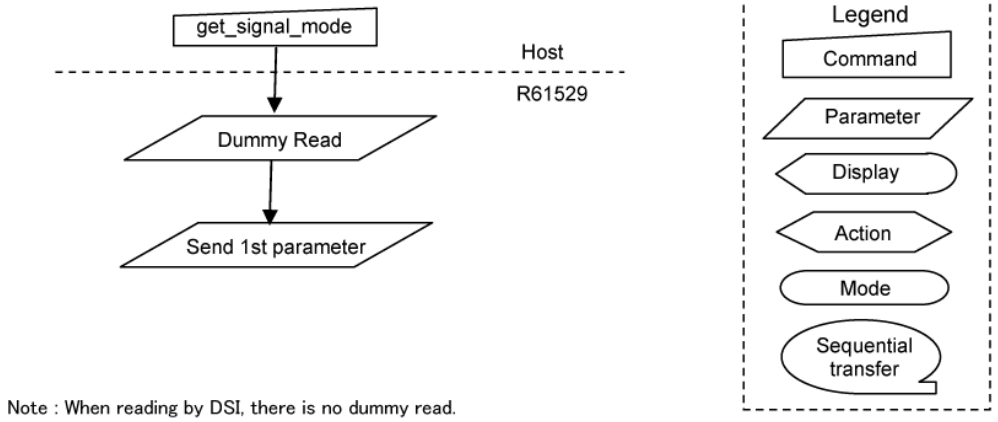
get_display_mode: 0Dh

<table>
<tr><th>0Dh</th><th colspan="12">get_display_mode</th></tr>
<tr><td></td><td>Direction</td><td>DCX</td><td>DB23-DB8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>H→D</td><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>Dummy parameter</td><td>D→H</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XXh</td></tr>
<tr><td>1st parameter</td><td>D→H</td><td>1</td><td>X</td><td>0</td><td>0</td><td>INV ON</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X0h</td></tr>
<tr><td>Description</td><td colspan="12">The display module returns the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Vertical Scrolling Status</td><td>Set to ‘0’.</td><td>—</td></tr>
<tr><td>D6</td><td>Reserved</td><td>Set to ‘0’.</td><td>—</td></tr>
<tr><td>D5</td><td>Inversion On/Off</td><td>-</td><td>INVON</td></tr>
<tr><td>D4</td><td>Reserved</td><td>Set to ‘0’.</td><td>—</td></tr>
<tr><td>D3</td><td>Reserved</td><td>Set to ‘0’.</td><td>—</td></tr>
<tr><td>D2</td><td>Gamma Curve Selection</td><td>Set to ‘0’.</td><td>—</td></tr>
<tr><td>D1</td><td>Gamma Curve Selection</td><td>Set to ‘0’.</td><td>—</td></tr>
<tr><td>D0</td><td>Gamma Curve Selection</td><td>Set to ‘0’.</td><td>—</td></tr>
</table>
• Bit D7 – Page Address Order
This bit is not applicable. Set to ‘0’. (Not supported)
• Bit D6 – Reserved
This bit is not applicable. Set to ‘0’. (Not supported)
• Bit D5 – Inversion On/Off
‘0’ = Inversion is Off.
‘1’ = Inversion is On.
• Bit D[4:3] – Reserved
This bit is not applicable. Set to ‘0’. (Not supported)
• Bit D[2:0] – Gamma Curve Selection
This bit is not applicable. Set to ’0’. (Not supported)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
</table>

Flow Chart	 Note : When reading by DSI, there is no dummy read.

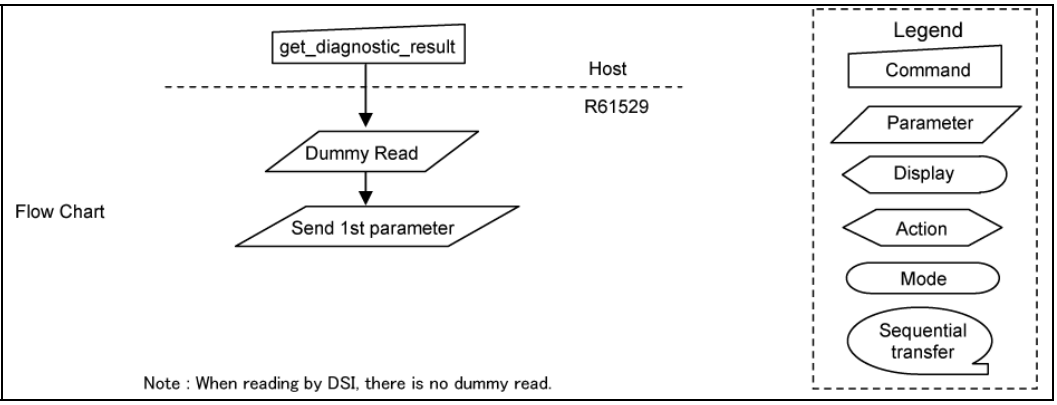
get_signal_mode: 0Eh

<table>
<tr><th>0Eh</th><th colspan="12">get_signal_mode</th></tr>
<tr><td></td><td>Direction</td><td>DCX</td><td>DB23-DB8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>H→D</td><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0Eh</td></tr>
<tr><td>Dummy parameter</td><td>D→H</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XXh</td></tr>
<tr><td>1st parameter</td><td>D→H</td><td>1</td><td>X</td><td>1</td><td>x</td><td>TE ON</td><td>TEL OM</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X0h</td></tr>
<tr><td>Description</td><td colspan="12">The display module returns the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Tearing Effect Line On/Off</td><td></td><td>TEON</td></tr>
<tr><td>D6</td><td>Tearing Effect Line Output Mode</td><td></td><td>TELOM</td></tr>
<tr><td>D5</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D4</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D3</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D2</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D1</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D0</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
</table>
Bit D7 – Tearing Effect Line On/Off
‘0’ = Tearing Effect Line is Off.
‘1’ = Tearing Effect Line is On.
Bit D6 – Tearing Effect Line Output Mode (See set_tear_on: 35h)
‘0’ = Mode 1
‘1’ = Mode 2
Bit D[5:0] – Reserved
This bit is not applicable. Set to ’0’. (Not supported)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
</table>

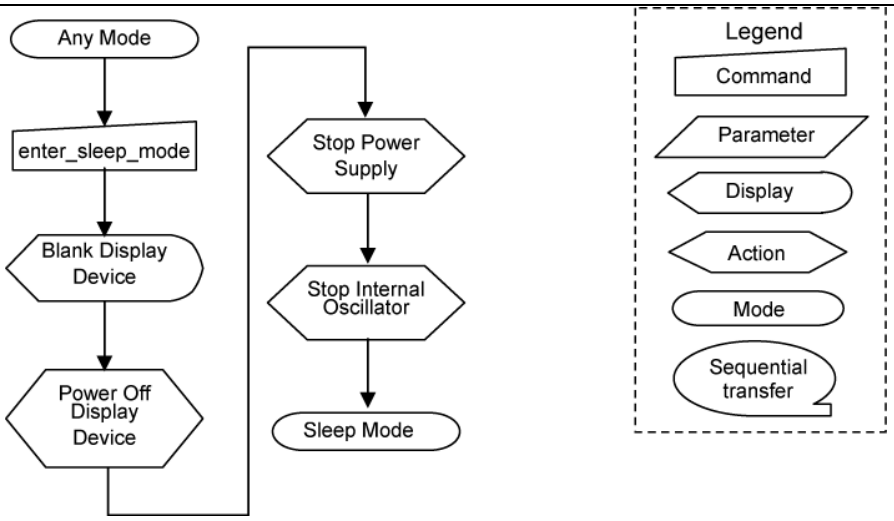
Flow Chart	 Note : When reading by DSI, there is no dummy read.

get_diagnostic_result: 0Fh

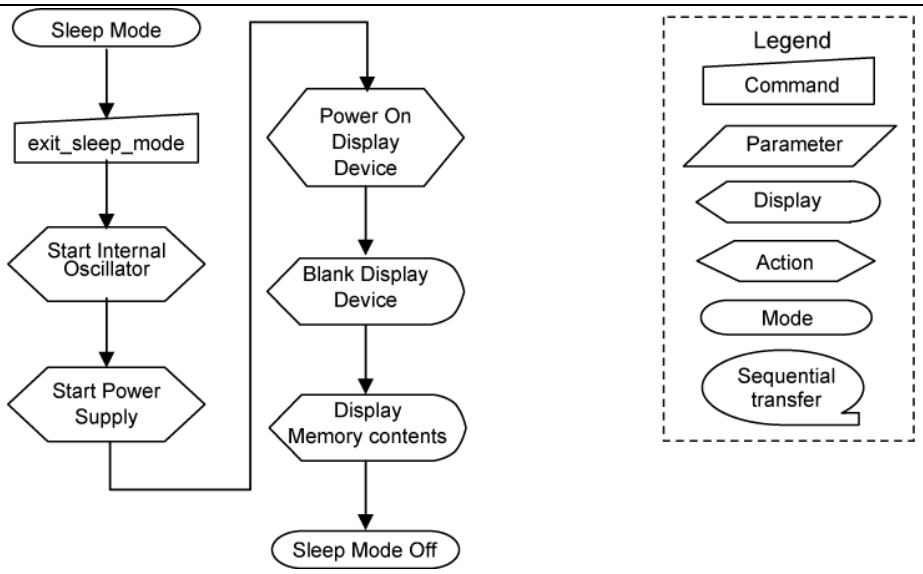
<table>
<tr><th>0Fh</th><th colspan="12">get_diagnostic_result</th></tr>
<tr><td></td><td>Direction</td><td>DCX</td><td>DB23-DB8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>H→D</td><td>0</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0Fh</td></tr>
<tr><td>Dummy parameter</td><td>D→H</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XXh</td></tr>
<tr><td>1st parameter</td><td>D→H</td><td>1</td><td>X</td><td>0</td><td>FUNCD</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X0h</td></tr>
<tr><td>Description</td><td colspan="12">
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Register Loading Detection</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D6</td><td>Functionality Detection</td><td>-</td><td>FUNCD</td></tr>
<tr><td>D5</td><td>Chip Attachment Detection</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D4</td><td>Display Glass Break Detection</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D3</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D2</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D1</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
<tr><td>D0</td><td>Reserved</td><td>Set to ‘0’.</td><td>–</td></tr>
</table>
The display module returns the self-diagnostic results following the exit_sleep_mode (11h) as shown in the table above.
• Bit D7 – Register Loading Detection
This bit is not applicable. Set to “0”.
• Bit D6 – Functionality Detection
• Bit D5 – Chip Attachment Detection
This bit is not applicable. Set to “0”.
• Bit D4 –Display Glass Break Detection
This bit is not applicable. Set to “0”.
• Bit D[3:0] – Reserved
Set to 0.
X = Don’t care
</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
</table>

Flow Chart	

enter_sleep_mode: 10h

10h	enter_sleep_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	1	0	0	0	0	10h
Parameter	None											
Description	This command causes the LCD module to enter the Sleep mode. In this mode, the step-up circuit, internal oscillator and panel scanning stop. See State Transition Diagram for each stage of transition. X = Don't care											
Restriction	This command has no effect when the module is already in Sleep mode. Sleep mode can be exited only when the exit_sleep_mode (11h) is transmitted. Sending a new command is prohibited while the R61529 performs either display off sequence or power off sequence. Using DSI Data Type (22h and 32h) with DCS commands (10h, 11h, 28h, or 29h) is prohibited.											
Flow Chart												

exit_sleep_mode: 11h

11h	exit_sleep_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	1	0	0	0	1	11h
Parameter	None											
Description	This command causes the display module to exit Sleep mode. The step-up circuit, internal oscillator, and panel scanning start. See State Transition Diagram for each stage of transition. X = Don't care											
Restriction	This command shall not cause any visual effect on display device when the display module is not in Sleep mode. No new command setting is allowed during power ON sequence. Operation may continue for more than 6 frame periods due to power ON sequence setting. Do not send any command either in this case. The host processor must wait 5 frame periods after sending an enter_sleep_mode command before sending an exit_sleep_mode command. The display runs the self-diagnostic function after this command is received. Using DSI Data Type (22h and 32h) with DCS commands (10h, 11h, 28h, or 29h) is prohibited.											
Flow Chart												

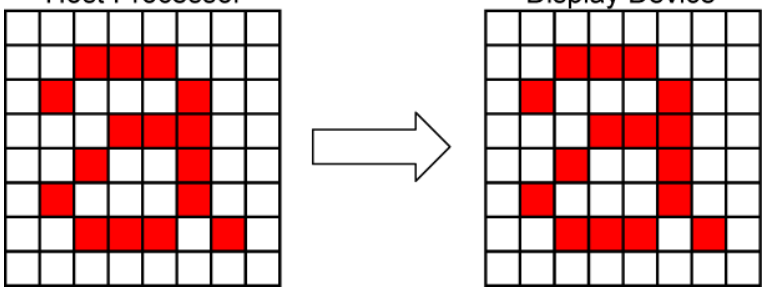
enter_partial_mode: 12h

12h	enter_partial_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	x	0	0	0	1	0	0	1	0	12h
Parameter	None											
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the set_partial_area command (30h). To leave Partial Display Mode, the enter_normal_mode (13h) should be written. X = Don't care Note: When a command breaks in the middle of frame period in Normal mode, the command is enabled from the next frame period.											
Restriction	This command has no effect when the module is already in Partial mode.											
Flow Chart	See "set_partial_area (30h)".											

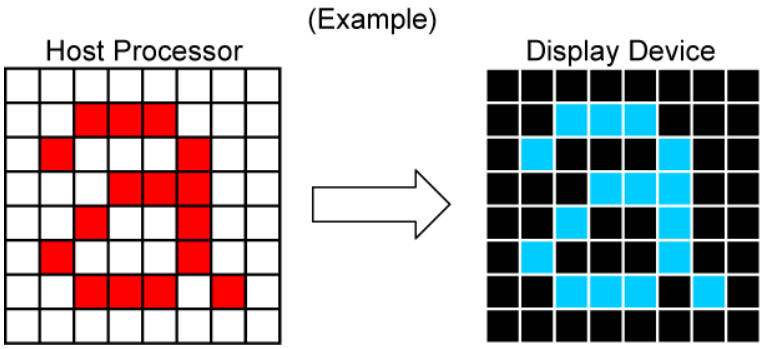
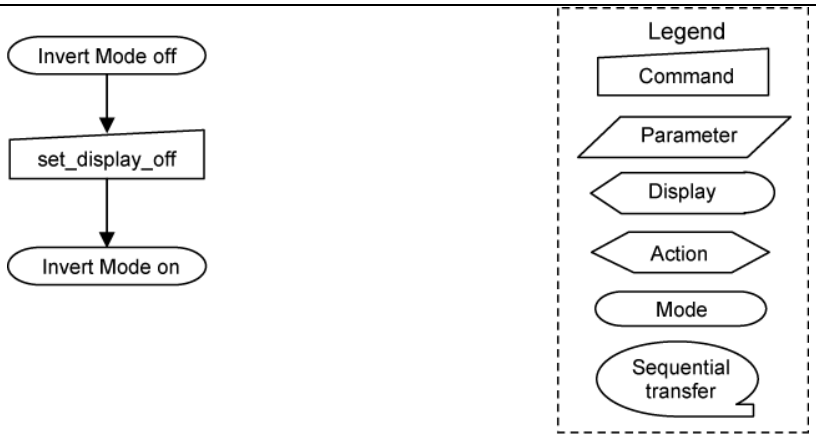
enter_normal_mode: 13h

13h	enter_normal_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	x	0	0	0	1	0	0	1	1	13h
Parameter	None											
Description	This command causes the display module to enter the Normal mode. Normal Mode means Partial mode is off. X = Don't care Note: When a command breaks in the middle of frame period in Partial mode, that command becomes valid from the next frame period.											
Restriction	This command has no effect when Normal mode is already active.											
Flow Chart	See the description of command set_partial_area (30h) when using this command.											

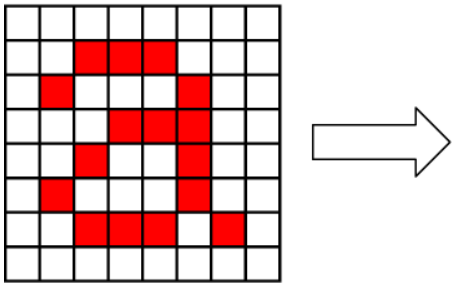
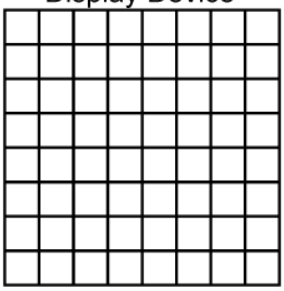
exit_invert_mode: 20h

20h	exit_invert_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	0	0	0	0	20h
Parameter	None											
Description	This command causes the display module to stop inverting the image data on the display device. No status bits are changed. (Example) Host Processor Display Device  X = Don't care											
Restriction	This command has no effect when the module is already in inversion off mode.											
Flow Chart												

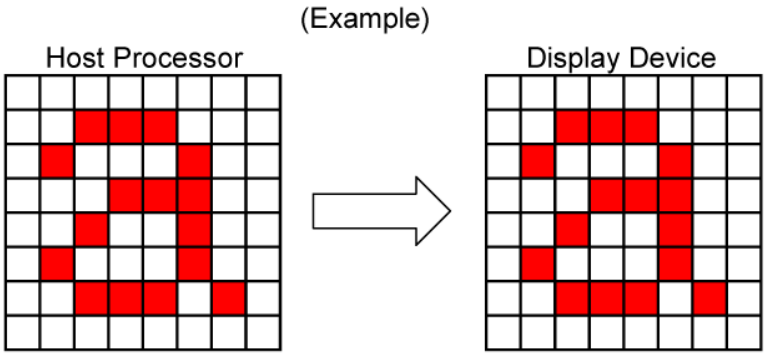
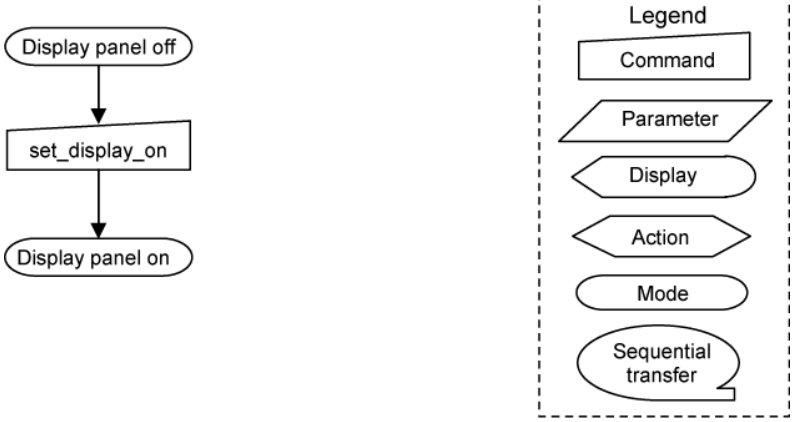
enter_invert_mode: 21h

21h	enter_invert_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	0	0	0	1	21h
Parameter	None											
Description	This command causes the display module to invert image data only on the display device. No status bits are changed.  X = Don't care											
Restriction	This command has no effect when the display module is already inverting the display image. This command disables BLC functions.											
Flow Chart	 											

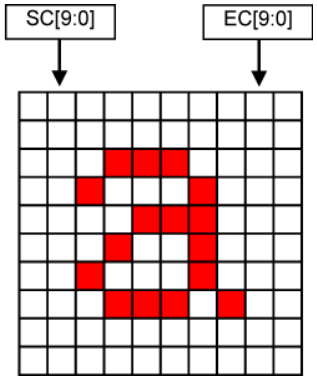
set_display_off: 28h

28h	set_display_off											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	1	0	0	0	28h
Parameter	None											
Description	This command causes the display module to stop displaying image data on the display device. No status bits are changed. (Example) Host Processor  Display Device  X = Don't care											
Restriction	This command has no effect when the display panel is already off. Do not use this command with DSI Data Type (22h and 32h) and DCS commands (10h, 11h, 28h, and 29h).											
Flow Chart												

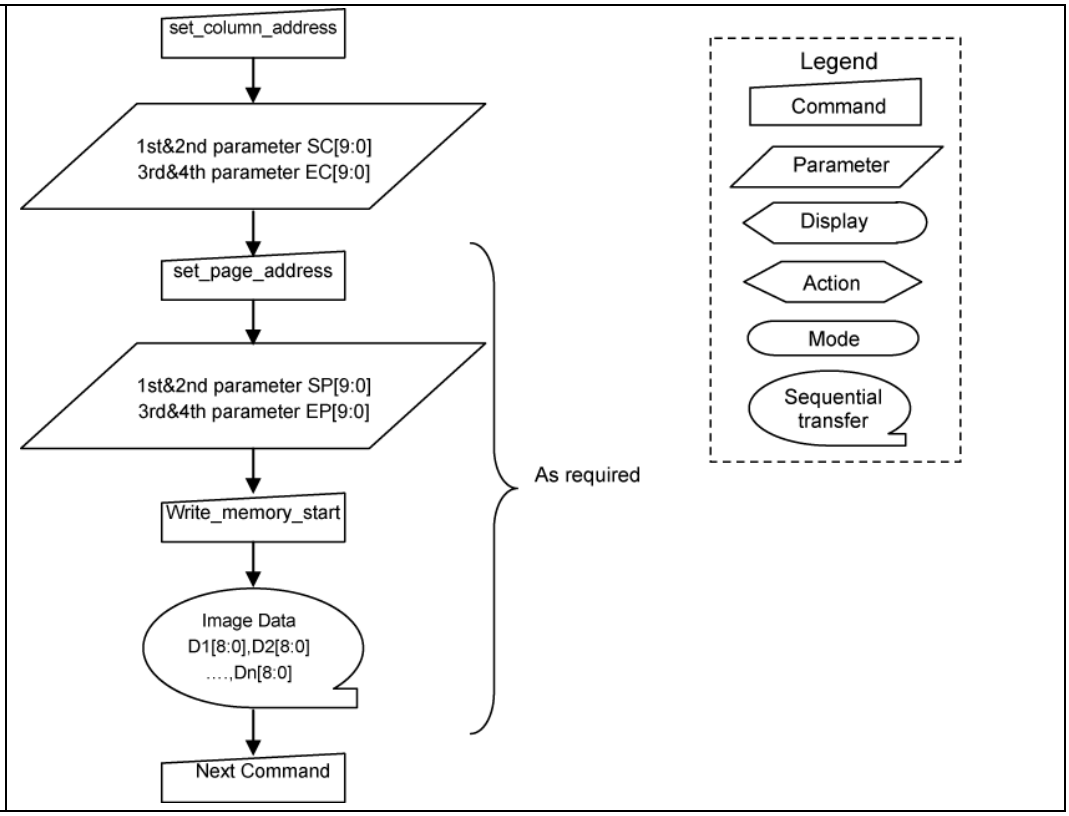
set_display_on: 29h

29h	set_display_on											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	1	0	0	1	29h
Parameter	None											
Description	This command causes the display module to start displaying the image data on the display device. No status bits are changed.  X = Don't care											
Restriction	This command has no effect when the display panel is already on. Do not use this command with DSI Data Type (22h and 32h) and DCS commands (10h, 11h, 28h, and 29h).											
Flow Chart	 											

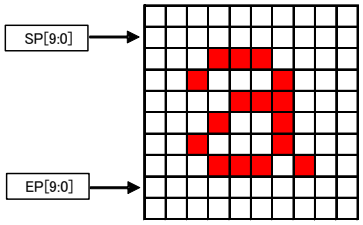
set_column_address: 2Ah

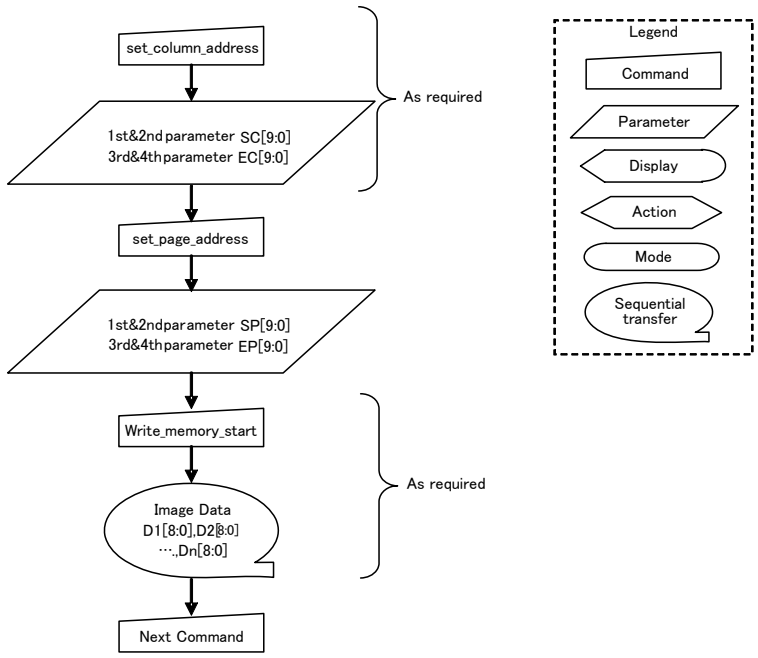
2Ah	set_column_address											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	1	0	1	0	2Ah
1st parameter	H→D	1	X	0	0	0	0	0	0	SC[9]	SC[8]	0Xh
2nd parameter	H→D	1	X	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]	XXh
3rd parameter	H→D	1	X	0	0	0	0	0	0	EC[9]	EC[8]	0Xh
4th parameter	H→D	1	X	EC[7]	EC[6]	EC[5]	EC[4]	EC[3]	EC[2]	EC[1]	EC[0]	XXh
Description	This command defines the column extent of the frame memory accessed by the host processor. The values of SC[9:0] and EC[9:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. No status bits are changed. (Example)  X=Don't care											
Restriction	SC [9:0] must be equal to or less than EC[9:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SC[9:0] or EC[9:0] > 1DFh • If set_address_mode B5 = 1: SC[9:0] or EC[9:0] > 35Fh											

Flow Chart



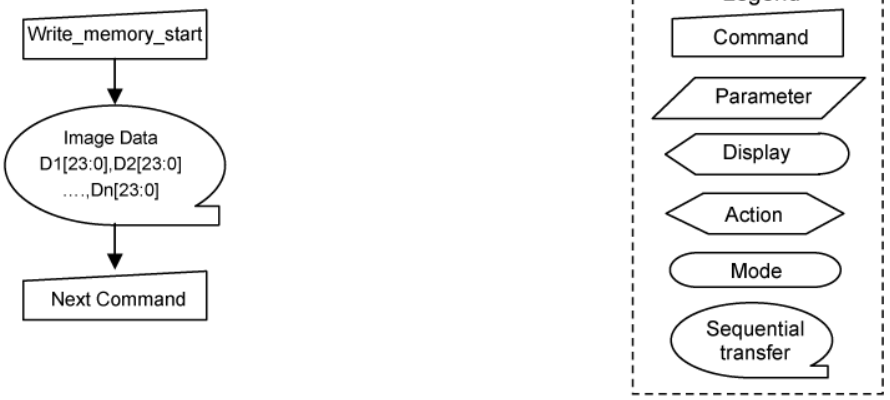
set_page_address: 2Bh

2Bh	set_page_address											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	1	0	1	1	2Bh
1st parameter	H→D	1	X	0	0	0	0	0	0	SP[9]	SP[8]	0Xh
2nd parameter	H→D	1	X	SP[7]	SP[6]	SP[5]	SP[4]	SP[3]	SP[2]	SP[1]	SP[0]	XXh
3rd parameter	H→D	1	X	0	0	0	0	0	0	EP[9]	EP[8]	0Xh
4th parameter	H→D	1	X	EP[7]	EP[6]	EP[5]	EP[4]	EP[3]	EP[2]	EP[1]	EP[0]	XXh
Description	This command defines the page extent of the frame memory accessed by the host processor. No status bits are changed. The values of SP[9:0] and EP[9:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. Example  X = Don't care											
Restriction	SP[9:0] must always be equal to or less than EP[9:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SP[9:0] or EP[9:0] > 1DF • If set_address_mode B5 = 1: SP[9:0] or EP[9:0] > 13F											

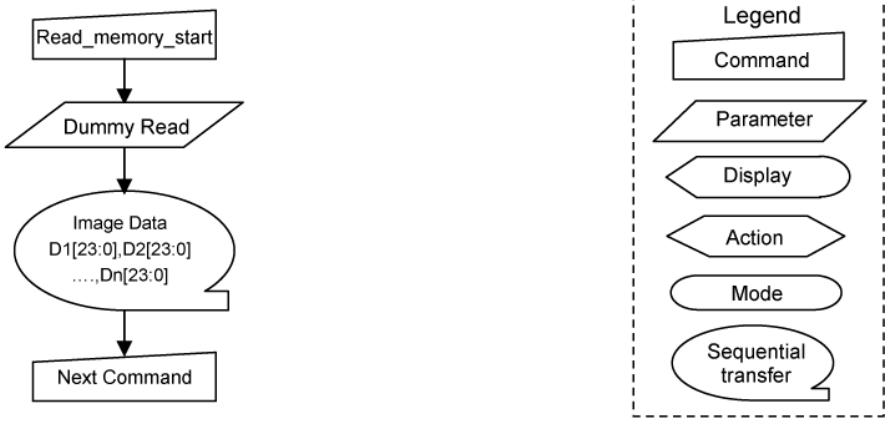
2Bh	set_page_address
Flow Chart	

write_memory_start: 2Ch

2Ch	write_memory_start											
	Direction	RDX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	1	X	0	0	1	0	1	1	0	0	2Ch
1st parameter	H→D	1	D1 [23:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
: :	H→D	1	Dx [23:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth parameter	H→D	1	Dn [23:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the host processor to the display module's frame memory. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data 1 is stored in frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If Frame Memory Access and Interface setting (B3h) WEMODE = 0: If the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. If Frame Memory Access and Interface setting (B3h) WEMODE = 1 When the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the column register and the page register are set to the Start Column and Start Page respectively. Then subsequent data are written to the frame memory. Sending any other command will stop writing to the frame memory. See DBI Data Format and DSI Data Format for write data formats in DBI Type B 24-/18-/16-/8-bit bus interface and DSI. X=Don't care.											
Restriction	In all color modes, there are no restrictions on the length of parameters. If data is not transferred in units of pixels, the extra data is regarded as invalid.											

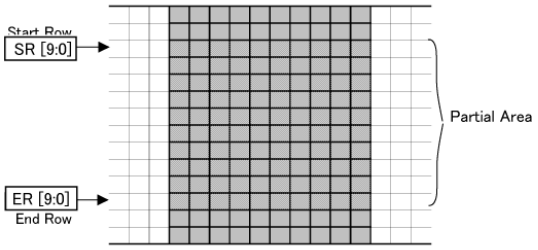
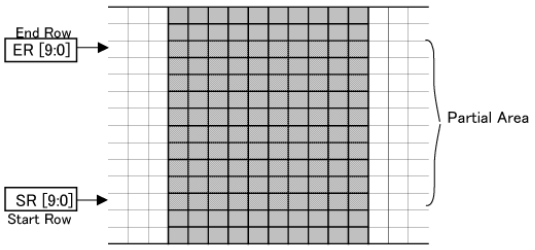
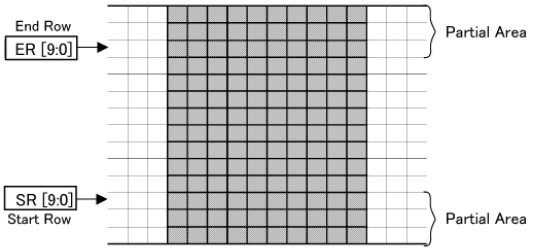
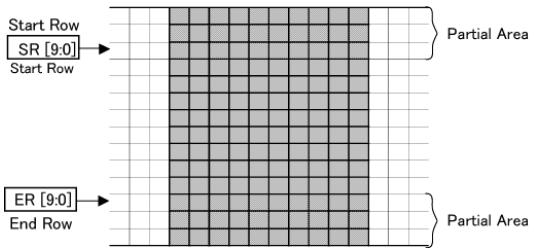
2Ch	write_memory_start
Flow Chart	

read_memory_start: 2Eh

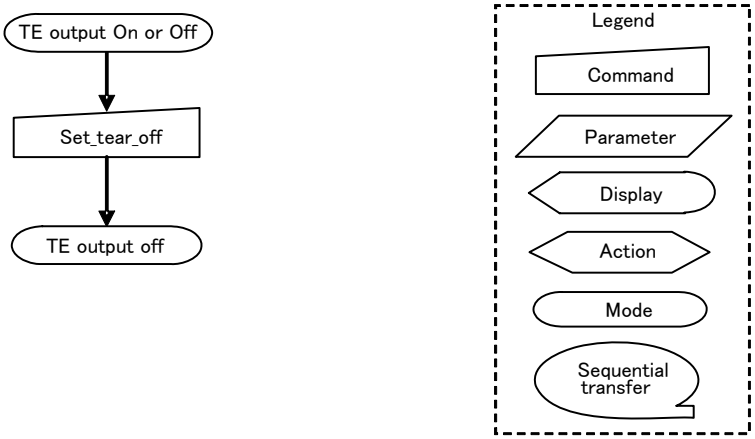
2Eh	read_memory_start											
	Direction	RDX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	1	X	0	0	1	0	1	1	1	0	2Eh
Dummy parameter	D→H	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	D→H	1	D1 [23:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
:	D→H	1	Dx [23:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth parameter	D→H	1	Dn [23:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the frame memory to the host processor. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data I are read from the frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If read operation continued after (EP, EC) data are read, the last data (EP, EC) continue to be read. Any other written command stops frame memory read. See DBI Data Format and DSI Data Format for read data formats in DBI Type B 24-/18-/16-/8-bit bus interface and DSI, respectively. X = Don't care.											
Restriction	In all color modes, the Frame read is always 24 bits so there is no restriction on the length of parameters. If data is not transferred in units of pixels, the extra data is regarded as invalid.											
Flow Chart	 Note : When reading by DSI, there is no dummy read.											

set_partial_area: 30h

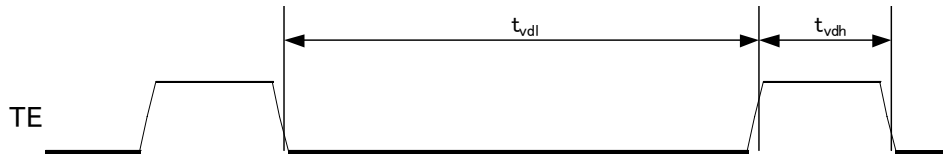
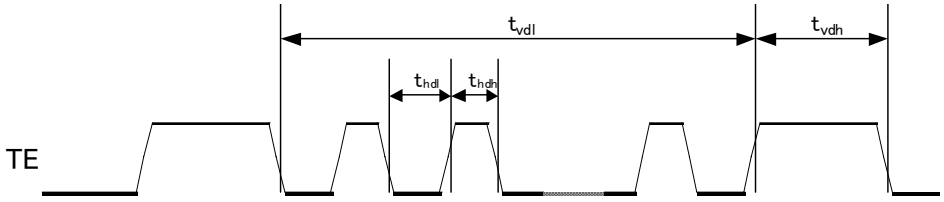
30h	set_partial_area											
	Direction	RDX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	1	X	0	0	1	1	0	0	0	0	30h
1st parameter	H→D	1	X	0	0	0	0	0	0	SR[9]	SR[8]	000h… 35Fh
2nd parameter	H→D	1	X	SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]	
3rd parameter	H→D	1	X	0	0	0	0	0	0	ER[9]	ER[8]	000h… 35Fh
4th parameter	H→D	RDX	X	ER[7]	ER[6]	ER[5]	ER[4]	ER[3]	ER[2]	ER[1]	ER[0]	

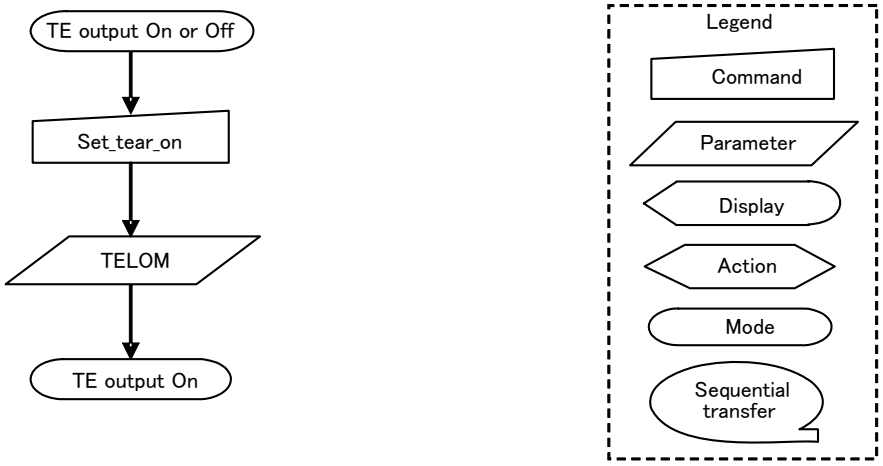
30h	set_partial_area
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. End Row > Start Row (set_address_mode(36h) B4=0)  End Row > Start Row(set_address_mode(36h) B4=1)  End Row < Start Row (set_address_mode(36h) B4=0)  End Row < Start Row (set_address_mode(36h) B4=1)  If End Row = Start Row, the partial area will be one row deep. X = Don't care.
Restriction	SR[9:0] and ER[9:0] must not be greater than a value set by NL. The bits other than SR[9:0] and ER[9:0] are "Don't care".

set_tear_off: 34h

34h	set_tear_off											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	0	1	0	0	34h
Parameter	None											
Description	This command turns off the Tearing Effect output signal from the TE signal line. X = Don't care											
Restriction	This command has no effect when Tearing Effect output is already off.											
Flow Chart												

set_tear_on: 35h

35h	set_tear_on											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	0	1	0	1	35h
Parameter	H→D	1	X	X	X	X	X	X	X	X	TELOM	XXh
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line. The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Refresh order). The Tearing Effect Line On has one parameter, TELON, that describes the Tearing Effect Output Line mode. See TE Pin Output Signal" for detail. TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only. The Tearing Effect Output line shall be high during vertical blanking period.  TELOM = 1: The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.  Vertical blanking period: Non-lit display period in (back porch + front porch + partial mode) Note 1: The Tearing Effect Output line shall be active low when the display module is in Sleep mode. Note 2: The Tearing Effect Output line shall be active low when the display module is in Sleep mode. X = Don't care											
Restriction	This command has no effect when Tearing Effect output is already ON. Changes in parameter TELOM is enabled from the next frame period.											

35h	set_tear_on
Flow Chart	

set_address_mode: 36h

36h	set_address_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	0	1	1	0	36h
1st parameter	H→D	1	X	B7	B6	B5	0	B3	0	0	B0	00h

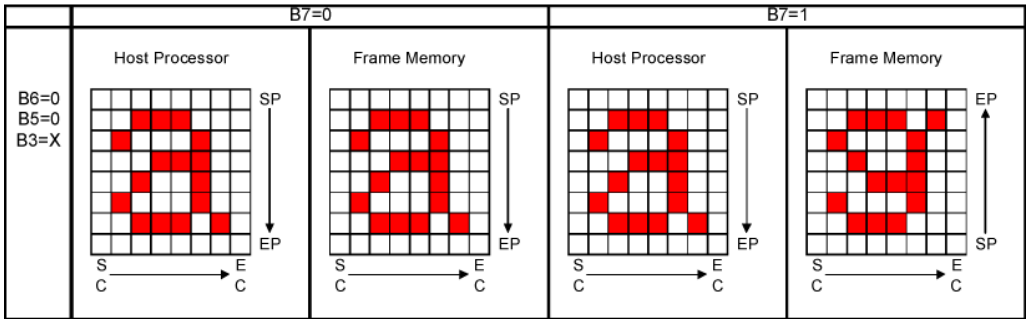
Description

This command sets read/write scanning direction of frame memory. No status bits are changed.

Bit	Description	Comment	Symbol	
			Command mode	Video mode
D7	Page Address Order	-	B7	-
D6	Column Address Order	-	B6	B6
D5	Page/Column Addressing Order	-	B5	-
D4	Display Device Line Refresh Order	Set to '0'.	-	-
D3	RGB/BGR Order	-	B3	B3
D2	Display Data Latch Data Order	Set to '0'.	-	-
D1	Flip Horizontal	Set to '0'.	-	-
D0	Flip Vertical	-	B0	-

- Bit D7 – Page Address Order

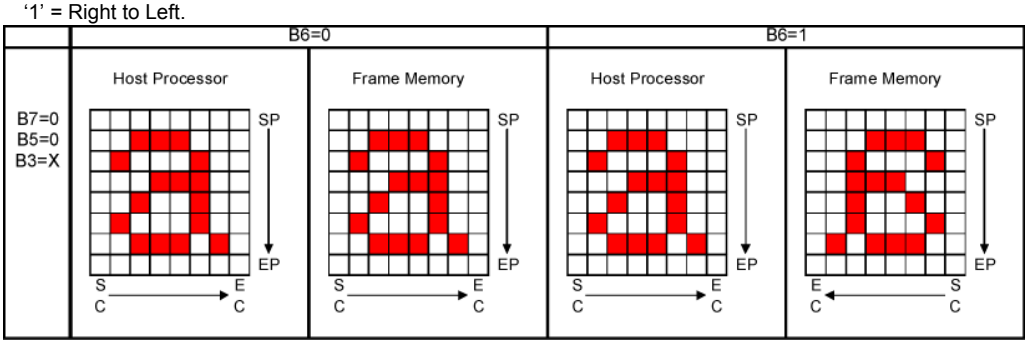
'0' = Top to Bottom.
'1' = Bottom to Top.



Description

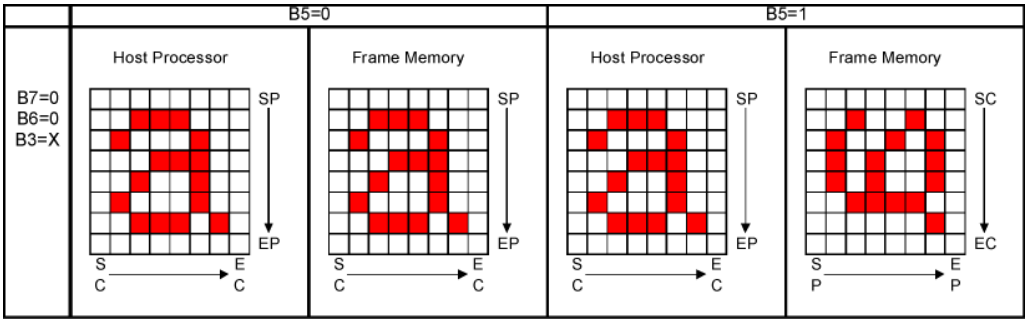
- Bit D6 – Column Address Order

'0' = Left to Right.
'1' = Right to Left.



- Bit D5 – Page/Column Addressing Order

'0' = Normal Mode.
'1' = Reverse Mode.



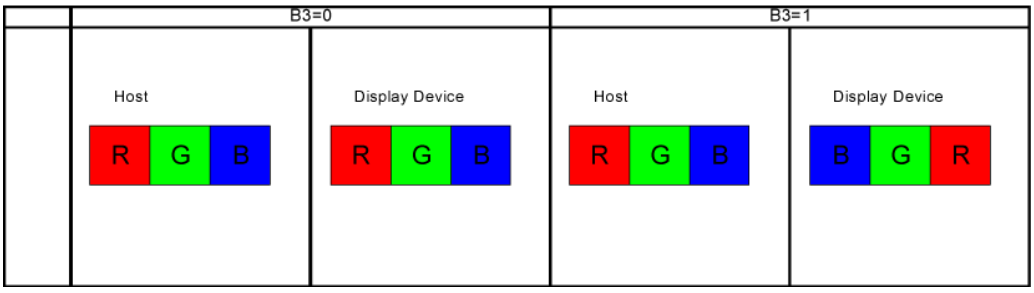
For bits B7 to B5, see "Frame Memory." Set B5 to 0 when DSI is used (B5 set to 1 is not supported).

- Bit D4 – Display Device Line Refresh Order

This bit is not applicable. Set to '0'. (Not supported)

- Bit D3 – RGB/BGR Order

'0' = RGB.
'1' = BGR.
The figure below shows relationships between pixel data sent from the host and display. For details, see "Relationship between Input Data and Display."



<table>
<tr><td>Description</td><td>

- Bit D2 – Display Data Latch Order

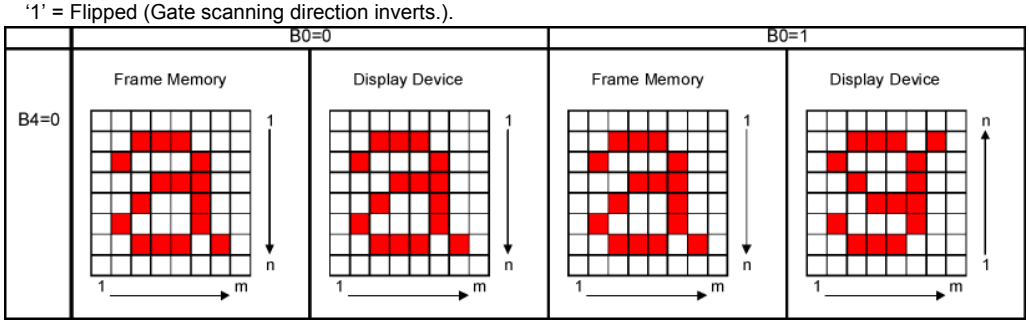
This bit is not applicable. Set to ‘0’. (Not supported)

- Bit D1 – Flip Horizontal

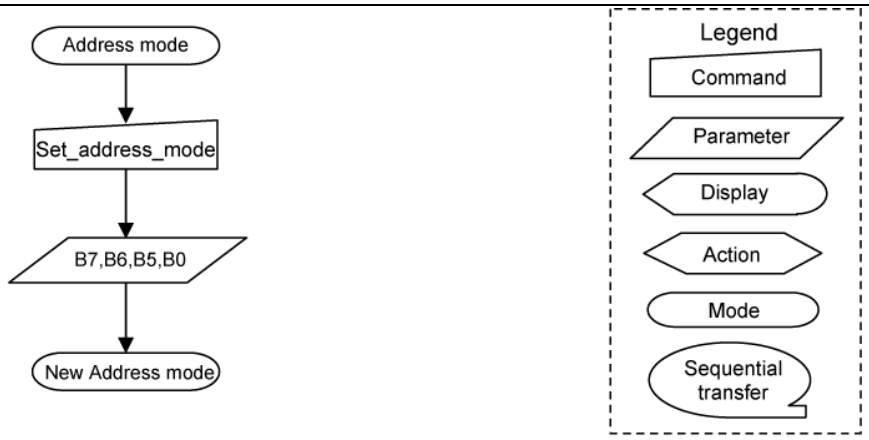
This bit is not applicable. Set to ‘0’. (Not supported)

- Bit D0 – Flip Vertical

‘0’ = Normal.
‘1’ = Flipped (Gate scanning direction inverts.).



</td></tr>
<tr><td>Flow Chart</td><td>



</td></tr>
</table>

The relationship between input data and display.

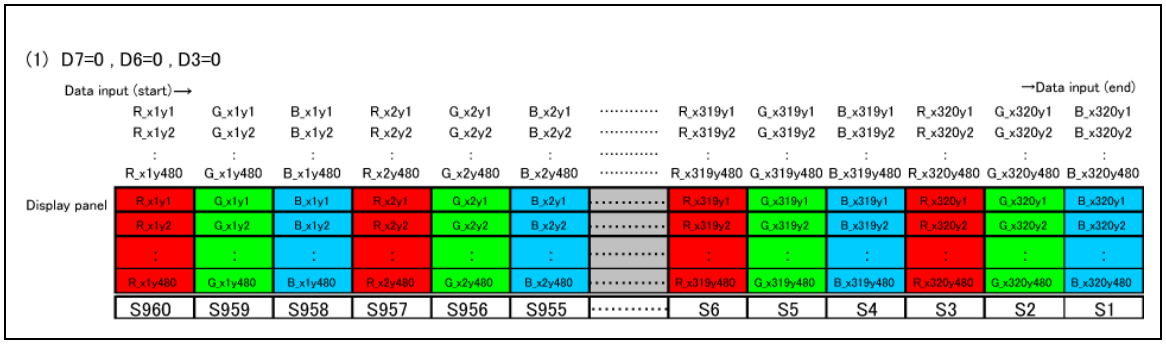


Figure 109

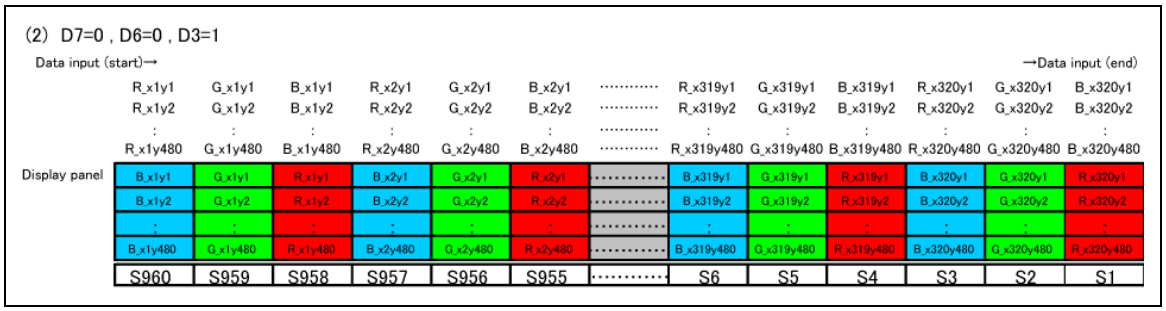


Figure 110

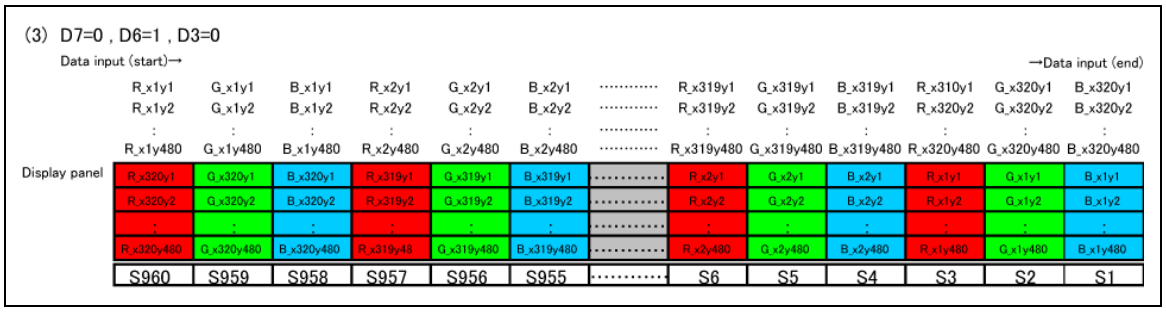


Figure 111

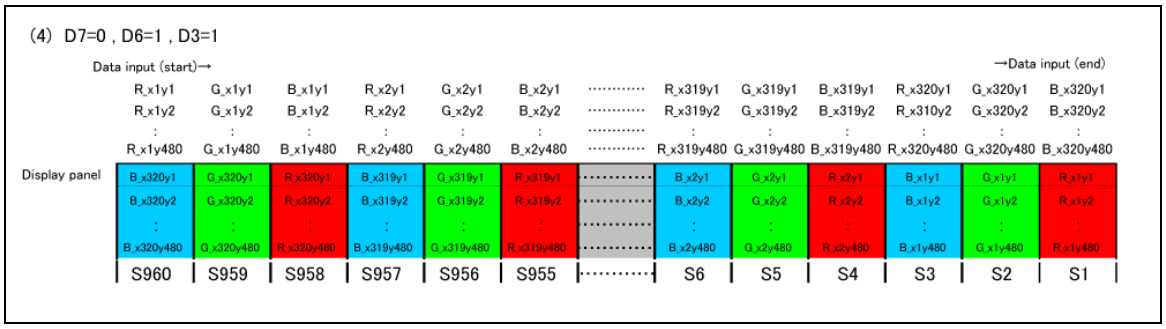


Figure 112

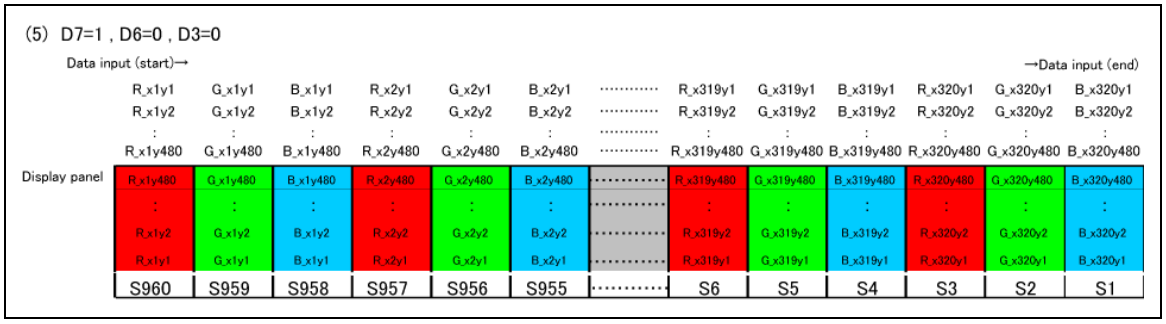


Figure 113

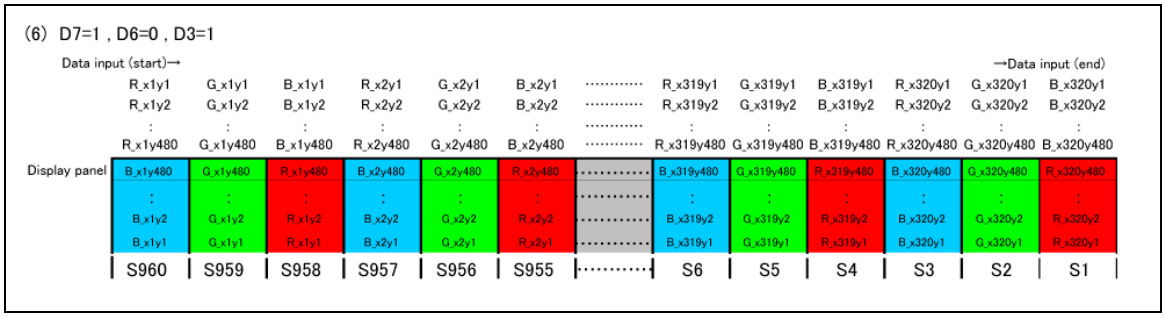


Figure 114

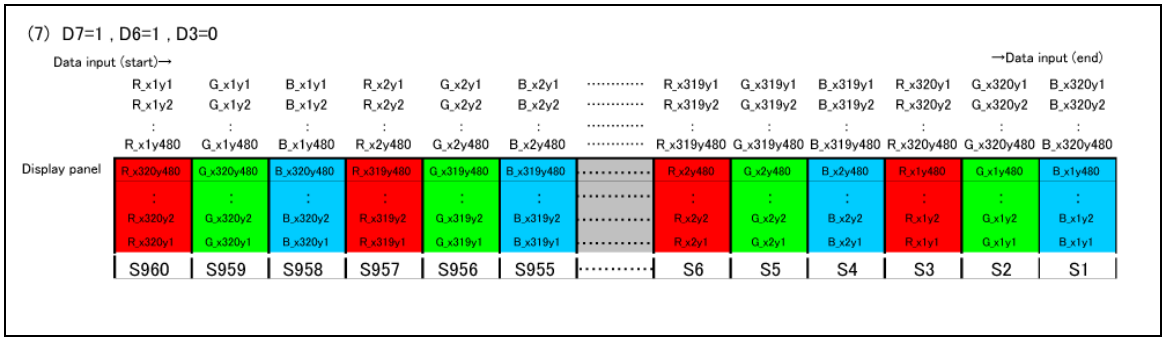


Figure 115

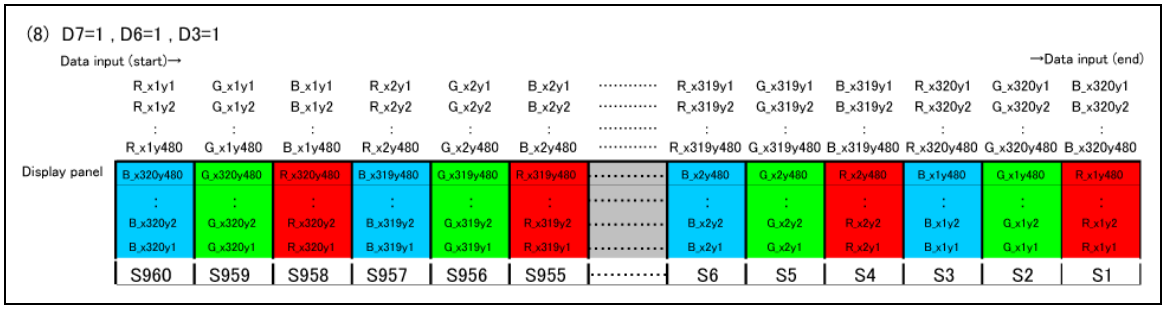
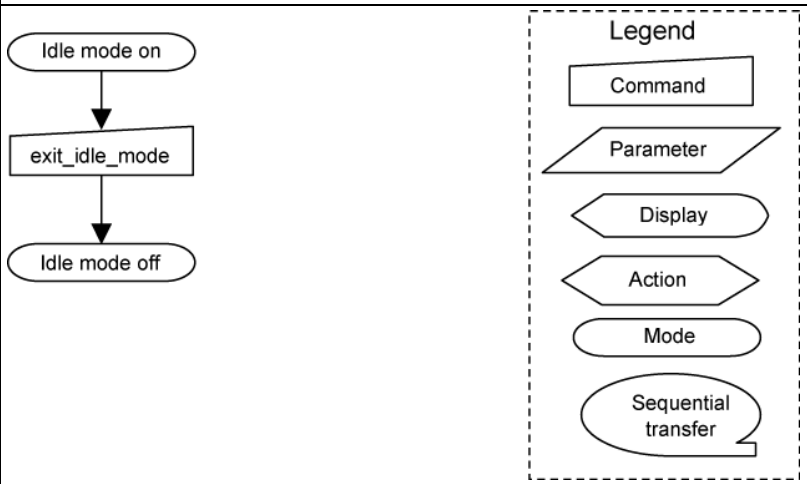


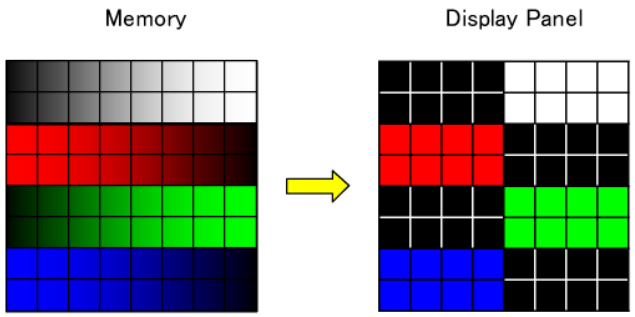
Figure 116

exit_idle_mode: 38h

38h	exit_idle_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	1	0	0	0	38h
Parameter	None											
Description	This command causes the display module to exit Idle mode. LCD can display up to maximum 16,777,216 colors. X = Don't care											
Restriction	This command has no effect when the display module is not in Idle mode.											
Flow Chart												

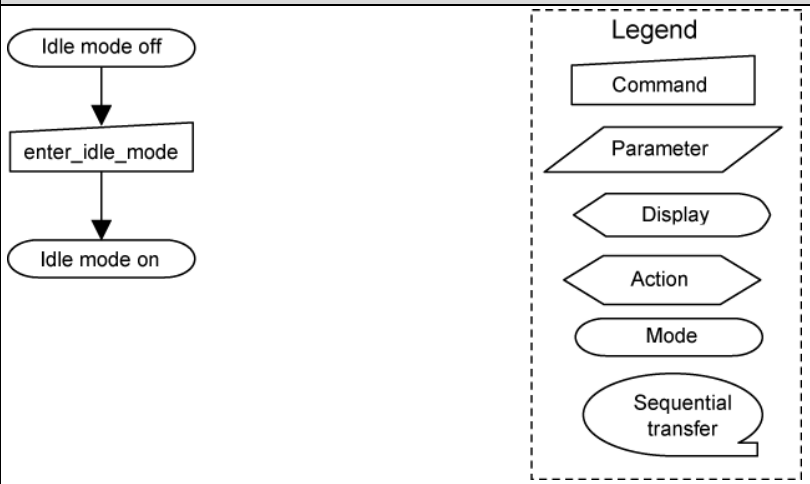
enter_idle_mode: 39h

39h	enter_idle_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	1	0	0	1	39h
Parameter	None											
Description	This command causes the display module to enter Idle mode. In Idle mode, color expression is reduced. Eight color depth data are displayed using MSB of each R, G and B color components in the Frame Memory. In this mode, only grayscale levels V0 and V255 are used and power supplies for other levels V1-V254 are halted, reducing power consumption. It is possible to reduce power consumption by optimizing settings for Idle Mode. Gamma settings (Gamma Set A-B (C8-Ah)) for each R, G, B are enabled when Idle Mode is On.											
Restriction	This command has no effect when module is already in Idle mode.											



Memory Contents vs. Display Color			
	R[7:0]	G[7:0]	B[7:0]
Black	0 X X X X X	0 X X X X X	0 X X X X X
Blue	0 X X X X X	0 X X X X X	1 X X X X X
Red	1 X X X X X	0 X X X X X	0 X X X X X
Magenta	1 X X X X X	0 X X X X X	1 X X X X X
Green	0 X X X X X	1 X X X X X	0 X X X X X
Cyan	0 X X X X X	1 X X X X X	1 X X X X X
Yellow	1 X X X X X	1 X X X X X	0 X X X X X
White	1 X X X X X	1 X X X X X	1 X X X X X

X = Don't care

39h	enter_idle_mode
Flow Chart	

set_pixel_format: 3Ah

3Ah	set_pixel_format											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	1	0	1	0	3Ah
1st parameter	H→D	1	X	0	D6	D5	D4	0	D2	D1	D0	XXh

Description

This command is used to define the format of RGB picture data, which are to be transferred via the DPI/DSI/MDDI.

Bits D6, D5, and D4 are used in MIPI DPI operation, MIPI DSI Video Mode, and MDDI Video Mode. Bits D2, D1, and D0 are used in MIPI DBI operation, MIPI DSI Command Mode, MDDI Command Mode, and I2C operation.

The formats are shown in the following table. Set Bits D7 and D3 to 0.

Control Interface Color Format	D6/D2	D5/D1	D4/D0
Setting inhibited	0	0	0
Setting inhibited	0	0	1
Setting inhibited	0	1	0
Setting inhibited	0	1	1
Setting inhibited	1	0	0
16 bits/pixel (65,536 colors)	1	0	1
18 bits/pixel (262,144 colors)	1	1	0
24 bits/pixel (16,777,216 colors)	1	1	1

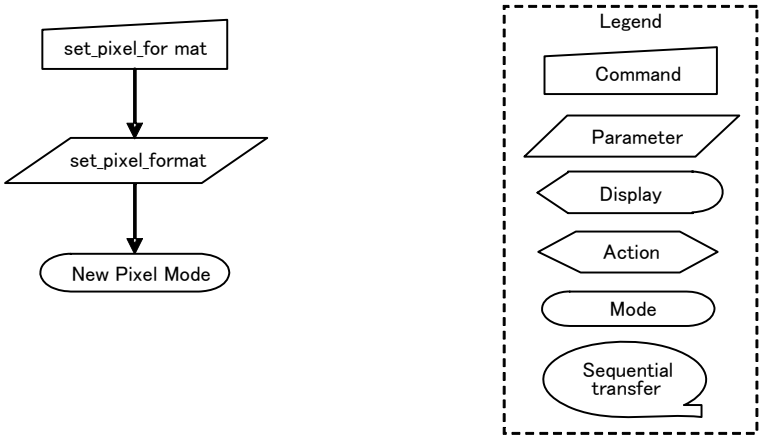
For each data format, see the corresponding section.

Note: When “Setting inhibited” is set, undesirable image will be displayed on the panel.

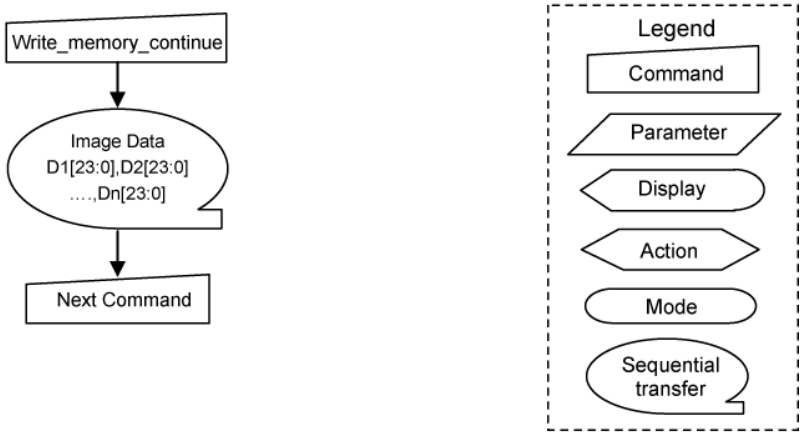
X = Don’t care

Restriction: -

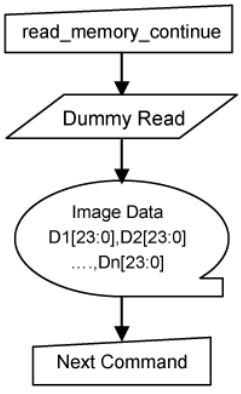
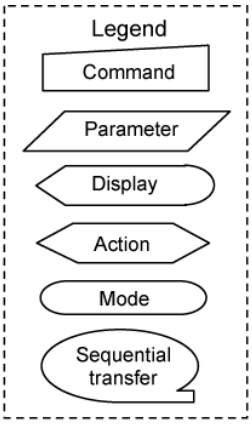
Flow Chart



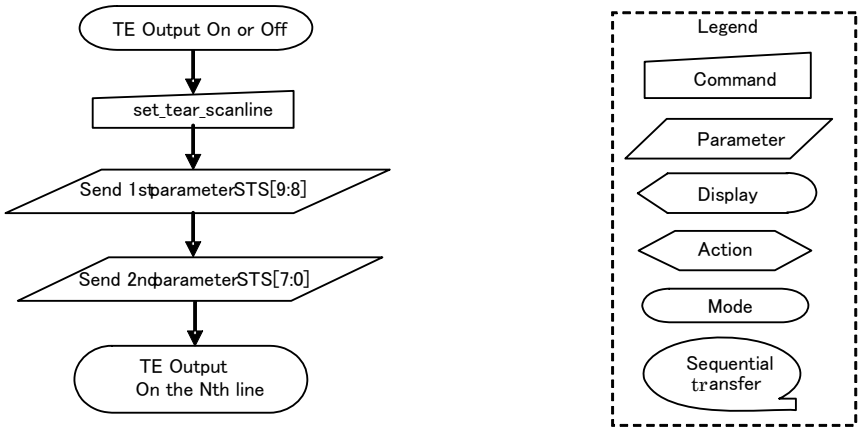
write_memory_continue: 3Ch

3Ch	write_memory_continue											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	x	0	0	1	1	1	1	0	0	3Ch
1st parameter	H→D	1	D1 [23:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … FFFh
:	H→D	1	Dx [23:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … FFFh
Nth parameter	H→D	1	Dn [23:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … FFFh
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Frame Memory Access and Interface setting (B3h): WEMODE = 0 If the number of pixels in the transfer data exceed (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. Frame Memory Access and Interface setting (B3h): WEMODE = 1 When the number of pixels in the transfer data exceed (EC-SC+1)*(EP-SP+1), the column register and the page register are reset to the Start Column/Start Page positions, and the subsequent data are written to the frame memory. X=Don't care											
Restriction	If write_memory_continue command is executed without setting set_column_address (2Ah), set_page_address (2Bh), and set_address_mode (36h), there is no guarantee that data are correctly written to the frame memory. If data is not transferred in units of pixels, the extra data is regarded as invalid.											
Flow Chart												

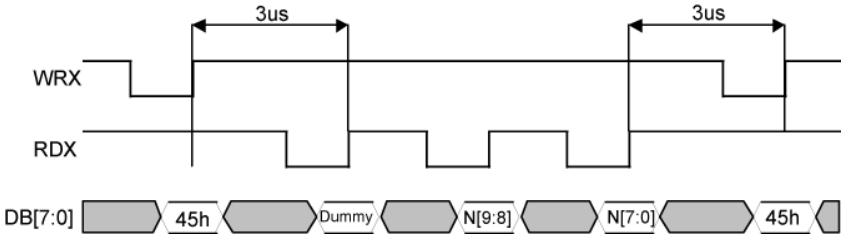
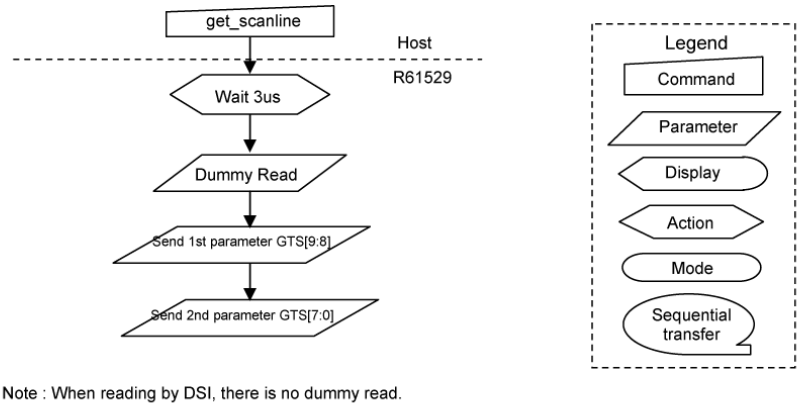
read_memory_continue: 3Eh

3Eh	read_memory_continue											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	x	0	0	1	1	1	1	1	0	3Eh
Dummy parameter	D→H	1	x	X	X	X	X	X	X	X	X	XXh
1st Pixel data	D→H	1	D1 [23:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h… FFFh
:	D→H	1	Dx [23:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h… FFFh
Nth Pixel data	D→H	1	Dn [23:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h… FFFh
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the location following the previous read_memory_continue or read_memory_start command. If read operation is executed after (EP. EC) is read, the last data (EP, EC) continue to output. After pixel data 1 are written to frame memory (SC, SP), address counter's direction differs depending on setting of set_address_mode (36h)'s Bits 5, 6, 7. See "Host Processor to Memory Write/Read Direction". X = Don't care											
Restriction	In any color mode, format returned by read_memory_continue is always 24 bits so there is no restriction on the length of parameter. If data is not transferred in units of pixels, the extra data is regarded as invalid.											
Flow Chart	  Note : When reading by DSI, there is no dummy read.											

set_tear_scanline:44h

44h	set_tear_scanline											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	x	0	1	0	0	0	1	0	0	44h
1st Parameter	H→D	1	x	0	0	0	0	0	0	STS [9]	STS [8]	0Xh
2nd Parameter	H→D	1	x	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	XXh
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N defined by STS [9:0]. TE line is unaffected by change in B4 bit of set_address_mode command. See figure in "TE Pin Output Signal". X =don't care.											
Restriction	The command takes affect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set_tear_on and set_tear_scanline commands until the end of currently scanned frame. Setting is disabled when TELOM=1 of set_tear_on (35h). Make sure that STS [9:0] ≤ NL (number of line) + 1.											
Flow Chart												

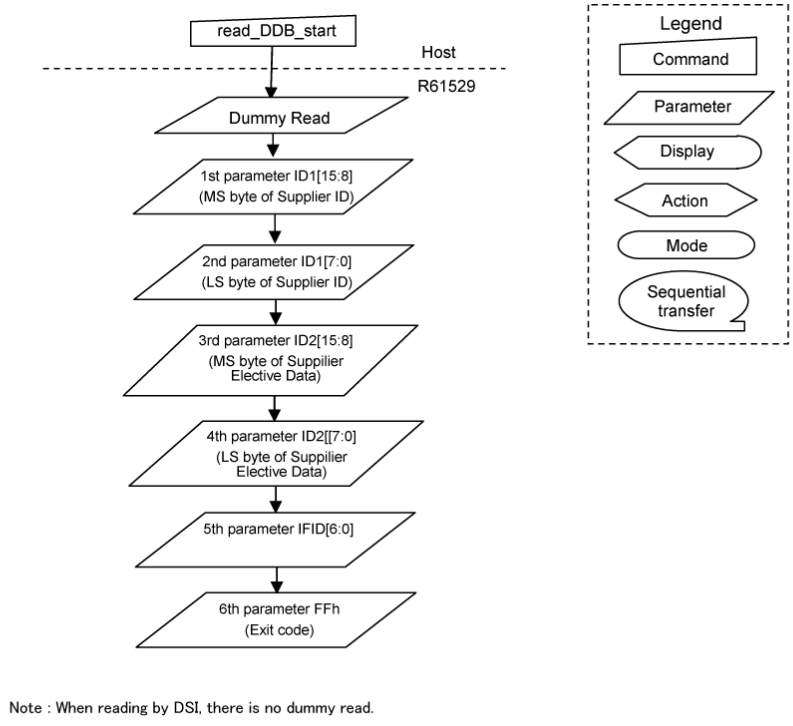
get_scanline: 45h

45h	get_scanline											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	x	0	1	0	0	0	1	0	1	45h
Dummy parameter	D→H	1	x	X	X	X	X	X	X	X	X	XXh
1st parameter	D→H	1	x	0	0	0	0	0	0	GTS [9]	GTS [8]	0Xh
2nd parameter	D→H	1	x	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	XXh
Description	The display module returns the current scan line. The total number of scan lines is defined as (BP + NL + FP). The first scan line of back porch period is defined as line 0. In sleep mode, the value returned by get_scanline is undefined. X = Don't care											
Restriction	After get_line command is input, it takes 3µs or more to read it. After parameters are read, wait 3µs or more to input this command again. 											
Flow Chart	 Note : When reading by DSI, there is no dummy read.											

read_DDB_start: A1h

A1h	read_DDB_start											
	Direction	DCX	DB23-DB8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	H → D	0	X	1	0	1	0	0	0	0	1	A1h
Dummy parameter	D → H	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	D → H	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd parameter	D → H	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd parameter	D → H	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th parameter	D → H	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th parameter	D → H	1	X	0	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	XXh
6th parameter	D → H	1	X	EEC [7]	EEC [6]	EEC [5]	EEC [4]	EEC [3]	EEC [2]	EEC [1]	EEC [0]	XXh
Description	The command returns information from the display module as follows: 1st parameter: MS byte of Supplier ID (ID1[15:8]) 2nd parameter: LS byte of Supplier ID (ID1[7:0]) 3rd parameter: Supplier Elective Data (ID2[15:8]) 4th parameter: Supplier Elective Data (ID2[7:0]) 5th parameter: IFID[6:0] 6th parameter: EEC[7:0] Supplier ID and Supplier Elective Data stored in internal NVM are read. X = Don't care											
Restriction	-											

Flow Chart

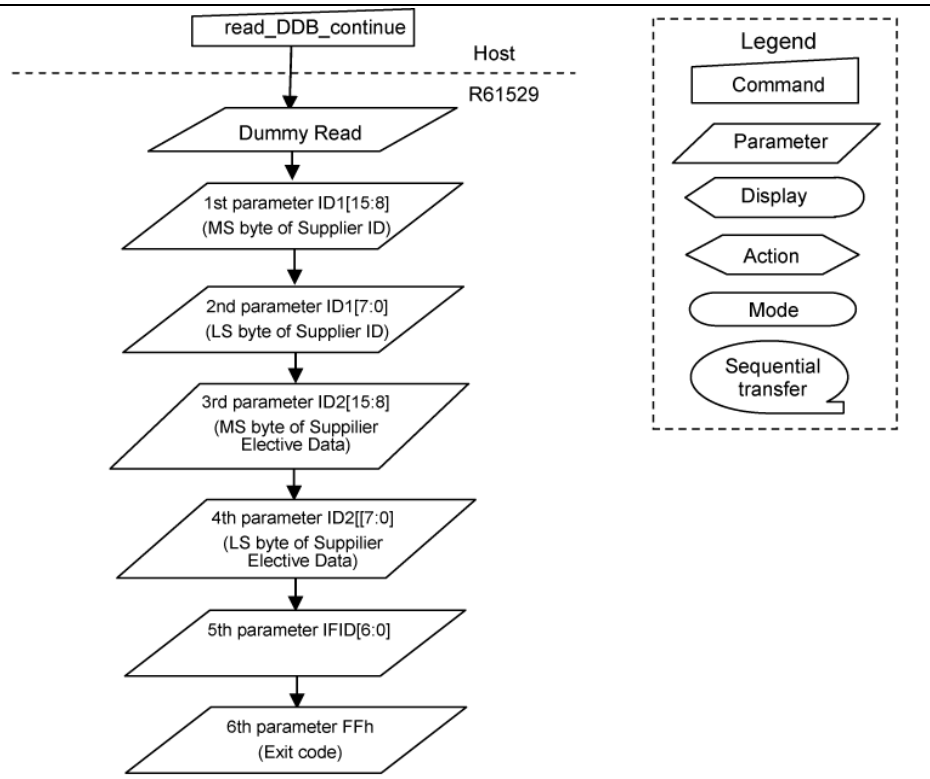


Note : When reading by DSI, there is no dummy read.

read_DDB_continue: A8h

A8h	read_DDB_continue											
	Direction	DCX	DB23-DB8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	H → D	0	X	1	0	1	0	0	0	0	1	A8h
Dummy parameter	D → H	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	D → H	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd parameter	D → H	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd parameter	D → H	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th parameter	D → H	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th parameter	D → H	1	X	0	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	XXh
6th parameter	D → H	1	X	EEC [7]	EEC [6]	EEC [5]	EEC [4]	EEC [3]	EEC [2]	EEC [1]	EEC [0]	XXh
Description	This command continues read operation from the position where the operation is halted by read_DDB_continue or read_DDB_start. For the position that information is returned, see read_DDB_start (A1h). X=Don't care											
Restriction	To fix the position that information is returned, execute read_DDB_start command and parameter read operation at least once before read_DDB_continue command is executed. If they are not executed, the value returned by read_DDB_continue command is invalid. [When MIPI DSI is selected] To fix the position that information is returned, execute read_DDB_start command at least twice and parameter read operation at least once before read_DDB_continue command is executed. If they are not executed, the value returned by read_DDB_continue command is invalid. After the 1st parameter of read_DDB_start command is read, executing read_DDB_continue command makes the R61529 output the 3rd parameter without outputting the 2nd parameter. When this command is read via DSI or MDDI, dummy read operation is not performed.											

Flow Chart



Note : When reading by DSI, there is no dummy read.

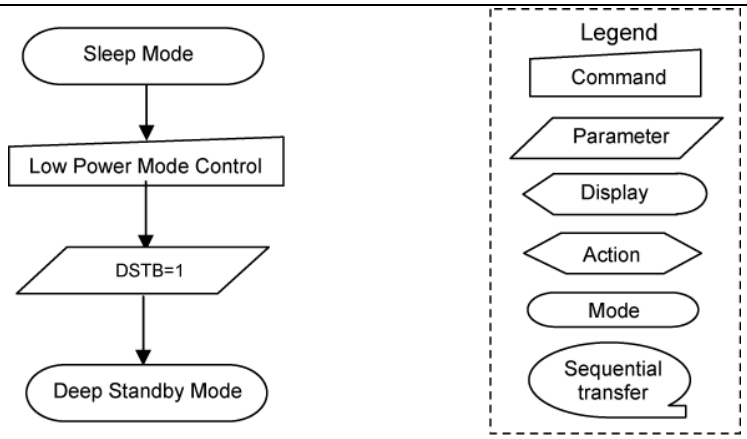
Manufacturer Command

Additional User Command

MCAP: Manufacturer Command Access Protect (B0h)

<table>
<tr><th>B0h</th><th colspan="12">MCAP(Manufacturer Command Access Protect)</th></tr>
<tr><td></td><td>W / R</td><td>DCX</td><td>DB23-DB8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>－</td><td>0</td><td>X</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>1st parameter</td><td>W / R</td><td>1</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>MCAP [1]</td><td>MCAP [0]</td><td>03h</td></tr>
<tr><td>Description</td><td colspan="12">MCAP[1:0]
The R61529 is required to release Access Packet before inputting a Manufacturer Command. This command releases parameters so that Manufacturer Command inputs are enabled. When the conditions to release Protect, as shown in the table above, are met, Manufacturer Command inputs are enabled.
<table>
<tr><th rowspan="2">Command</th><th colspan="4">MCAP[1:0]</th></tr>
<tr><th>2’b00</th><th>2’b01</th><th>2’b10</th><th>2’b11 (default)</th></tr>
<tr><td>B0h</td><td>Yes</td><td rowspan="3">Setting inhibited</td><td>Yes</td><td>Yes</td></tr>
<tr><td>B1h－BFh</td><td>Yes</td><td>Yes</td><td>No</td></tr>
<tr><td>C0h－FFh</td><td>Yes</td><td>No</td><td>No</td></tr>
</table>
Yes : Access Possible(Protect Off)
No : Access impossible(Protect On)
Once the R61529 enables Manufacturer Command inputs, it keeps the state until MCAP[2:0] is written so that the R61529 enters Protect ON state again.</td></tr>
<tr><td>Restriction</td><td colspan="12">After H/W Reset or exiting Deep Standby Mode, accessing a Manufacturer Command is restricted so that Manufacturer Commands B1h-BFh inputs are identified as nop command.</td></tr>
</table>

Low Power Mode Control (B1h)

B1h	Low Power Mode Control											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	X	1	0	1	1	0	0	0	1	B1h
1st parameter	W / R	1	X	0	0	0	0	0	0	0	DSTB	00h
Description	This command is used to enter the Deep Standby Mode. **DSTB** The driver enters the Deep Standby Mode when DSTB=1. Internal logic power supply circuit (VDD) is turned down enabling low power consumption. In the Deep Standby mode, data stored in the frame memory and the instructions are not retained. Rewrite them after the Deep Standby mode is exited. Do not input soft_reset command and other commands in deep standby mode.											
Restriction	Deep standby mode can be set in only Sleep Mode On. Accessing DSTB in Sleep Mode Off is regarded (treated as nop command). When this command is read via DSI or MDDI, dummy read operation is not performed.											
Flow Chart												

Frame Memory Access and Interface Setting (B3h)

B3h	Frame Memory Access and Interface Setting											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	0	1	1	0	0	1	1	B3h
1st parameter	W / R	1	x	0	0	0	0	0	0	WE MODE	0	0Xh
2nd parameter	W / R	1	x	0	0	0	0	0	TEI [2]	TEI [1]	TEI [0]	XXh
3rd parameter	W / R	1	X	0	0	0	0	0	DENC [2]	DENC [1]	DENC [0]	XXh
4th parameter	W / R	1	X	0	0	EPF [1]	EPF [0]	0	0	0	DFM [0]	XXh

Description

WEMODE

WEMODE	Window group setting for memory write
0	The write start position is not reset to the start of window address, and the subsequent data are disregarded.
1	The write start position is reset to the start of window address area to overwrite the subsequent data to the previous data.

EPF[1:0]

This bit is used to set data format when 16/18bpp (R,G,B) data are converted to 24bpp (r,g,b) stored in internal frame memory (24bpp).

EPF[1:0]	18bpp (R, G, B) → 24bpp (r, g, b)	16bpp (R, G, B) → 24bpp (r, g, b)
2'h0	"0" is written to the LSB. r[7:0]={ R[5:0], 2'h0 } g[7:0]={ G[5:0], 2'h0 } b[7:0]={ B[5:0], 2'h0 } Note that the data are converted as follows: R[5:0], B[5:0]=6'h3F → r, b[7:0]=8'hFF G[5:0]=6'h3F → g[7:0]=8'hFF	"0" is written to the LSB. r[7:0]={ R[5:0], 2'h0 } g[7:0]={ G[5:0], 2'h0 } b[7:0]={ B[5:0], 2'h0 } Note that the data are converted as follows: R[4:0], B[4:0]=5'h1F → r, b[7:0]=8'hFF G[5:0]=6'h3F → g[7:0]=8'hFF
2'h1	"1" is written to the LSB. r[7:0]={ R[5:0], 2'h3 } g[7:0]={ G[5:0], 2'h3 } b[7:0]={ B[5:0], 2'h3 } Note that the data are converted as follows: R[5:0], B[5:0]=6'h0 → r, b[7:0]=8'h00 G[5:0]=6'h0 → g[7:0]=8'h00	"1" is written to the LSB. r[7:0]={ R[5:0], 2'h3 } g[7:0]={ G[5:0], 2'h3 } b[7:0]={ B[5:0], 2'h3 } Note that the data are converted as follows: R[4:0], B[4:0]=5'h0 → r, b[7:0]=8'h00 G[5:0]=6'h0 → g[7:0]=8'h00
2'h2	The MSB value is written to the LSB. r[7:0]={ R[5:0], R[5:4] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[5:0], B[5:4] }	The MSB value is written to the LSB. r[7:0]={ R[4:0], R[4:2] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[4:0], B[4:2] }
2'h3	Setting inhibited	

Description

Description

DFM[1:0]

The bit is used to define image data write/read format to the Frame Memory. For details, see a section of each data format.

TEI[2:0]

The bit is used to define interval between outputs of TE signal. Set in accordance with update cycle and transfer rate of the display data.

TEI[2:0]	Interval
0	Every frame
1	2 frames
3	4 frames
5	6 frames
Other than above	Setting inhibited

DENC[2:0]

The bit is used to define frame memory write cycle in DPI operation.

Set in accordance with update cycle of the display data.

DENC[2]	DENC[1]	DENC[0]	Frame Memory write cycle
0	0	0	Every frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	3 frames
1	0	0	4 frames
1	0	1	5 frames
1	1	0	6 frames
1	1	1	7 frames

Restriction

Display mode and Frame memory write mode (B4h)

<table>
<tr><th>B4h</th><th colspan="12">Display mode and Frame memory write mode</th></tr>
<tr><td></td><td>W / R</td><td>DCX</td><td>DB23-DB8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>–</td><td>0</td><td>x</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>B4h</td></tr>
<tr><td>1st parameter</td><td>R</td><td>1</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DM[1]</td><td>DM[0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="12">D M[1:0]
The bit is used to select display operation mode. The R61529 allows switching the display operation mode between internal clock operation mode and the external display operation mode by DM[1:0] setting. Switching from MIPI DPI interface operation to VSYNC interface operation and vise versa is prohibited. The setting is enabled switching operation in Standby mode only. The operation in other modes is not guaranteed.
<table>
<tr><th>DM[1:0]</th><th>Display mode</th></tr>
<tr><td>2’h0</td><td>Internal oscillation clock</td></tr>
<tr><td>2’h1</td><td>DPI signal</td></tr>
<tr><td>2’h2</td><td>VSYNC signal</td></tr>
<tr><td>2’h3</td><td>Setting inhibited</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
</table>

Read Checksum and ECC Error Count (B5h)

B5h	Read Checksum and ECC Error Count											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	0	1	1	0	1	0	1	B5h
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	x	CSOUT [7]	CSOUT [6]	CSOUT [5]	CSOUT [4]	CSOUT [3]	CSOUT [2]	CSOUT [1]	CSOUT [0]	XXh
2nd parameter	R	1	x	DSIECP[7]	DSIECP[6]	DSIECP[5]	DSIECP[4]	DSIECP[3]	DSIECP[2]	DSIECP[1]	DSIECP[0]	XXh
3rd parameter	R	1	x	DSIECE[7]	DSIECE[6]	DSIECE[5]	DSIECE[4]	DSIECE[3]	DSIECE[2]	DSIECE[1]	DSIECE[0]	XXh
Description	**CSOUT[7:0]** Reads Checksum Error count value. Checksum Error count value is counted up when the Checksum Error are occurred during DSI Long Packet receiving time. CSOUT[7:0] is cleared by 8'00 after the read operation. **DSIECP[7:0]** Reads Single ECC Error count value. Single ECC Error count value is counted up when 1-bit ECC Errors are occurred during DSI Packet Header receiving time. DSIEP[7:0] is cleared by 8'00 after the read operation. **DSIECE[7:0]** Reads Multiple ECC Error count value. Multiple ECC Error count value is counted up when 2-bit ECC Errors are occurred during DSI Packet Header receiving time. DSIECE[7:0] is cleared by 8'00 after the read operation.											
Restriction												

DSI Control (B6h)

B6h	DSI Control											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	X	1	0	1	1	0	1	1	0	B6h
1st parameter	W / R	1	X	0	1	0	1	0	0	DSITX DIV[1]	DSITX DIV[0]	3Xh
2nd parameter	W / R	1	X	DSI_THS SET[1]	DSI_THS SET [0]	0	0	0	0	1	0	X2h

Description

DSITXDIV[1:0]

These bits are used to define the division ratio to generate transmit clock in LP mode. If DSICLK stops, data is transmitted by using the internal oscillator (14MHz).

DSITXDIV[1:0]	DSICLK division ratio
2'b00	fDSICLK/4
2'b01	fDSICLK/8
2'b10	fDSICLK/16
2'b11	fDSICLK/32

DSITXDIV setting example

Status of Clock Lane	Host to R61529		R61529 to Host		
	Bit Rate [Mbps]	fDSICLK [MHz]	Setting of DSITXDIV [1:0]	fTXCLK [MHz]	Bit rate [Mbps]
Active	480	240	2'b10	15.0	7.50
	440	220		13.8	6.88
	400	200		12.5	6.25
	320	160	2'b01	20.0	10.0
	300	150		18.8	4.69
	200	100		12.5	6.25
	160	80	2'b00	20	10.0
	100	50		12.5	6.25
Inactive (Stop)	-	-	-	0.785 (fosc)	0.3925

<table>
<tr><td>Description</td><td>DSI_THSSET[1:0]
These bits are used to change operation frequency according to DSI clock when MIPI DSI is selected.
<table>
<tr><th rowspan="2">DSI_THSSET[1:0]</th><th colspan="2">Operating frequency (MHz)</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td>00</td><td>100</td><td>180</td></tr>
<tr><td>01</td><td>180</td><td>280</td></tr>
<tr><td>10</td><td>280</td><td>420</td></tr>
<tr><td>11</td><td>420</td><td>500</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

MDDI Control (B7h)

B7h	MDDI Control											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	0	1	1	0	1	1	1	B7h
1st parameter	W / R	1	x	0	0	0	0	0	0	CRCSTP	MDCRC	3Xh
2nd parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
3rd parameter	W / R	1	x	0	0	0	1	0	MDDI_ICONT_TX [2]	MDDI_ICONT_TX [1]	MDDI_ICONT_TX [0]	2Xh
4th parameter	W / R	1	x	0	0	1	0	0	0	0	1	23h

Description

MDCRC

When MDDI error detection mode is enabled, an output level of the DIN pin is set to “High” if an error is detected. For details, see “CRC Error Detection Mode Setting” in “MDDI (Mobile Display Digital Interface).”

MDCRC	CRC error detection mode
0	Halt
1	Enabled

CRCSTP

While CRCSTP is set to 1, detection is temporarily disabled. When the DIN pin returns to “Low” level, CRCSTP is set to 0. CRCSTP is also used as an error detection signal. For details, see “CRC Error Detection Mode Setting” in “MDDI (Mobile Display Digital Interface.”

MDDI_ICONT_TX[2:0]

They are used to adjust bias current for MDDI reverse link. They decide TX output differential signal level.

MDDI_ICONT_TX[2:0]	Theoretical value of differential output current from Reverse Transmitter.	
3’h0	50%（1.75mA）	
3’h 1	60%（2.10mA）	Center of values specified by MDDI standard (ver.1.2)
3’h 2	70%（2.45mA）	
3’h 3	80%（2.80mA）	
3’h 4	90%（3.15mA）	
3’h 5	100%（3.50mA）	Center of values specified by MDDI standard (ver.1.0)
3’h 6	110%（3.85mA）	
3’h 7	120%（4.20mA）	

Write 00h in the 2nd parameter. Write 23h in the 4th parameter.

Restriction

Backlight Control (1) (B8h)

B8h	Backlight Control (1)											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	0	1	1	1	0	0	0	B8h
1st parameter	W / R	1	x	0	0	0	0	0	0	BLCM	BLC ON	0Xh
2nd parameter	W / R	1	x	0	0	0	THREW0[4]	THREW0[3]	THREW0[2]	THREW0[1]	THREW0[0]	XXh
3rd parameter	W / R	1	x	0	0	0	THREW1[4]	THREW1[3]	THREW1[2]	THREW1[1]	THREW1[0]	XXh
4th parameter	W / R	1	x	ULMTW0[7]	ULMTW0[6]	ULMTW0[5]	ULMTW0[4]	ULMTW0[3]	ULMTW0[2]	ULMTW0[1]	ULMTW0[0]	XXh
5th parameter	W / R	1	x	ULMTW1[7]	ULMTW1[6]	ULMTW1[5]	ULMTW1[4]	ULMTW1[3]	ULMTW1[2]	ULMTW1[1]	ULMTW1[0]	XXh
6th parameter	W / R	1	x	LLMTW0[7]	LLMTW0[6]	LLMTW0[5]	LLMTW0[4]	LLMTW0[3]	LLMTW0[2]	LLMTW0[1]	LLMTW0[0]	XXh
7th parameter	W / R	1	x	LLMTW1[7]	LLMTW1[6]	LLMTW1[5]	LLMTW1[4]	LLMTW1[3]	LLMTW1[2]	LLMTW1[1]	LLMTW1[0]	XXh
8th parameter	W / R	1	x	0	0	0	0	PITCHW[3]	PITCHW[2]	PITCHW[1]	PITCHW[0]	0Xh
9th parameter	W / R	1	x	0	0	0	CGAPW [4]	CGAPW [3]	CGAPW [2]	CGAPW [1]	CGAPW [0]	XXh
10th parameter	W / R	1	x	LNCOM0	0	0	COEFK0[4]	COEFK0[3]	COEFK0[2]	COEFK0[1]	COEFK0[0]	XXh
11th parameter	W / R	1	x	LNCOM1	0	0	COEFK1[4]	COEFK1[3]	COEFK1[2]	COEFK1[1]	COEFK1[0]	XXh
12th parameter	W / R	1	x	TBL3[7]	TBL3[6]	TBL3[5]	TBL3[4]	TBL3[3]	TBL3[2]	TBL3[1]	TBL3[0]	XXh
13th parameter	W / R	1	x	TBL4[7]	TBL4[6]	TBL4[5]	TBL4[4]	TBL4[3]	TBL4[2]	TBL4[1]	TBL4[0]	XXh
14th parameter	W / R	1	x	TBL5[7]	TBL5[6]	TBL5[5]	TBL5[4]	TBL5[3]	TBL5[2]	TBL5[1]	TBL5[0]	XXh
15th parameter	W / R	1	x	TBL6[7]	TBL6[6]	TBL6[5]	TBL6[4]	TBL6[3]	TBL6[2]	TBL6[1]	TBL6[0]	XXh
16th parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h

Description

Note: Make sure that BLC function is turned off (DB0 (the 1st parameter): BLCON=0) when changing parameter values of B8h and switching BLC modes (DB1 (the 1st parameter: BLCM).

Write 00h in the 16th parameter.

BLCM

The bit is used to select BLC mode. There are two sets of bits for each of THREW, ULMTW, LLMTW, COEFK, and LNCOM registers, enabling different settings for different display images.

Before changing BLCM value, turn BLC function off (DB0 (the 1st parameter): BLCON=0).

BLCM	BLC mode	Enabled register						
0	Mode 0	THREW0	ULMTW0	LLMTW0	PITCHW	CGAPW	LNCOM0	COEFK0
1	Mode 1	THREW1	ULMTW1	LLMTW1			LNCOM1	COEFK1

BLCON

The bit is used to turn the BLC function ON/OFF.

BLCON	BLC function
0	OFF
1	ON

The BLC function is disabled in Display Invert Mode On. Use BLC function (BLCON = 1) in Normal Mode On and Display Invert Mode Off.

Description

THREW0[4:0], THREW1[4:0]

The bits are used to specify percentage from the threshold to grayscale number 63 in the total of grayscale data. This is the ratio (percentage) of the maximum number of pixels that makes display image white (= data “63”) to the total of pixels by image processing.

Percentage of pixels =

Number of pixels with the grayscale from the threshold to grayscale No. 63/ Number of all pixels

THREW0 is enabled when BLCM=0.

THREW1 is enabled when BLCM=1.

THREW0[4:0] THREW1[4:0]	Percentage of pixels
5’h00	0%
5’h01	2%
5’h02	4%
5’h03	6%
5’h04	8%
5’h05	10%
5’h06	12%
5’h07	14%
5’h08	16%
5’h09	18%
5’h0A	20%
5’h0B	22%
5’h0C	24%
5’h0D	26%
5’h0E	28%
5’h0F	30%

THREW0[4:0] THREW1[4:0]	Percentage of pixels
5’h10	32%
5’h11	34%
5’h12	36%
5’h13	38%
5’h14	40%
5’h15	42%
5’h16	44%
5’h17	46%
5’h18	48%
5’h19	50%
5’h1A	52%
5’h1B	54%
5’h1C	56%
5’h1D	58%
5’h1E	60%
5’h1F	62%

Description

ULMTW0[7:0], ULMTW1[7:0]

The possible maximum value of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale. ULMTW0 is enabled when BLCM=0. ULMTW1 is enabled when BLCM=1.

ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)
8'h00	0	8'h10	16	8'h20	32	8'h30	48
8'h01	1	8'h11	17	8'h21	33	8'h31	49
8'h02	2	8'h12	18	8'h22	34	8'h32	50
8'h03	3	8'h13	19	8'h23	35	8'h33	51
8'h04	4	8'h14	20	8'h24	36	8'h34	52
8'h05	5	8'h15	21	8'h25	37	8'h35	53
8'h06	6	8'h16	22	8'h26	38	8'h36	54
8'h07	7	8'h17	23	8'h27	39	8'h37	55
8'h08	8	8'h18	24	8'h28	40	8'h38	56
8'h09	9	8'h19	25	8'h29	41	8'h39	57
8'h0A	10	8'h1A	26	8'h2A	42	8'h3A	58
8'h0B	11	8'h1B	27	8'h2B	43	8'h3B	59
8'h0C	12	8'h1C	28	8'h2C	44	8'h3C	60
8'h0D	13	8'h1D	29	8'h2D	45	8'h3D	61
8'h0E	14	8'h1E	30	8'h2E	46	8'h3E	62
8'h0F	15	8'h1F	31	8'h2F	47	8'h3F	63

Description

ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)
8'h40	64	8'h50	80	8'h60	96	8'h70	112
8'h41	65	8'h51	81	8'h61	97	8'h71	113
8'h42	66	8'h52	82	8'h62	98	8'h72	114
8'h43	67	8'h53	83	8'h63	99	8'h73	115
8'h44	68	8'h54	84	8'h64	100	8'h74	116
8'h45	69	8'h55	85	8'h65	101	8'h75	117
8'h46	70	8'h56	86	8'h66	102	8'h76	118
8'h47	71	8'h57	87	8'h67	103	8'h77	119
8'h48	72	8'h58	88	8'h68	104	8'h78	120
8'h49	73	8'h59	89	8'h69	105	8'h79	121
8'h4A	74	8'h5A	90	8'h6A	106	8'h7A	122
8'h4B	75	8'h5B	91	8'h6B	107	8'h7B	123
8'h4C	76	8'h5C	92	8'h6C	108	8'h7C	124
8'h4D	77	8'h5D	93	8'h6D	109	8'h7D	125
8'h4E	78	8'h5E	94	8'h6E	110	8'h7E	126
8'h4F	79	8'h5F	95	8'h6F	111	8'h7F	127

Description

ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)
8'h80	128	8'h90	144	8'hA0	160	8'hB0	176
8'h81	129	8'h91	145	8'hA1	161	8'hB1	177
8'h82	130	8'h92	146	8'hA2	162	8'hB2	178
8'h83	131	8'h93	147	8'hA3	163	8'hB3	179
8'h84	132	8'h94	148	8'hA4	164	8'hB4	180
8'h85	133	8'h95	149	8'hA5	165	8'hB5	181
8'h86	134	8'h96	150	8'hA6	166	8'hB6	182
8'h87	135	8'h97	151	8'hA7	167	8'hB7	183
8'h88	136	8'h98	152	8'hA8	168	8'hB8	184
8'h89	137	8'h99	153	8'hA9	169	8'hB9	185
8'h8A	138	8'h9A	154	8'hAA	170	8'hBA	186
8'h8B	139	8'h9B	155	8'hAB	171	8'hBB	187
8'h8C	140	8'h9C	156	8'hAC	172	8'hBC	188
8'h8D	141	8'h9D	157	8'hAD	173	8'hBD	189
8'h8E	142	8'h9E	158	8'hAE	174	8'hBE	190
8'h8F	143	8'h9F	159	8'hAF	175	8'hBF	191

Description

ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)
8'hC0	192	8'hD0	208	8'hE0	224	8'hF0	240
8'hC1	193	8'hD1	209	8'hE1	225	8'hF1	241
8'hC2	194	8'hD2	210	8'hE2	226	8'hF2	242
8'hC3	195	8'hD3	211	8'hE3	227	8'hF3	243
8'hC4	196	8'hD4	212	8'hE4	228	8'hF4	244
8'hC5	197	8'hD5	213	8'hE5	229	8'hF5	245
8'hC6	198	8'hD6	214	8'hE6	230	8'hF6	246
8'hC7	199	8'hD7	215	8'hE7	231	8'hF7	247
8'hC8	200	8'hD8	216	8'hE8	232	8'hF8	248
8'hC9	201	8'hD9	217	8'hE9	233	8'hF9	249
8'hCA	202	8'hDA	218	8'hEA	234	8'hFA	250
8'hCB	203	8'hDB	219	8'hEB	235	8'hFB	251
8'hCC	204	8'hDC	220	8'hEC	236	8'hFC	252
8'hCD	205	8'hDD	221	8'hED	237	8'hFD	253
8'hCE	206	8'hDE	222	8'hEE	238	8'hFE	254
8'hCF	207	8'hDF	223	8'hEF	239	8'hFF	255

Description

LMTW0[7:0], LMTW1[7:0]

The possible minimum value of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale. LLMTW0 is enabled when BLCM=0. LLMTW1 is enabled when BLCM=1.

LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)
8'h00	0	8'h10	16	8'h20	32	8'h30	48
8'h01	1	8'h11	17	8'h21	33	8'h31	49
8'h02	2	8'h12	18	8'h22	34	8'h32	50
8'h03	3	8'h13	19	8'h23	35	8'h33	51
8'h04	4	8'h14	20	8'h24	36	8'h34	52
8'h05	5	8'h15	21	8'h25	37	8'h35	53
8'h06	6	8'h16	22	8'h26	38	8'h36	54
8'h07	7	8'h17	23	8'h27	39	8'h37	55
8'h08	8	8'h18	24	8'h28	40	8'h38	56
8'h09	9	8'h19	25	8'h29	41	8'h39	57
8'h0A	10	8'h1A	26	8'h2A	42	8'h3A	58
8'h0B	11	8'h1B	27	8'h2B	43	8'h3B	59
8'h0C	12	8'h1C	28	8'h2C	44	8'h3C	60
8'h0D	13	8'h1D	29	8'h2D	45	8'h3D	61
8'h0E	14	8'h1E	30	8'h2E	46	8'h3E	62
8'h0F	15	8'h1F	31	8'h2F	47	8'h3F	63

Description

LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)
8'h40	64	8'h50	80	8'h60	96	8'h70	112
8'h41	65	8'h51	81	8'h61	97	8'h71	113
8'h42	66	8'h52	82	8'h62	98	8'h72	114
8'h43	67	8'h53	83	8'h63	99	8'h73	115
8'h44	68	8'h54	84	8'h64	100	8'h74	116
8'h45	69	8'h55	85	8'h65	101	8'h75	117
8'h46	70	8'h56	86	8'h66	102	8'h76	118
8'h47	71	8'h57	87	8'h67	103	8'h77	119
8'h48	72	8'h58	88	8'h68	104	8'h78	120
8'h49	73	8'h59	89	8'h69	105	8'h79	121
8'h4A	74	8'h5A	90	8'h6A	106	8'h7A	122
8'h4B	75	8'h5B	91	8'h6B	107	8'h7B	123
8'h4C	76	8'h5C	92	8'h6C	108	8'h7C	124
8'h4D	77	8'h5D	93	8'h6D	109	8'h7D	125
8'h4E	78	8'h5E	94	8'h6E	110	8'h7E	126
8'h4F	79	8'h5F	95	8'h6F	111	8'h7F	127

Description

LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)
8'h80	128	8'h90	144	8'hA0	160	8'hB0	176
8'h81	129	8'h91	145	8'hA1	161	8'hB1	177
8'h82	130	8'h92	146	8'hA2	162	8'hB2	178
8'h83	131	8'h93	147	8'hA3	163	8'hB3	179
8'h84	132	8'h94	148	8'hA4	164	8'hB4	180
8'h85	133	8'h95	149	8'hA5	165	8'hB5	181
8'h86	134	8'h96	150	8'hA6	166	8'hB6	182
8'h87	135	8'h97	151	8'hA7	167	8'hB7	183
8'h88	136	8'h98	152	8'hA8	168	8'hB8	184
8'h89	137	8'h99	153	8'hA9	169	8'hB9	185
8'h8A	138	8'h9A	154	8'hAA	170	8'hBA	186
8'h8B	139	8'h9B	155	8'hAB	171	8'hBB	187
8'h8C	140	8'h9C	156	8'hAC	172	8'hBC	188
8'h8D	141	8'h9D	157	8'hAD	173	8'hBD	189
8'h8E	142	8'h9E	158	8'hAE	174	8'hBE	90
8'h8F	143	8'h9F	159	8'hAF	175	8'hBF	191

Description

LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)
8'hC0	192	8'hD0	208	8'hE0	224	8'hF0	240
8'hC1	193	8'hD1	209	8'hE1	225	8'hF1	241
8'hC2	194	8'hD2	210	8'hE2	226	8'hF2	242
8'hC3	195	8'hD3	211	8'hE3	227	8'hF3	243
8'hC4	196	8'hD4	212	8'hE4	228	8'hF4	244
8'hC5	197	8'hD5	213	8'hE5	229	8'hF5	245
8'hC6	198	8'hD6	214	8'hE6	230	8'hF6	246
8'hC7	199	8'hD7	215	8'hE7	231	8'hF7	247
8'hC8	200	8'hD8	216	8'hE8	232	8'hF8	248
8'hC9	201	8'hD9	217	8'hE9	233	8'hF9	249
8'hCA	202	8'hDA	218	8'hEA	234	8'hFA	250
8'hCB	203	8'hDB	219	8'hEB	235	8'hFB	251
8'hCC	204	8'hDC	220	8'hEC	236	8'hFC	252
8'hCD	205	8'hDD	221	8'hED	237	8'hFD	253
8'hCE	206	8'hDE	222	8'hEE	238	8'hFE	254
8'hCF	207	8'hDF	223	8'hEF	239	8'hFF	255

Note: LLMTW0[7:0] and LLMTW1[7:0] values are restricted as above table according to COEFK0[4:0] and COEFK1[4:0] values. Make sure to follow the above minimum LLMTW*[5:0] setting to each COEFK[4:0] value.

Description

PITCHW0[3:0], PITCHW1[3:0]

This parameter sets the amount of change of threshold grayscale value (Dth) that makes display image white per frame in units of one half of the grayscale.

PITCHW[3:0]	Amount of change (grayscale)
4'h0	Setting inhibited
4'h1	1/2 grayscale
4'h2	1 grayscale
4'h3	3/2 grayscales
4'h4	2 grayscales
4'h5	5/2 grayscales
4'h6	3 grayscales
4'h7	7/2 grayscales
4'h8	4 grayscales
4'h9	9/2 grayscales
4'hA	5 grayscales
4'hB	11/2 grayscales
4'hC	6 grayscales
4'hD	13/2 grayscales
4'hE	7 grayscales
4'hF	15/2 grayscales

LNCOM0, LNCOM1

LNCOM0, LNCOM1: Used to select 2- or 4-point interpolation when BLC function is used. When BLCM is set to 0, LNCOM0 is enabled. When BLCM is set to 1, LNCOM1 is enabled.

BLCM=0

LNCOM0	Interpolation
0	4-point interpolation
1	2-point interpolation

BLCM=1

LNCOM1	Interpolation
0	4-point interpolation
1	2-point interpolation

Description

CGAPW0[4:0], CGAPW1[4:0]

The difference of the two grayscales counted by the threshold counter is set in units of one half of the grayscale.

CGAPW[4:0]	Grayscale difference
5'h00	Setting inhibited
5'h01	1/2 grayscale
5'h02	1 grayscale
5'h03	3/2 grayscale
5'h04	2 grayscales
5'h05	5/2 grayscales
5'h06	3 grayscales
5'h07	7/2 grayscales
5'h08	4 grayscales
5'h09	9/2 grayscales
5'h0A	5 grayscales
5'h0B	11/2 grayscales
5'h0C	6 grayscales
5'h0D	13/2 grayscales
5'h0E	7 grayscales
5'h0F	15/2 grayscales

CGAPW[4:0]	Grayscale difference
5'h10	2 grayscales
5'h11	17/2 grayscales
5'h12	9 grayscales
5'h13	19/2 grayscales
5'h14	10 grayscales
5'h15	21/2 grayscales
5'h16	11 grayscales
5'h17	23/2 grayscales
5'h18	12 grayscales
5'h19	25/2 grayscales
5'h1A	13 grayscales
5'h1B	27/2 grayscales
5'h1C	14 grayscales
5'h1D	29/2 grayscales
5'h1E	15 grayscales
5'h1F	31/2 grayscales

Description

COEFK0[4:0] , COEFK1[4:0]

This register sets the range of the grayscale that prevents display image from being white, according to the ratio of the grayscale mentioned here to the grayscale number that makes data white.

COEFK0[4:0] COEFK1[4:0]	Range of grayscale preventing image from being white	COEFK0[4:0] COEFK1[4:0]	Range of grayscale preventing image from being white
5'h00	0%	5'h10	100.00%
5'h01	6.25%	5'h11	Setting inhibited
5'h02	12.50%	5'h12	Setting inhibited
5'h03	18.75%	5'h13	Setting inhibited
5'h04	25.00%	5'h14	Setting inhibited
5'h05	31.25%	5'h15	Setting inhibited
5'h06	37.50%	5'h16	Setting inhibited
5'h07	43.75%	5'h17	Setting inhibited
5'h08	50.00%	5'h18	Setting inhibited
5'h09	56.25%	5'h19	Setting inhibited
5'h0A	62.50%	5'h1A	Setting inhibited
5'h0B	68.75%	5'h1B	Setting inhibited
5'h0C	75.00%	5'h1C	Setting inhibited
5'h0D	81.25%	5'h1D	Setting inhibited
5'h0E	87.50%	5'h1E	Setting inhibited
5'h0F	93.75%	5'h1F	Setting inhibited

Description

TBL_MIN[7:0], TBL3[7:0], TBL4[7:0], TBL5[7:0], TBL6[7:0]

The reference value used for interpolation calculation in gamma table are set by TBL_*.

TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value
8'h00	8'h00	8'h20	8'h20	8'h40	8'h40	8'h60	8'h60
8'h01	8'h01	8'h21	8'h21	8'h41	8'h41	8'h61	8'h61
8'h02	8'h02	8'h22	8'h22	8'h42	8'h42	8'h62	8'h62
8'h03	8'h03	8'h23	8'h23	8'h43	8'h43	8'h63	8'h63
8'h04	8'h04	8'h24	8'h24	8'h44	8'h44	8'h64	8'h64
8'h05	8'h05	8'h25	8'h25	8'h45	8'h45	8'h65	8'h65
8'h06	8'h06	8'h26	8'h26	8'h46	8'h46	8'h66	8'h66
8'h07	8'h07	8'h27	8'h27	8'h47	8'h47	8'h67	8'h67
8'h08	8'h08	8'h28	8'h28	8'h48	8'h48	8'h68	8'h68
8'h09	8'h09	8'h29	8'h29	8'h49	8'h49	8'h69	8'h69
8'h0A	8'h0A	8'h2A	8'h2A	8'h4A	8'h4A	8'h6A	8'h6A
8'h0B	8'h0B	8'h2B	8'h2B	8'h4B	8'h4B	8'h6B	8'h6B
8'h0C	8'h0C	8'h2C	8'h2C	8'h4C	8'h4C	8'h6C	8'h6C
8'h0D	8'h0D	8'h2D	8'h2D	8'h4D	8'h4D	8'h6D	8'h6D
8'h0E	8'h0E	8'h2E	8'h2E	8'h4E	8'h4E	8'h6E	8'h6E
8'h0F	8'h0F	8'h2F	8'h2F	8'h4F	8'h4F	8'h6F	8'h6F
8'h10	8'h10	8'h30	8'h30	8'h50	8'h50	8'h70	8'h70
8'h11	8'h11	8'h31	8'h31	8'h51	8'h51	8'h71	8'h71
8'h12	8'h12	8'h32	8'h32	8'h52	8'h52	8'h72	8'h72
8'h13	8'h13	8'h33	8'h33	8'h53	8'h53	8'h73	8'h73
8'h14	8'h14	8'h34	8'h34	8'h54	8'h54	8'h74	8'h74
8'h15	8'h15	8'h35	8'h35	8'h55	8'h55	8'h75	8'h75
8'h16	8'h16	8'h36	8'h36	8'h56	8'h56	8'h76	8'h76
8'h17	8'h17	8'h37	8'h37	8'h57	8'h57	8'h77	8'h77
8'h18	8'h18	8'h38	8'h38	8'h58	8'h58	8'h78	8'h78
8'h19	8'h19	8'h39	8'h39	8'h59	8'h59	8'h79	8'h79
8'h1A	8'h1A	8'h3A	8'h3A	8'h5A	8'h5A	8'h7A	8'h7A
8'h1B	8'h1B	8'h3B	8'h3B	8'h5B	8'h5B	8'h7B	8'h7B
8'h1C	8'h1C	8'h3C	8'h3C	8'h5C	8'h5C	8'h7C	8'h7C
8'h1D	8'h1D	8'h3D	8'h3D	8'h5D	8'h5D	8'h7D	8'h7D
8'h1E	8'h1E	8'h3E	8'h3E	8'h5E	8'h5E	8'h7E	8'h7E
8'h1F	8'h1F	8'h3F	8'h3F	8'h5F	8'h5F	8'h7F	8'h7F

Description

TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value
8'h80	8'h80	8'hA0	8'hA0	8'hC0	8'hC0	8'hE0	8'hE0
8'h81	8'h81	8'hA1	8'hA1	8'hC1	8'hC1	8'hE1	8'hE1
8'h82	8'h82	8'hA2	8'hA2	8'hC2	8'hC2	8'hE2	8'hE2
8'h83	8'h83	8'hA3	8'hA3	8'hC3	8'hC3	8'hE3	8'hE3
8'h84	8'h84	8'hA4	8'hA4	8'hC4	8'hC4	8'hE4	8'hE4
8'h85	8'h85	8'hA5	8'hA5	8'hC5	8'hC5	8'hE5	8'hE5
8'h86	8'h86	8'hA6	8'hA6	8'hC6	8'hC6	8'hE6	8'hE6
8'h87	8'h87	8'hA7	8'hA7	8'hC7	8'hC7	8'hE7	8'hE7
8'h88	8'h88	8'hA8	8'hA8	8'hC8	8'hC8	8'hE8	8'hE8
8'h89	8'h89	8'hA9	8'hA9	8'hC9	8'hC9	8'hE9	8'hE9
8'h8A	8'h8A	8'hAA	8'hAA	8'hCA	8'hCA	8'hEA	8'hEA
8'h8B	8'h8B	8'hAB	8'hAB	8'hCB	8'hCB	8'hEB	8'hEB
8'h8C	8'h8C	8'hAC	8'hAC	8'hCC	8'hCC	8'hEC	8'hEC
8'h8D	8'h8D	8'hAD	8'hAD	8'hCD	8'hCD	8'hED	8'hED
8'h8E	8'h8E	8'hAE	8'hAE	8'hCE	8'hCE	8'hEE	8'hEE
8'h8F	8'h8F	8'hAF	8'hAF	8'hCF	8'hCF	8'hEF	8'hEF
8'h90	8'h90	8'hB0	8'hB0	8'hD0	8'hD0	8'hF0	8'hF0
8'h91	8'h91	8'hB1	8'hB1	8'hD1	8'hD1	8'hF1	8'hF1
8'h92	8'h92	8'hB2	8'hB2	8'hD2	8'hD2	8'hF2	8'hF2
8'h93	8'h93	8'hB3	8'hB3	8'hD3	8'hD3	8'hF3	8'hF3
8'h94	8'h94	8'hB4	8'hB4	8'hD4	8'hD4	8'hF4	8'hF4
8'h95	8'h95	8'hB5	8'hB5	8'hD5	8'hD5	8'hF5	8'hF5
8'h96	8'h96	8'hB6	8'hB6	8'hD6	8'hD6	8'hF6	8'hF6
8'h97	8'h97	8'hB7	8'hB7	8'hD7	8'hD7	8'hF7	8'hF7
8'h98	8'h98	8'hB8	8'hB8	8'hD8	8'hD8	8'hF8	8'hF8
8'h99	8'h99	8'hB9	8'hB9	8'hD9	8'hD9	8'hF9	8'hF9
8'h9A	8'h9A	8'hBA	8'hBA	8'hDA	8'hDA	8'hFA	8'hFA
8'h9B	8'h9B	8'hBB	8'hBB	8'hDB	8'hDB	8'hFB	8'hFB
8'h9C	8'h9C	8'hBC	8'hBC	8'hDC	8'hDC	8'hFC	8'hFC
8'h9D	8'h9D	8'hBD	8'hBD	8'hDD	8'hDD	8'hFD	8'hFD
8'h9E	8'h9E	8'hBE	8'hBE	8'hDE	8'hDE	8'hFE	8'hFE
8'h9F	8'h9F	8'hBF	8'hBF	8'hDF	8'hDF	8'hFF	8'hFF

Backlight Control (2) (B9h)

B9h	Backlight Control (2)											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	x	1	0	1	1	1	0	0	1	B9h
1st parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
2nd parameter	W / R	1	x	BDCV [7]	BDCV [6]	BDCV [5]	BDCV [4]	BDCV [3]	BDCV [2]	BDCV [1]	BDCV [0]	00h
3rd parameter	W / R	1	x	PWMDIV [7]	PWMDIV [6]	PWMDIV [5]	PWMDIV [4]	PWMDIV [3]	PWMDIV [2]	PWMDIV [1]	PWMDIV [0]	00h
4th parameter	W / R	1	x	0	0	0	PWMWM	LEDPWME	0	0	0	00h

Description

PWMWM

PWMWM = 0: Controls On/Off of the PWM output according to Display On/Off state.
PWMWM = 1: Controls On/Off of the PWM output according to PWMON setting. Note that LEDPWM is OFF when in Sleep Mode regardless of PWMON value.
PWMWM setting can be changed only in Sleep Mode On.

LEDPWME

LEDPWME pin output enable bit. In the system configuration using no LEDPWM pin, set the bit to 0. In the system configuration using LEDPWM pin, set the bit to 1. This setting can be changed only in Sleep Mode On.

LEDPWME	PWMWM	PWMON	BLCON	RDPWM	LEDPWM output	Note
0	0	*	0	BDCV	0%	
			1	BLC*BDCV	0%	
	1	0	0	0%	0%	
			1	Setting inhibited	Setting inhibited	
		1	0	BDCV	0%	
			1	BLC*BDCV	0%	*2
1	0	*	0	BDCV	BDCV	*1
			1	BLC*BDCV	BLC*BDCV	*1
	1	0	0	0%	0%	
			1	Setting inhibited	Setting inhibited	
		1	0	BDCV	BDCV	
			1	BLC*BDCV	BLC*BDCV	*2

Notes: 1. If PWMWM = 0, On/Off of the PWM output is automatically controlled according to display ON/Off state.
Display Off: Sleep Mode On + set_display_off
Display On: sleep Mode Off + set_display_on

2. If PWMWM = 1, RDPWM and LEDPWM outputs cause BDCV value to be read during Display Off.

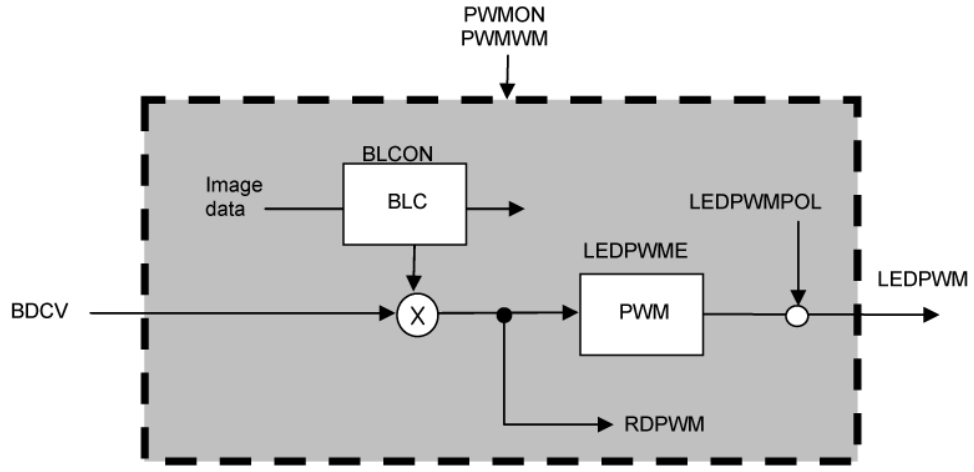
Description	**BDCV[7:0]** PWM signal's width is selected from 256 values between 8'hFF and 8'h00 when LED is adjusted externally. BLCON=0: PWM signal whose width is determined by BDCV[7:0] is output. BLCON=1: PWM signal whose width is determined by (BDCV*BLC).

BDCV[7:0]	Amount of light
8'h00	None (0%)
8'h01	1/255
8'h02	2/255
8'h03	3/255
:	:
8'hFE	254/255
8'hFF	255/255 (100%)

PWMDIV, LEDPWM, DIMON

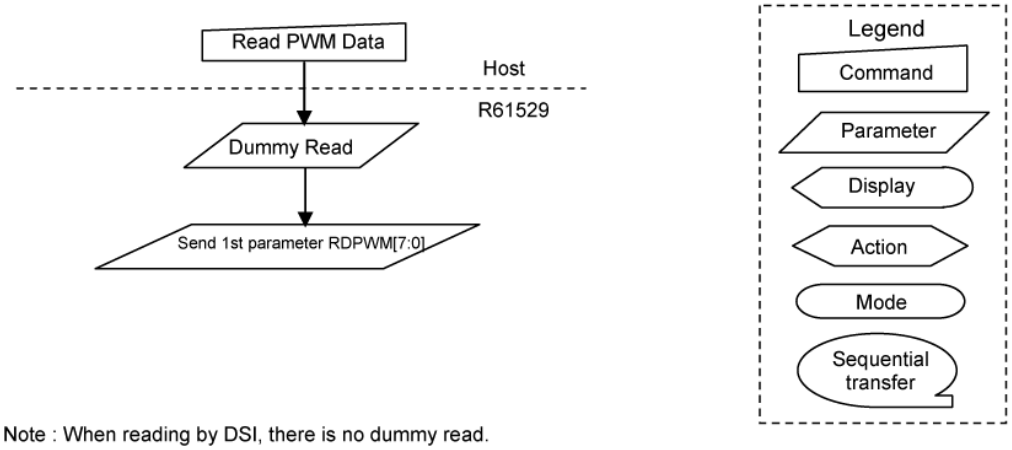
T.B.D.

Back light control Block diagram

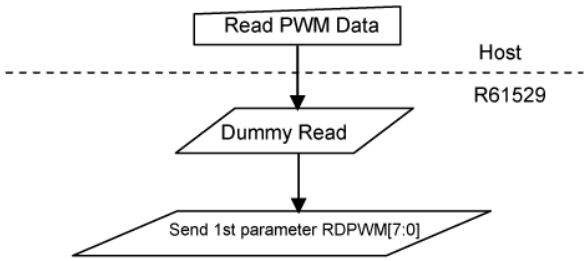
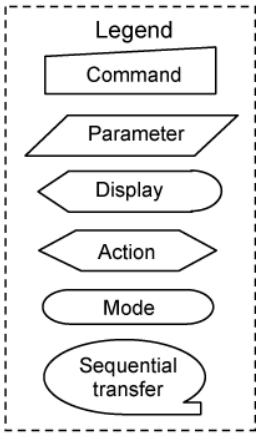


Restriction	

Backlight Control (3) (BAh)

BAh	Backlight Control (3) (Read PWM Data)											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	0	1	1	1	0	1	0	BAh
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	x	RDPWM[7]	RDPWM[6]	RDPWM[5]	RDPWM[4]	RDPWM[3]	RDPWM[2]	RDPWM[1]	RDPWM[0]	00h
Description	**RDPWM[7:0]** The command is used to read LED brightness data for LEDPWM signal. X = Don't care											
Restriction	Read data is invalid in Sleep Mode On.											
Flow Chart	 Note : When reading by DSI, there is no dummy read.											

Device Code Read (BFh)

BFh	Device Code Read											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	X	1	0	1	1	1	1	1	1	BFh
Dummy parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	0	0	0	0	0	0	0	1	01h
2nd parameter	R	1	X	0	0	1	0	0	0	1	0	22h
3rd parameter	R	1	X	0	0	0	1	0	1	0	0	14h
4th parameter	R	1	X	0	0	0	0	1	0	0	0	08h
5th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
Description	The parameters are used to read the information as follows. 1st parameter: Returns the upper byte "01h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 2nd parameter: Returns the lower byte "22h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 3rd parameter: Returns the upper byte "15h" of product code of this LSI. 4th parameter: Returns the lower byte "29h" of product code of this LSI. X = Don't care											
Restriction												
Flow Chart	  Note : When reading by DSI, there is no dummy read.										

Panel Control Command

Panel Driving Setting (C0h)

C0h	Panel Driving Setting											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	x	1	1	0	0	0	0	0	0	C0h
1st parameter	W / R	1	x	0	0	0	REV	SM	GS	BGR	SS	0Xh
2nd parameter	W / R	1	x	0	0	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	XXh
3rd parameter	W / R	1	x	0	0	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	XXh
4th parameter	W / R	1	x	0	0	0	0	0	0	BLV	PTV	XXh
5th parameter	W / R	1	x	0	0	0	NDL	PTDC	0	0	0	XXh
6th parameter	W / R	1	x	0	0	0	PTG	ISC[3]	ISC[2]	ISC[1]	ISC[0]	XXh
7th parameter	W / R	1	x	0	0	0	0	BLS	0	0	0	XXh
8th parameter	W / R	1	x	PCDIV H[3]	PCDIV H[2]	PCDIV H[1]	PCDIV H[0]	PCDIV L[3]	PCDIV L[2]	PCDIV L[1]	PCDIV L[0]	XXh

Description

REV

Source output level in display period.

REV	Input Data	Source output level in display area	
		Positive polarity	Positive polarity
0	24'h000000	V255	V255
	:	:	:
	24'hFFFFFF	V0	V0
1	24'h000000	V0	V0
	:	:	:
	24'hFFFFFF	V255	V255

SM

SM=0: Left/right interchanging scan
SM=1: Left/right one-side scan

GS

GS=0: Forward scan
GS=1: Reverse scan

The R61529 allows changing gate driver assignment and the scan mode by combination of SM and GS bits. Set these bits in accordance with the configuration of the module. For details, see "Scan Mode Setting".

BGR

The bit is used to switch RGB/BGR. (See "Command 36h; B3-bit) The relationship between BGR setting and gamma correction registers are shown below.

36h(B3)	BGR	Host processor	Display Device	Gamma correction registers
0	0	RGB	RGB	R: Gamma correction register C G: Gamma correction register B B: Gamma correction register A
	1	RGB	BGR	R: Gamma correction register A G: Gamma correction register B B: Gamma correction register C
1	0	RGB	BGR	R: Gamma correction register A G: Gamma correction register B B: Gamma correction register C
	1	RGB	RGB	R: Gamma correction register C G: Gamma correction register B B: Gamma correction register A

SS

The bit is used to select the shifting direction of the source driver output.

36h(B6)	SS	Source Output
0	0	S1 → S960
	1	S960 → S1

36h(B6)	SS	Source Output
1	0	S960 → S1
	1	S1 → S960

To change the RGB order, set SS and BGR bit in accordance with mounting position. The setting is enabled when it is written to the frame memory.

Description

NL[5:0]

These bits set the number of lines to drive the LCD to in units of 8 lines in the range from 400 to 480 lines. The frame memory address mapping is not affected by the number of NL[5:0]. The number of lines should be set according to the panel size.

NL[5:0]	Number of drive line
6'h00-6'h30	Setting inhibited
6'h31	400 lines
6'h32	408 lines
6'h33	416 lines
6'h34	424 lines
6'h35	432 lines
6'h36	440 lines
6'h37	448 lines
6'h38	456 lines
6'h39	464 lines
6'h3A	472 lines
6'h3B	480 lines
6'h3C-6'h3F	Setting inhibited

SCN[5:0]

The bit is used to set scanning start position.

SCN[5:0]	Scanning start position (N: Number of line(s) defined by NL[5:0])			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6'h00	G[1]	G[(N)]	G[1]	G[(2N－480)]
6'h01	G[9]	G[(N+8)]	G[16]	G[(2N－464)]
6'h02	G[17]	G[(N+16)]	G[33]	G[(2N－448)]
6'h03	G[25]	G[(N+24)]	G[49]	G[(2N－432)]
6'h04	G[33]	G[(N+32)]	G[65]	G[(2N－416)]
6'h05	G[41]	G[(N+40)]	G[81]	G[(2N－400)]
6'h06	G[49]	G[(N+48)]	G[97]	G[(2N－384)]
6'h07	G[57]	G[(N+56)]	G[113]	G[(2N－368)]
6'h08	G[65]	G[(N+64)]	G[129]	G[(2N－352)]
6'h09	G[73]	G[(N+72)]	G[145]	G[(2N－336)]
6'h0A	G[81]	G[(N+80)]	G[161]	G[(2N－320)]
6'h0B-6'h2F	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited

Description

To set SCN, follow the restriction below:

SM	GS	Restriction
0	0	(Scanning start position -1) + (Number of line (NL bit)) ≤ 480
0	1	Scanning start position ≤ 480
1	0	(Scanning start position -1)/2 + (Number of line (NL bit)) ≤ 480
1	1	Scanning start position ≤ 480

BLV

The bit selects line or frame inversion during the retrace period.

BLV	Inverting operation during retrace period
0	Not Inverting
1	Inverting

BLS

The bit is used to define source output level in the Retrace Period.

BLS	Positive polarity	Negative polarity
0	V255	V0
1	V0	V255

PTV

The bit is used to define inversion in the non-lit display area.

PTV	Inverting operation in non-lit display area
0	Not inverting
1	Inverting

NDL

The bit is used to define source output level (PTV=1) in the non-lit display area.

NDL	Source output level in the non-lit display area	
	Positive polarity	Negative polarity
2'h0	V255	V255
2'h1	V0	V0
2'h2	GND	GND
2'h3	Setting inhibited	

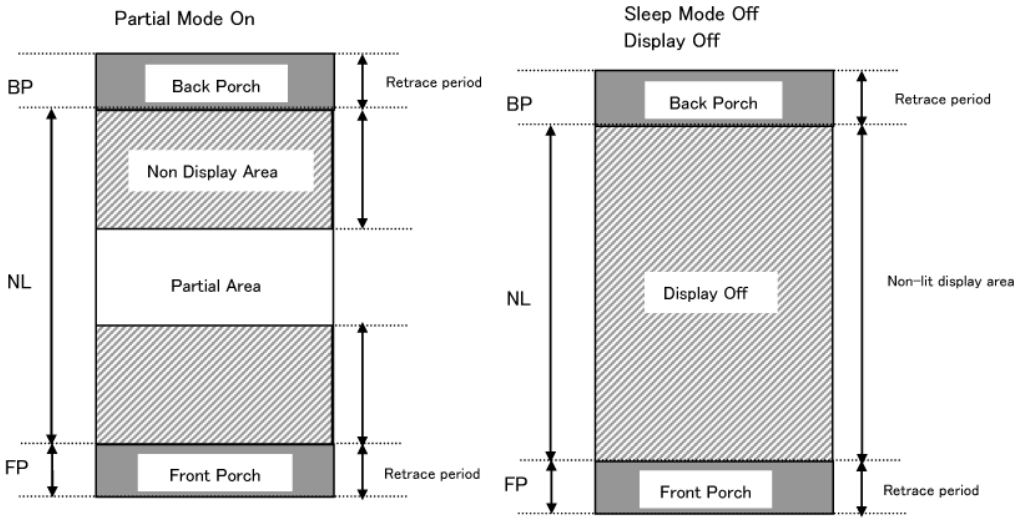
Description

PTDC

The bit is used to define low power consumption operation and to set step-up clock frequency (D0n) in non-lit display area.
For details, see "Step-up clock frequency (D0n) register descriptions. “Retrace period” means back and front porches.

“Non-lit display area” means:

Non-display area other than the Partial Area defined by SR[8:0] and ER[8:0].
Display area when Sleep mode is off and the display operation is off.



PTG

The bit is used to select gate scan mode in non-lit display area.

PTG	gate output in non-lit display area
0	Normal scan
1	Interval scan

Note: Selects the frame-n inversion liquid crystal drive waveform (B/C = 0) when selecting interval scan.

Description

ISC[3:0]

The bit is used to set gate interval scan when PTG bit sets interval scan in non-lit display area. The scan interval is always of odd number. The polarity of liquid crystal drive waveform is inverted in the same timing as the interval scan.

ISC[3:0]	Scan interval	ISC[3:0]	Scan interval
4'h0	Setting inhibited	4'h8	17 frames
4'h1	3 frames	4'h9	19 frames
4'h2	5 frames	4'hA	21 frames
4'h3	7 frames	4'hB	23 frames
4'h4	9 frames	4'hC	25 frames
4'h5	11 frames	4'hD	27 frames
4'h6	13 frames	4'hE	29 frames
4'h7	15 frames	4'hF	31 frames

PCDIVH[3:0]/PCDIVL[3:0]

When the R61529's display operation is synchronized with PCLK (DM=1, DPI), internal clock for display operation switches from internal oscillation clock to PCLKD. The bits are used to define the division ratio of PCLKD to PCLK.

PCDIVH defines the number of PCLK in PCLKD=High period in units of 1 clock.
PCDIVL defines the number of PCLK in PCLKD=Low period in units of 1 clock.

PCDIVH[3:0] PCDIVL[3:0]	Number of clocks	PCDIVH[3:0] PCDIVL[3:0]	Number of clocks
4'h0	Setting inhibited	4'h8	8 clocks
4'h1	1 clock	4'h9	9 clocks
4'h2	2 clocks	4'hA	10 clocks
4'h3	3 clocks	4'hB	11 clocks
4'h4	4 clocks	4'hC	12 clocks
4'h5	5 clocks	4'hD	13 clocks
4'h6	6 clocks	4'hE	14 clocks
4'h7	7 clocks	4'hF	15 clocks

Set PCDIVL=PCDIVH or PCDIVH-1.

Also, set PCDIVH and PCDIVL so that PCLKD frequency becomes the closest to internal oscillation clock frequency.

Display Timing Setting for Normal Mode (C1h)
Display Timing Setting for Partial Mode (C2h)
Display Timing Setting for Idle Mode (C3h)

C1h	Display Timing Setting for Normal Mode											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	0	0	0	0	1	C1h
1st parameter	W / R	1	x	0	0	0	0	DIV0 [3]	DIV0[2]	DIV0[1]	DIV0[0]	0Xh
2nd parameter	W / R	1	x	0	DPI_OFF	RTN0 [5]	RTN0 [4]	RTN0 [3]	RTN0 [2]	RTN0 [1]	RTN0 [0]	XXh
3rd parameter	W / R	1	x	BP0 [7]	BP0 [6]	BP0 [5]	BP0 [4]	BP0 [3]	BP0 [2]	BP0 [1]	BP0 [0]	XXh
4th parameter	W / R	1	x	FP0 [7]	FP0 [6]	FP0 [5]	FP0 [4]	FP0 [3]	FP0 [2]	FP0 [1]	FP0 [0]	XXh
5th parameter	W / R	1	x	0	LINEIN V0[2]	LINEIN V0[1]	LINEIN V0[0]	0	PNSET 0 [2]	PNSET 0 [1]	PNSET 0[0]	XXh
C2h	**Display Timing Setting for Partial Mode**											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	0	0	0	1	0	C2h
1st parameter	W / R	1	x	0	0	0	0	DIV1 [3]	DIV1 [2]	DIV1 [1]	DIV1 [0]	0Xh
2nd parameter	W / R	1	x	0	0	RTN1 [5]	RTN1 [4]	RTN1 [3]	RTN1 [2]	RTN1 [1]	RTN1 [0]	XXh
3rd parameter	W / R	1	x	BP1 [7]	BP1 [6]	BP1 [5]	BP1 [4]	BP1 [3]	BP1 [2]	BP1 [1]	BP1 [0]	XXh
4th parameter	W / R	1	x	FP1 [7]	FP1 [6]	FP1 [5]	FP1 [4]	FP1 [3]	FP1 [2]	FP1 [1]	FP1 [0]	XXh
C3h	**Display Timing Setting for Idle Mode**											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	0	0	0	1	1	C3h
1st parameter	W / R	1	x	0	0	0	0	DIV2 [3]	DIV2 [2]	DIV2 [1]	DIV2 [0]	0Xh
2nd parameter	W / R	1	x	0	0	RTN2 [5]	RTN2 [4]	RTN2 [3]	RTN2 [2]	RTN2 [1]	RTN2 [0]	XXh
3rd parameter	W / R	1	x	BP2 [7]	BP2 [6]	BP2 [5]	BP2 [4]	BP2 [3]	BP2 [2]	BP2 [1]	BP2 [0]	XXh
4th parameter	W / R	1	x	FP2 [7]	FP2 [6]	FP2 [5]	FP2 [4]	FP2 [3]	FP2 [2]	FP2 [1]	FP2 [0]	XXh

Description

These commands (C1h, C2h, C3h) can be defined separately for different modes.

Display mode	division ratio of clock (DIV)	number of clocks in 1H period (RTN)	Back porch (BP)	Front porch (FP)
Normal + Idle mode off	C1h:DIV0	C1h:RTN0	C1h:BP0	C1h:FP0
Partial mode + Idle mode off	C2h:DIV1	C2h:RTN1	C2h:BP1	C2h:FP1
Idle mode on + (Normal / Partial mode off)	C3h:DIV2	C3h:RTN2	C3h:BP2	C3h:FP2

DIVn[3:0]

These bits set the division ratio of the internal clock frequency. A clock whose frequency is divided is a reference clock (unit: clk) for a display circuit and step-up circuit. One clock width equals 1 clk. Set DIVn[3:0] before use according to use conditions. fOSC=14MHz(Typ.). If a division ratio is set to 1/7 (3'h2), 1/ (14MHz/ 7)= 0.5 μ s= 1clk . If a division ratio is set to 1/9 (3'h4), 1/(14MHz/ 9) ≒ 0.643μs= 1 clk.

DIVI[3:0]	Setting
3'h0	Setting inhibited
3'h1	Setting inhibited
3'h2	fOSC/7
3'h3	Setting inhibited
3'h4	fOSC/9
3'h5	fOSC/10
3'h6	Setting inhibited
3'h7	fOSC/12
Other than the above	Setting inhibited

DPI_OFF

Use DPI_OFF for transition from DPI Display Operation to Internal Clock Operation when using the DPI interface. For details, see "Internal Clock Operation (Transition Sequence DPI Display Operation)."

RTNn[4:0]

These bits set the number of clocks in 1 line period.

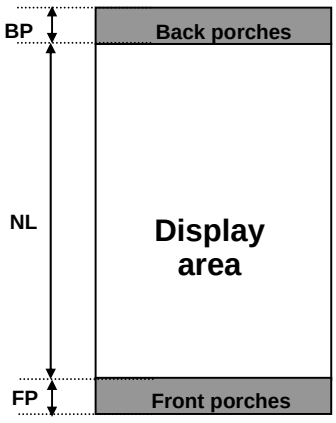
RTNn[4:0]	Clocks per line	RTNn[4:0]	Clocks per line	RTNn[4:0]	Clocks per line
5'h00-5'h1F	Setting inhibited	5'h25	37 clocks	5'h2B	43 clocks
5'h20	32 clocks	5'h26	38 clocks	5'h2C	44 clocks
5'h21	33 clocks	5'h27	39 clocks	5'h2D	45 clocks
5'h22	34 clocks	5'h28	40 clocks	5'h2E	46 clocks
5'h23	35 clocks	5'h29	41 clocks	5'h2F	47 clocks
5'h24	36 clocks	5'h2A	42 clocks		

Description

FPn[7:0], BPn[7:0]

These parameters define the retrace period (i.e. front and back porches) which appears before and after the display area. DPn bits define number of front porch lines while BPn bits define number of back porch lines.

FPn[7:0], BPn[7:0]	Number of front porch lines	Number of back porch lines
8'h00	Setting inhibited	Setting inhibited
8'h01	Setting inhibited	Setting inhibited
8'h02	Setting inhibited	Setting inhibited
8'h03	Setting inhibited	Setting inhibited
8'h04	4 lines	4 lines
8'h05	5 lines	5 lines
8'h06	6 lines	6 lines
8'h07	7 lines	7 lines
8'h08	8 lines	8 lines
8'h09	9 lines	9 lines
8'h0A	10 lines	10 lines
8'h0B	11 lines	11 lines
8'h0C	12 lines	12 lines
8'h0D	13 lines	13 lines
8'h0E	14 lines	14 lines
8'h0F	15 lines	15 lines
:	:	:
8'h7F	127 lines	127 lines
8'h80	128 lines	128 lines
8'h81	Setting inhibited	Setting inhibited
:	:	:
8'hFF	Setting inhibited	Setting inhibited



Description

PNSET0[1:0]

Dot inversion method setting

PNSET0[1:0]	Setting
2'h0	Spatial configuration mode 1
2'h1	Spatial configuration mode 2
2'h2	Setting inhibited
2'h3	Setting inhibited

LINEINV0[2:0]

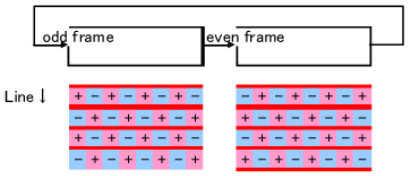
Line inversion frequency setting for the dot inversion method

LINEINV0[2:0]	Setting	
3'h0	1-line inversion	Spatial configuration mode 1 only
3'h1	2-line inversion	
3'h2	3-line inversion	
3'h3	4-line inversion	
3'h4	8-line inversion	
3'h5	column inversion	Spatial configuration mode 1 only
2'h6	Setting inhibited	
3'h7	Setting inhibited	

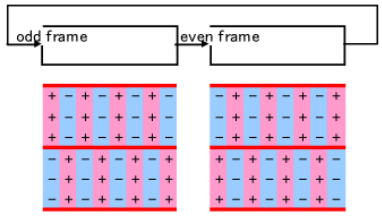
Restriction	Make sure that the total of lines set by the BP and FP bits is an even number.

Description	Souce output operation by combination of PNSET0 and LINEINV0 is as below.

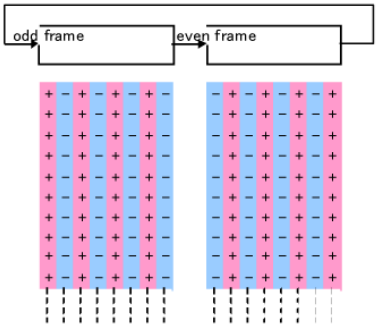
● 1-line inversion Spatial configuration mode 1 only



● 3-line inversion Spatial configuration mode 1 only

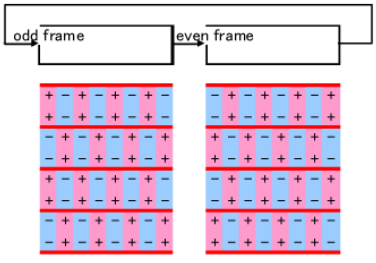


● colum inversion Spatial configuration mode 1 only

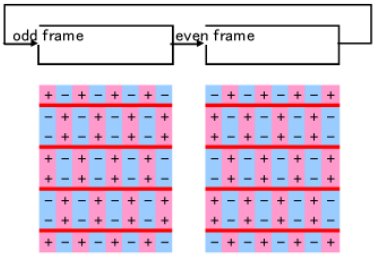


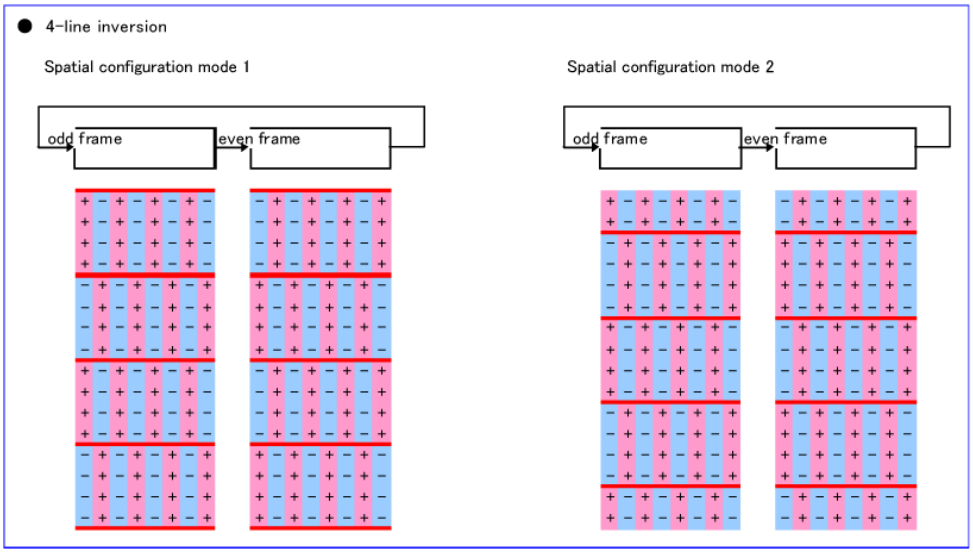
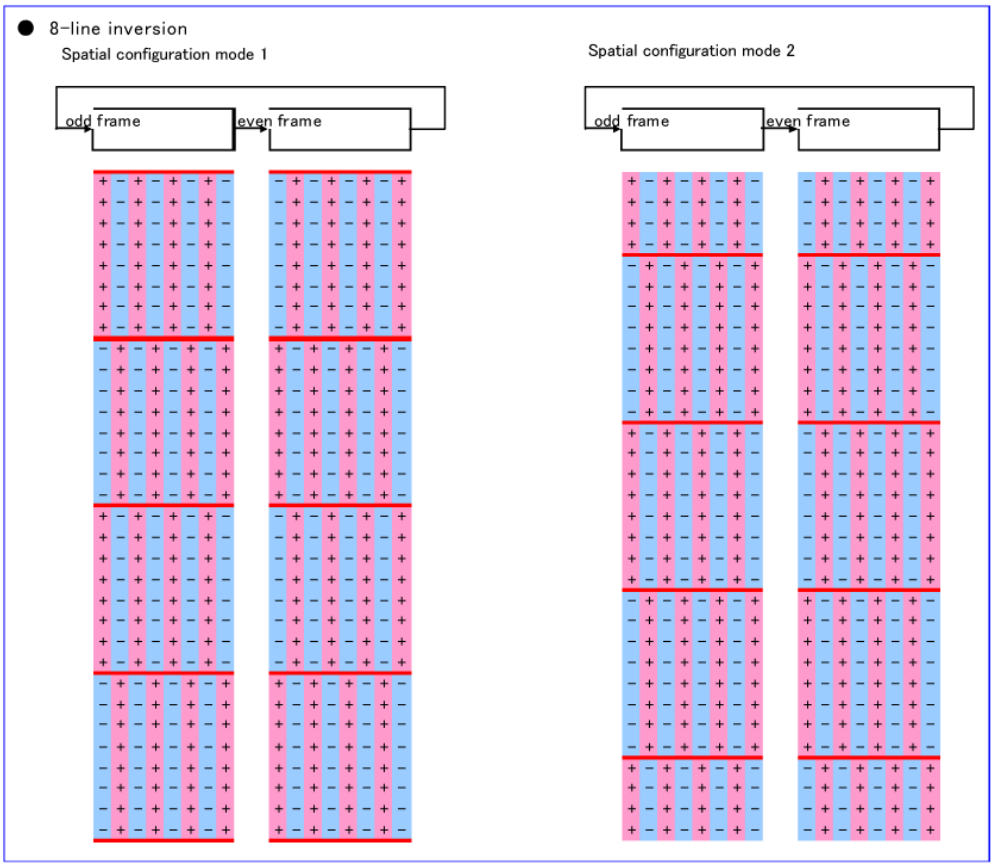
● 2-line inversion

Spatial configuration mode 1



Spatial configuration mode 2



Description	● 4-line inversion Spatial configuration mode 1 / Spatial configuration mode 2  ● 8-line inversion Spatial configuration mode 1 / Spatial configuration mode 2 
Restriction	Make sure that the total of lines set by the BP and FP bits is an even number.

Source／Gate Driving Timing Setting (C4h)

C4h	Panel Driving Setting											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	0	0	1	0	0	C4h
1st parameter	W / R	1	x	0	SDT [2]	SDT [1]	SDT [0]	0	NOW [2]	NOW [1]	NOW [0]	0Xh
2nd parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
3rd parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
4th parameter	W / R	1	x	0	0	0	0	SEQGND[3]	SEQGND[2]	SEQGND[1]	SEQGND[0]	XXh
5th parameter	W / R	1	x	0	0	0	0	SEQVCIL3]	SEQVCIL[2]	SEQVCIL[1]	SEQVCIL[0]	XXh

Description

SDT[2:0]

The bit is used to set the source output alternating position in 1 line period.

SDT[2:0]	Source output alternating position
3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h and C3h).

NOW[2:0]

These bits set the gate output start position (non-overlap period) in 1 line period.

NOW[2:0]	Gate output start position
3'h0	0 clock
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

These bits set the gate output start position (non-overlap period) in 1 line period.

Description

SEQGND[3:0]

Sets source pre-charge (pre-charge for GND) period.

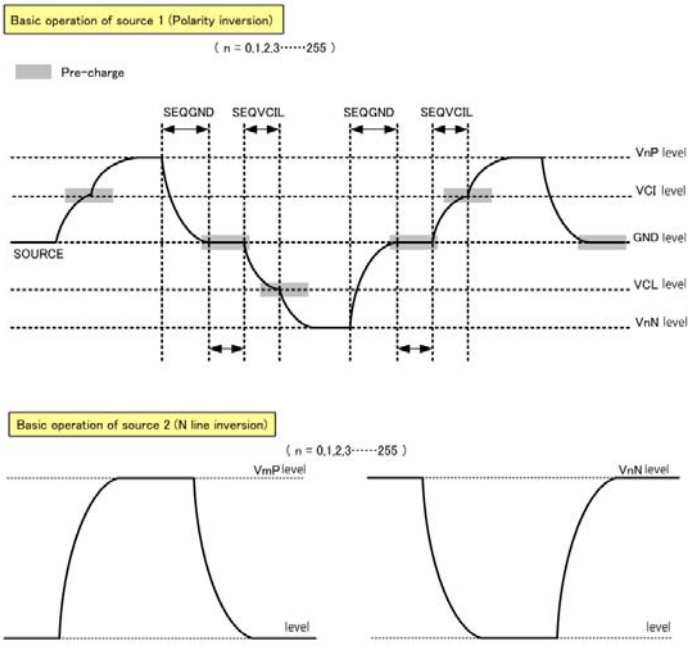
SEQGND[3:0]	Period
4'h0	Setting inhibited
4'h1	Setting inhibited
4'h2	Setting inhibited
4'h3	3clks
4'h4	4clks
4'h5	5clks
4'h6	6clks
:	:
4'h9	9clks
4'hA	10clks
4'hB	11clks
4'hC	12clks
4'hD	13clks
4'hE	14clks
4'hF	15clks

SEQVCIL[3:0]

Sets source pre-charge (pre-charge for VCI) period.

SEQVCIL[3:0]	Period
4'h0	Setting inhibited
4'h1	1clk
4'h2	2clks
4'h3	3clks
4'h4	4clks
4'h5	5clks
4'h6	6clks
:	:
4'h9	9clks
4'hA	10clks
4'hB	11clks
4'hC	12clks
4'hD	13clks
4'hE	14clks
4'hF	15clks

Examples of source output waveform (pre-charge)



DPI polarity Control (C6h)

C6h	Panel Driving Setting											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	0	0	1	1	0	C6h
1st parameter	W / R	1	x	0	0	0	VSPL	HSPL	EPL	0	DPL	XXh
Description												

VSPL

Sets the signal polarity of the VSYNC pin.

VSPL=0 Low active
VSPL=1 High active

HSPL

Sets the signal polarity of the HSYNC pin

HSPL=0 Low active
HSPL=1 High active

EPL

Sets the signal polarity of the DE pin

EPL=0 DE=0: Writing DB[23:0] data is enabled. DE=1: Writing DB[23:0] is disabled.
EPL=1 DE=0: Writing DB[23:0] data is disabled. DE=1: Writing DB[23:0] is enabled.

DPL

Sets the signal polarity of the PCLK pin.

DPL=0 Reads data on the rising edge of the PCLK signal.
DPL=1 Reads data on the falling edge of the PCLK signal.

Display Control Setting (C7h)

C7h	Display Control Setting											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	0	0	1	1	1	C7h
1st parameter	W / R	1	x	0	0	0	0	0	0	0	DEM	0Xh
2nd parameter	W / R	1	x	DTS [7]	DTS [6]	DTS [5]	DTS [4]	DTS [3]	DTS [2]	DTS [1]	DTS [0]	XXh

Description

DEM

Sets the data enable mode.

DEM	Setting	
0	Yes	Valid data period = ENABLE signal + BP setting
1	No	Valid data period = DTS and BP setting

DTS[7:0]

DEM=1 (No enable signal input): Sets the valid data start position.
1clk corresponds to a basic clock (CLK) which is set by DIV[3:0] of C5h command (2nd parameter).
1clk =0.5us (when DIV[3:0]=3'h2) or 1clk =0.643us (when DIV[3:0]=3"h4)

DTS[7:0]	設定
8'h00	設
8'h01	設
8'h02	設
8'h03	設
8'h04	設
8'h05	5c
8'h06	6c
:	:
8'h19	25
8'h1A	26
8'h1B	27
:	:
8'hFA	25
8'hFB	25
8'hFC	25
8'hFD	25
8'hFE	25
8'hFF	25

TBD.

Restriction

Gamma Control Command

Gamma Setting A set (C8h)

C8h	Gamma Setting A set											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	0	1	0	0	0	C8h
1st parameter	W / R	1	x	0	GSELA P0[6]	GSELA P0[5]	GSELA P0[4]	GSELA P0[3]	GSELA P0[2]	GSELA P0[1]	GSELA P0[0]	0Xh
2nd parameter	W / R	1	x	0	GSELA P1[6]	GSELA P1[5]	GSELA P1[4]	GSELA P1[3]	GSELA P1[2]	GSELA P1[1]	GSELA P1[0]	XXh
3rd parameter	W / R	1	x	0	GSELA P2[6]	GSELA P2[5]	GSELA P2[4]	GSELA P2[3]	GSELA P2[2]	GSELA P2[1]	GSELA P2[0]	XXh
4th parameter	W / R	1	x	0	GSELA P3[6]	GSELA P3[5]	GSELA P3[4]	GSELA P3[3]	GSELA P3[2]	GSELA P3[1]	GSELA P3[0]	XXh
5th parameter	W / R	1	x	0	GSELA P4[6]	GSELA P4[5]	GSELA P4[4]	GSELA P4[3]	GSELA P4[2]	GSELA P4[1]	GSELA P4[0]	XXh
6th parameter	W / R	1	x	0	GSELA P5[6]	GSELA P5[5]	GSELA P5[4]	GSELA P5[3]	GSELA P5[2]	GSELA P5[1]	GSELA P5[0]	XXh
7th parameter	W / R	1	x	0	GSELA P6[6]	GSELA P6[5]	GSELA P6[4]	GSELA P6[3]	GSELA P6[2]	GSELA P6[1]	GSELA P6[0]	XXh
8th parameter	W / R	1	x	0	GSELA P7[6]	GSELA P7[5]	GSELA P7[4]	GSELA P7[3]	GSELA P7[2]	GSELA P7[1]	GSELA P7[0]	XXh
9th parameter	W / R	1	x	0	GSELA P8[6]	GSELA P8[5]	GSELA P8[4]	GSELA P8[3]	GSELA P8[2]	GSELA P8[1]	GSELA P8[0]	XXh
10th parameter	W / R	1	x	0	GSELA P9[6]	GSELA P9[5]	GSELA P9[4]	GSELA P9[3]	GSELA P9[2]	GSELA P9[1]	GSELA P9[0]	XXh
11th parameter	W / R	1	x	0	GSELA P10[6]	GSELA P10[5]	GSELA P10[4]	GSELA P10[3]	GSELA P10[2]	GSELA P10[1]	GSELA P10[0]	XXh
12th parameter	W / R	1	x	0	GSELA P11[6]	GSELA P11[5]	GSELA P11[4]	GSELA P11[3]	GSELA P11[2]	GSELA P11[1]	GSELA P11[0]	XXh
13th parameter	W / R	1	x	0	GSELA N0[6]	GSELA N0[5]	GSELA N0[4]	GSELA N0[3]	GSELA N0[2]	GSELA N0[1]	GSELA N0[0]	XXh
14th parameter	W / R	1	x	0	GSELA N1[6]	GSELA N1[5]	GSELA N1[4]	GSELA N1[3]	GSELA N1[2]	GSELA N1[1]	GSELA N1[0]	XXh
15th parameter	W / R	1	x	0	GSELA N2[6]	GSELA N2[5]	GSELA N2[4]	GSELA N2[3]	GSELA N2[2]	GSELA N2[1]	GSELA N2[0]	XXh
16th parameter	W / R	1	x	0	GSELA N3[6]	GSELA N3[5]	GSELA N3[4]	GSELA N3[3]	GSELA N3[2]	GSELA N3[1]	GSELA N3[0]	XXh

17th parameter	W / R	1	x	0	GSELA N4[6]	GSELA N4[5]	GSELA N4[4]	GSELA N4[3]	GSELA N4[2]	GSELA N4[1]	GSELA N4[0]	XXh
18th parameter	W / R	1	x	0	GSELA N5[6]	GSELA N5[5]	GSELA N5[4]	GSELA N5[3]	GSELA N5[2]	GSELA N5[1]	GSELA N5[0]	XXh
19th parameter	W / R	1	x	0	GSELA N6[6]	GSELA N6[5]	GSELA N6[4]	GSELA N6[3]	GSELA N6[2]	GSELA N6[1]	GSELA N6[0]	XXh
20th parameter	W / R	1	x	0	GSELA N7[6]	GSELA N7[5]	GSELA N7[4]	GSELA N7[3]	GSELA N7[2]	GSELA N7[1]	GSELA N7[0]	XXh
21st parameter	W / R	1	x	0	GSELA N8[6]	GSELA N8[5]	GSELA N8[4]	GSELA N8[3]	GSELA N8[2]	GSELA N8[1]	GSELA N8[0]	XXh
22nd parameter	W / R	1	x	0	GSELA N9[6]	GSELA N9[5]	GSELA N9[4]	GSELA N9[3]	GSELA N9[2]	GSELA N9[1]	GSELA N9[0]	XXh
23rd parameter	W / R	1	x	0	GSELA N10[6]	GSELA N10[5]	GSELA N10[4]	GSELA N10[3]	GSELA N10[2]	GSELA N10[1]	GSELA N10[0]	XXh
24th parameter	W / R	1	x	0	GSELA N11[6]	GSELA N11[5]	GSELA N11[4]	GSELA N11[3]	GSELA N11[2]	GSELA N11[1]	GSELA N11[0]	XXh
Description	Gamma Setting A Set registers are applied to red grayscale. See "Gamma Correction Function" for detailed description of the parameters.											

Gamma Setting B set (C9h)

C9h	Gamma Setting B set											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	0	1	0	0	1	C9h
1st parameter	W / R	1	x	0	GSELB P0[6]	GSELB P0[5]	GSELB P0[4]	GSELB P0[3]	GSELB P0[2]	GSELB P0[1]	GSELB P0[0]	0Xh
2nd parameter	W / R	1	x	0	GSELB P1[6]	GSELB P1[5]	GSELB P1[4]	GSELB P1[3]	GSELB P1[2]	GSELB P1[1]	GSELB P1[0]	XXh
3rd parameter	W / R	1	x	0	GSELB P2[6]	GSELB P2[5]	GSELB P2[4]	GSELB P2[3]	GSELB P2[2]	GSELB P2[1]	GSELB P2[0]	XXh
4th parameter	W / R	1	x	0	GSELB P3[6]	GSELB P3[5]	GSELB P3[4]	GSELB P3[3]	GSELB P3[2]	GSELB P3[1]	GSELB P3[0]	XXh
5th parameter	W / R	1	x	0	GSELB P4[6]	GSELB P4[5]	GSELB P4[4]	GSELB P4[3]	GSELB P4[2]	GSELB P4[1]	GSELB P4[0]	XXh
6th parameter	W / R	1	x	0	GSELB P5[6]	GSELB P5[5]	GSELB P5[4]	GSELB P5[3]	GSELB P5[2]	GSELB P5[1]	GSELB P5[0]	XXh
7th parameter	W / R	1	x	0	GSELB P6[6]	GSELB P6[5]	GSELB P6[4]	GSELB P6[3]	GSELB P6[2]	GSELB P6[1]	GSELB P6[0]	XXh
8th parameter	W / R	1	x	0	GSELB P7[6]	GSELB P7[5]	GSELB P7[4]	GSELB P7[3]	GSELB P7[2]	GSELB P7[1]	GSELB P7[0]	XXh
9th parameter	W / R	1	x	0	GSELB P8[6]	GSELB P8[5]	GSELB P8[4]	GSELB P8[3]	GSELB P8[2]	GSELB P8[1]	GSELB P8[0]	XXh
10th parameter	W / R	1	x	0	GSELB P9[6]	GSELB P9[5]	GSELB P9[4]	GSELB P9[3]	GSELB P9[2]	GSELB P9[1]	GSELB P9[0]	XXh
11th parameter	W / R	1	x	0	GSELB P10[6]	GSELB P10[5]	GSELB P10[4]	GSELB P10[3]	GSELB P10[2]	GSELB P10[1]	GSELB P10[0]	XXh
12th parameter	W / R	1	x	0	GSELB P11[6]	GSELB P11[5]	GSELB P11[4]	GSELB P11[3]	GSELB P11[2]	GSELB P11[1]	GSELB P11[0]	XXh
13th parameter	W / R	1	x	0	GSELB N0[6]	GSELB N0[5]	GSELB N0[4]	GSELB N0[3]	GSELB N0[2]	GSELB N0[1]	GSELB N0[0]	XXh
14th parameter	W / R	1	x	0	GSELB N1[6]	GSELB N1[5]	GSELB N1[4]	GSELB N1[3]	GSELB N1[2]	GSELB N1[1]	GSELB N1[0]	XXh
15th parameter	W / R	1	x	0	GSELB N2[6]	GSELB N2[5]	GSELB N2[4]	GSELB N2[3]	GSELB N2[2]	GSELB N2[1]	GSELB N2[0]	XXh
16th parameter	W / R	1	x	0	GSELB N3[6]	GSELB N3[5]	GSELB N3[4]	GSELB N3[3]	GSELB N3[2]	GSELB N3[1]	GSELB N3[0]	XXh

17th parameter	W / R	1	x	0	GSELB N4[6]	GSELB N4[5]	GSELB N4[4]	GSELB N4[3]	GSELB N4[2]	GSELB N4[1]	GSELB N4[0]	XXh
18th parameter	W / R	1	x	0	GSELB N5[6]	GSELB N5[5]	GSELB N5[4]	GSELB N5[3]	GSELB N5[2]	GSELB N5[1]	GSELB N5[0]	XXh
19th parameter	W / R	1	x	0	GSELB N6[6]	GSELB N6[5]	GSELB N6[4]	GSELB N6[3]	GSELB N6[2]	GSELB N6[1]	GSELB N6[0]	XXh
20th parameter	W / R	1	x	0	GSELB N7[6]	GSELB N7[5]	GSELB N7[4]	GSELB N7[3]	GSELB N7[2]	GSELB N7[1]	GSELB N7[0]	XXh
21st parameter	W / R	1	x	0	GSELB N8[6]	GSELB N8[5]	GSELB N8[4]	GSELB N8[3]	GSELB N8[2]	GSELB N8[1]	GSELB N8[0]	XXh
22nd parameter	W / R	1	x	0	GSELB N9[6]	GSELB N9[5]	GSELB N9[4]	GSELB N9[3]	GSELB N9[2]	GSELB N9[1]	GSELB N9[0]	XXh
23rd parameter	W / R	1	x	0	GSELB N10[6]	GSELB N10[5]	GSELB N10[4]	GSELB N10[3]	GSELB N10[2]	GSELB N10[1]	GSELB N10[0]	XXh
24th parameter	W / R	1	x	0	GSELB N11[6]	GSELB N11[5]	GSELB N11[4]	GSELB N11[3]	GSELB N11[2]	GSELB N11[1]	GSELB N11[0]	XXh
Description	Gamma Setting B Set registers are applied to green grayscale. See "Gamma Correction Function" for detailed description of the parameters.											

Gamma Setting C set (CAh)

CAh	Gamma Setting C set											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	0	1	0	1	0	CAh
1st parameter	W / R	1	x	0	GSELC P0[6]	GSELC P0[5]	GSELC P0[4]	GSELC P0[3]	GSELC P0[2]	GSELC P0[1]	GSELC P0[0]	0Xh
2nd parameter	W / R	1	x	0	GSELC P1[6]	GSELC P1[5]	GSELC P1[4]	GSELC P1[3]	GSELC P1[2]	GSELC P1[1]	GSELC P1[0]	XXh
3rd parameter	W / R	1	x	0	GSELC P2[6]	GSELC P2[5]	GSELC P2[4]	GSELC P2[3]	GSELC P2[2]	GSELC P2[1]	GSELC P2[0]	XXh
4th parameter	W / R	1	x	0	GSELC P3[6]	GSELC P3[5]	GSELC P3[4]	GSELC P3[3]	GSELC P3[2]	GSELC P3[1]	GSELC P3[0]	XXh
5th parameter	W / R	1	x	0	GSELC P4[6]	GSELC P4[5]	GSELC P4[4]	GSELC P4[3]	GSELC P4[2]	GSELC P4[1]	GSELC P4[0]	XXh
6th parameter	W / R	1	x	0	GSELC P5[6]	GSELC P5[5]	GSELC P5[4]	GSELC P5[3]	GSELC P5[2]	GSELC P5[1]	GSELC P5[0]	XXh
7th parameter	W / R	1	x	0	GSELC P6[6]	GSELC P6[5]	GSELC P6[4]	GSELC P6[3]	GSELC P6[2]	GSELC P6[1]	GSELC P6[0]	XXh
8th parameter	W / R	1	x	0	GSELC P7[6]	GSELC P7[5]	GSELC P7[4]	GSELC P7[3]	GSELC P7[2]	GSELC P7[1]	GSELC P7[0]	XXh
9th parameter	W / R	1	x	0	GSELC P8[6]	GSELC P8[5]	GSELC P8[4]	GSELC P8[3]	GSELC P8[2]	GSELC P8[1]	GSELC P8[0]	XXh
10th parameter	W / R	1	x	0	GSELC P9[6]	GSELC P9[5]	GSELC P9[4]	GSELC P9[3]	GSELC P9[2]	GSELC P9[1]	GSELC P9[0]	XXh
11th parameter	W / R	1	x	0	GSELC P10[6]	GSELC P10[5]	GSELC P10[4]	GSELC P10[3]	GSELC P10[2]	GSELC P10[1]	GSELC P10[0]	XXh
12th parameter	W / R	1	x	0	GSELC P11[6]	GSELC P11[5]	GSELC P11[4]	GSELC P11[3]	GSELC P11[2]	GSELC P11[1]	GSELC P11[0]	XXh
13th parameter	W / R	1	x	0	GSELC N0[6]	GSELC N0[5]	GSELC N0[4]	GSELC N0[3]	GSELC N0[2]	GSELC N0[1]	GSELC N0[0]	XXh
14th parameter	W / R	1	x	0	GSELC N1[6]	GSELC N1[5]	GSELC N1[4]	GSELC N1[3]	GSELC N1[2]	GSELC N1[1]	GSELC N1[0]	XXh
15th parameter	W / R	1	x	0	GSELC N2[6]	GSELC N2[5]	GSELC N2[4]	GSELC N2[3]	GSELC N2[2]	GSELC N2[1]	GSELC N2[0]	XXh
16th parameter	W / R	1	x	0	GSELC N3[6]	GSELC N3[5]	GSELC N3[4]	GSELC N3[3]	GSELC N3[2]	GSELC N3[1]	GSELC N3[0]	XXh

17th parameter	W / R	1	x	0	GSELC N4[6]	GSELC N4[5]	GSELC N4[4]	GSELC N4[3]	GSELC N4[2]	GSELC N4[1]	GSELC N4[0]	XXh
18th parameter	W / R	1	x	0	GSELC N5[6]	GSELC N5[5]	GSELC N5[4]	GSELC N5[3]	GSELC N5[2]	GSELC N5[1]	GSELC N5[0]	XXh
19th parameter	W / R	1	x	0	GSELC N6[6]	GSELC N6[5]	GSELC N6[4]	GSELC N6[3]	GSELC N6[2]	GSELC N6[1]	GSELC N6[0]	XXh
20th parameter	W / R	1	x	0	GSELC N7[6]	GSELC N7[5]	GSELC N7[4]	GSELC N7[3]	GSELC N7[2]	GSELC N7[1]	GSELC N7[0]	XXh
21st parameter	W / R	1	x	0	GSELC N8[6]	GSELC N8[5]	GSELC N8[4]	GSELC N8[3]	GSELC N8[2]	GSELC N8[1]	GSELC N8[0]	XXh
22nd parameter	W / R	1	x	0	GSELC N9[6]	GSELC N9[5]	GSELC N9[4]	GSELC N9[3]	GSELC N9[2]	GSELC N9[1]	GSELC N9[0]	XXh
23rd parameter	W / R	1	x	0	GSELC N10[6]	GSELC N10[5]	GSELC N10[4]	GSELC N10[3]	GSELC N10[2]	GSELC N10[1]	GSELC N10[0]	XXh
24th parameter	W / R	1	x	0	GSELC N11[6]	GSELC N11[5]	GSELC N11[4]	GSELC N11[3]	GSELC N11[2]	GSELC N11[1]	GSELC N11[0]	XXh
Description	Gamma Setting C Set registers are applied to blue grayscale. See "Gamma Correction Function" for detailed description of the parameters.											
Restriction												

Power Control Command

Power Setting (D0h)

D0h	Power Setting (Charge Pump Setting)											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	1	0	0	0	0	D0h
1st parameter	W / R	1	x	0	1	1	1	0	0	DC1 [1]	DC1 [0]	7Xh
2nd parameter	W / R	1	x	0	0	0	0	0	0	DC2 [1]	DC2 [0]	XXh
3rd parameter	W / R	1	x	1	VLMT 4[2]	VLMT 4[1]	VLMT 4[0]	0	0	DC4 [1]	DC4 [0]	XXh
4th parameter	W / R	1	x	1	1	1	1	0	0	DC1M [1]	DC1M [0]	FXh
5th parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
6th parameter	W / R	1	x	0	VC3 [2]	VC3 [1]	VC3 [0]	0	VC2 [2]	VC2 [1]	VC2 [0]	XXh
7th parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
8th parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
9th parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
10th parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
11th parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h
12th parameter	W / R	1	x	0	0	0	0	0	0	0	0	00h

Description

DC1[1:0]

Sets a step-up clock cycle of the internal step-up circuit generating VSP when charge pump is used. 1H equals 1 horizontal (line) period.

DC1[1:0]	Step-up clock cycle
2'h0	Halt
2'h1	1H
2'h2	1/2H
2'h3	Setting inhibited

DC2[1:0]

Sets a step-up clock cycle of the internal step-up circuit generating VGH and VGL. 1H equals 1 horizontal (line) period. 2H equals 2 horizontal (2-line) periods.

DC2[1:0]	Step-up clock cycle
2'h0	Halt
2'h1	2H
2'h2	4H
2'h3	8H

DC4[1:0]

Sets a step-up clock cycle of the internal step-up circuit generating VCL. 1H equals 1 horizontal (line) period.

DC4[1:0]	Step-up clock cycle
2'h0	Halt
2'h1	1H
2'h2	1/2H
2'h3	Setting inhibited

VLMT4[2:0]

Sets VCL step-up limit voltage. Make sure that VCI-VCL ≤ 6V.

VLMT4[2:0]	VCL step-up limit voltage
3'h0	No limit
3'h1	-2.40V
3'h2	-2.50V
3'h3	-2.60V
3'h4	-2.70V
3'h5	-2.80V
3'h6	-2.90V
3'h7	-3.00V

DC1M[1:0]

Sets a step-up clock cycle of the internal step-up circuit generating VSN when charge pump is used.

DC1M[1:0]	Step-up clock cycle
2'h0	Halt
2'h1	1H
2'h2	1/2H
2'h3	Setting inhibited

VC2[2:0]

Sets VCI2 that is power supply of voltage generating VGH and VGL.

VC2[2:0]	VCI2 voltage
3'h0	Setting inhibited
3'h1	3.60V
3'h2	3.80V
3'h3	4.00V
3'h4	4.20V
3'h5	4.40V
3'h6	4.60V
3'h7	4.80V

VC3[2:0]

Sets VCI3 that is power supply of voltage generating VGH and VGL.

VC3[2:0]	VCI3 voltage
3'h0	Setting inhibited
3'h1	Setting inhibited
3'h2	2.00V
3'h3	2.20V
3'h4	2.40V
3'h5	2.60V
3'h6	2.80V
3'h7	3.00V

Write 00h in the 7th to 12th parameters.

Restriction	

Power Setting for Normal Mode (D3h)

D3h	Power Setting for Normal Mode											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	1	0	0	1	1	D3h
1st parameter	W / R	1	x	0	APN [2]	APN [1]	APN [0]	0	AP[2]	AP[1]	AP[0]	XXh

Description

AP[2:0]

Adjusts the constant current in the operational amplifier circuit on the positive polarity of the LCD power supply circuit. Adjust the constant current taking the trade-off into account between the display quality and the current consumption.

AP[2:0]	Constant current in operational amplifier in LCD power supply circuit
3'h0	Halt
3'h1	50%(TBD)
3'h2	75%(TBD)
3'h3	100%(TBD)
3'h4	125%(TBD)
3'h5	Setting inhibited
3'h6	Setting inhibited
3'h7	Setting inhibited

APN[2:0]

Adjusts the constant current in the operational amplifier circuit on the positive polarity of the LCD power supply circuit. Adjust the constant current taking the trade-off into account between the display quality and the current consumption.

APN[2:0]	Constant current in operational amplifier in LCD power supply circuit
3'h0	Halt
3'h1	50%(TBD)
3'h2	75%(TBD)
3'h3	100%(TBD)
3'h4	125%(TBD)
3'h5	Setting inhibited
3'h6	Setting inhibited
3'h7	Setting inhibited

Restriction

VCOM Setting (D5h)

D5h	VCOM Setting											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	0	1	0	1	0	1	D5h
1st parameter	W / R	1	x	0	0	0	0	0	0	WCVDC	0	0Xh
2nd parameter	W / R	1	x	0	PVH [6]	PVH [5]	PVH [4]	PVH [3]	PVH [2]	PVH [1]	PVH [0]	XXh
3rd parameter	W / R	1	x	0	NVH [6]	NVH [5]	NVH [4]	NVH [3]	NVH [2]	NVH [1]	NVH [0]	XXh
4th parameter	W / R	1	x	VDC [7]	VDC [6]	VDC [5]	VDC [4]	VDC [3]	VDC [2]	VDC [1]	VDC [0]	XXh

Description

WCVDC

WCVCM=1: Used to enable write to VDC[7:0]. To set NVM write data, write 1 in WCVCM.
WCVCM=0: Used to disable write to VDC[7:0]. Values loaded from NVM are retained even if this parameter is written.

PVH[6:0]

Sets VPLVL that is reference voltage of γ correction registers for positive polarity. Make sure that VSP – VPLVL ≥ 0.3V.

PVH [6:0]	VPLVL
7'h00	5.700V
7'h01	5.675V
7'h02	5.650V
7'h03	5.625V
7'h04	5.600V
7'h05	5.575V
7'h06	5.550V
7'h07	5.525V
7'h08	5.500V
7'h09	5.475V
7'h0A	5.450V
7'h0B	5.425V
7'h0C	5.400V
7'h0D	5.375V
7'h0E	5.350V
7'h0F	5.325V

PVH [6:0]	VPLVL
7'h10	5.300V
7'h11	5.275V
7'h12	5.250V
7'h13	5.225V
7'h14	5.200V
7'h15	5.175V
7'h16	5.150V
7'h17	5.125V
7'h18	5.100V
7'h19	5.075V
7'h1A	5.050V
7'h1B	5.025V
7'h1C	5.000V
7'h1D	4.975V
7'h1E	4.950V
7'h1F	4.925V

PVH [6:0]	VPLVL
7'h20	4.900V
7'h21	4.875V
7'h22	4.850V
7'h23	4.825V
7'h24	4.800V
7'h25	4.775V
7'h26	4.750V
7'h27	4.725V
7'h28	4.700V
7'h29	4.675V
7'h2A	4.650V
7'h2B	4.625V
7'h2C	4.600V
7'h2D	4.575V
7'h2E	4.550V
7'h2F	4.525V

Description

PVH [6:0]	VPLVL
7'h30	4.500V
7'h31	4.475V
7'h32	4.450V
7'h33	4.425V
7'h34	4.400V
7'h35	4.375V
7'h36	4.350V
7'h37	4.325V
7'h38	4.300V
7'h39	4.275V
7'h3A	4.250V
7'h3B	4.225V
7'h3C	4.200V
7'h3D	4.175V
7'h3E	4.150V
7'h3F	4.125V
7'h40	4.100V
7'h41	4.075V
7'h42	4.050V
7'h43	4.025V
7'h44	4.000V
7'h45	3.975V
7'h46	3.950V
7'h47	3.925V

PVH [6:0]	VPLVL
7'h48	3.900V
7'h49	3.875V
7'h4A	3.850V
7'h4B	3.825V
7'h4C	3.800V
7'h4D	3.775V
7'h4E	3.750V
7'h4F	3.725V
7'h50	3.700V
7'h51	3.675V
7'h52	3.650V
7'h53	3.625V
7'h54	3.600V
7'h55	3.575V
7'h56	3.550V
7'h57	3.525V
7'h58	3.500V
7'h59	3.475V
7'h5A	3.450V
7'h5B	3.425V
7'h5C	3.400V
7'h5D	3.375V
7'h5E	3.350V
7'h5F	3.325V

PVH [6:0]	VPLVL
7'h60	3.300V
7'h61	3.275V
7'h62	3.250V
7'h63	3.225V
7'h64	3.200V
7'h65	3.175V
7'h66	3.150V
7'h67	3.125V
7'h68	3.100V
7'h69	3.075V
7'h6A	3.050V
7'h6B	3.025V
7'h6C	3.000V
7'h6D	Setting inhibited
7'h6E	Setting inhibited
7'h6F	Setting inhibited
7'h70	Setting inhibited
7'h71	Setting inhibited
7'h72	Setting inhibited
:	:
7'h7C	Setting inhibited
7'h7D	Setting inhibited
7'h7E	Setting inhibited
7'h7F	Setting inhibited

NVH[6:0]

Sets VNLVL that is reference voltage of γ correction registers for negative polarity. Make sure that VSP – VPLVL ≥ 0.3V.

NVH [6:0]	VNLVL	NVH [6:0]	VNLVL	NVH [6:0]	VNLVL
7'h00	-5.700V	7'h20	-4.900V	7'h40	-4.100V
7'h01	-5.675V	7'h21	-4.875V	7'h41	-4.075V
7'h02	-5.650V	7'h22	-4.850V	7'h42	-4.050V
7'h03	-5.625V	7'h23	-4.825V	7'h43	-4.025V
7'h04	-5.600V	7'h24	-4.800V	7'h44	-4.000V
7'h05	-5.575V	7'h25	-4.775V	7'h45	-3.975V
7'h06	-5.550V	7'h26	-4.750V	7'h46	-3.950V
7'h07	-5.525V	7'h27	-4.725V	7'h47	-3.925V
7'h08	-5.500V	7'h28	-4.700V	7'h48	-3.900V
7'h09	-5.475V	7'h29	-4.675V	7'h49	-3.875V
7'h0A	-5.450V	7'h2A	-4.650V	7'h4A	-3.850V
7'h0B	-5.425V	7'h2B	-4.625V	7'h4B	-3.825V
7'h0C	-5.400V	7'h2C	-4.600V	7'h4C	-3.800V
7'h0D	-5.375V	7'h2D	-4.575V	7'h4D	-3.775V
7'h0E	-5.350V	7'h2E	-4.550V	7'h4E	-3.750V
7'h0F	-5.325V	7'h2F	-4.525V	7'h4F	-3.725V
7'h10	-5.300V	7'h30	-4.500V	7'h50	-3.700V
7'h11	-5.275V	7'h31	-4.475V	7'h51	-3.675V
7'h12	-5.250V	7'h32	-4.450V	7'h52	-3.650V
7'h13	-5.225V	7'h33	-4.425V	7'h53	-3.625V
7'h14	-5.200V	7'h34	-4.400V	7'h54	-3.600V
7'h15	-5.175V	7'h35	-4.375V	7'h55	-3.575V
7'h16	-5.150V	7'h36	-4.350V	7'h56	-3.550V
7'h17	-5.125V	7'h37	-4.325V	7'h57	-3.525V
7'h18	-5.100V	7'h38	-4.300V	7'h58	-3.500V
7'h19	-5.075V	7'h39	-4.275V	7'h59	-3.475V
7'h1A	-5.050V	7'h3A	-4.250V	7'h5A	-3.450V
7'h1B	-5.025V	7'h3B	-4.225V	7'h5B	-3.425V
7'h1C	-5.000V	7'h3C	-4.200V	7'h5C	-3.400V
7'h1D	-4.975V	7'h3D	-4.175V	7'h5D	-3.375V
7'h1E	-4.950V	7'h3E	-4.150V	7'h5E	-3.350V
7'h1F	-4.925V	7'h3F	-4.125V	7'h5F	-3.325V

Description

NVH [6:0]	VNLVL
7'h60	-3.300V
7'h61	-3.275V
7'h62	-3.250V
7'h63	-3.225V
7'h64	-3.200V
7'h65	-3.175V
7'h66	-3.150V
7'h67	-3.125V

NVH [6:0]	VNLVL
7'h68	-3.100V
7'h69	-3.075V
7'h6A	-3.050V
7'h6B	-3.025V
7'h6C	-3.000V
7'h6D	Setting inhibited
7'h6E	Setting inhibited
7'h6F	Setting inhibited

NVH [6:0]	VNLVL
7'h70	Setting inhibited
7'h71	Setting inhibited
7'h72	Setting inhibited
:	:
7'h7C	Setting inhibited
7'h7D	Setting inhibited
7'h7E	Setting inhibited
7'h7F	Setting inhibited

VDC[7:0]

The bit is used to set VCOMDC output voltage. VCOMDC = -0.3V ~ -3.0V.

VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC
8'h00	Setting inhibited	8'h20	VNLVL x 0.096	8'h40	VNLVL x 0.193
8'h01	Setting inhibited	8'h21	VNLVL x 0.099	8'h41	VNLVL x 0.196
8'h02	Setting inhibited	8'h22	VNLVL x 0.102	8'h42	VNLVL x 0.199
8'h03	Setting inhibited	8'h23	VNLVL x 0.105	8'h43	VNLVL x 0.202
8'h04	Setting inhibited	8'h24	VNLVL x 0.108	8'h44	VNLVL x 0.205
8'h05	Setting inhibited	8'h25	VNLVL x 0.111	8'h45	VNLVL x 0.208
8'h06	Setting inhibited	8'h26	VNLVL x 0.114	8'h46	VNLVL x 0.211
8'h07	Setting inhibited	8'h27	VNLVL x 0.117	8'h47	VNLVL x 0.214
8'h08	Setting inhibited	8'h28	VNLVL x 0.120	8'h48	VNLVL x 0.217
8'h09	Setting inhibited	8'h29	VNLVL x 0.123	8'h49	VNLVL x 0.220
8'h0A	Setting inhibited	8'h2A	VNLVL x 0.127	8'h4A	VNLVL x 0.223
8'h0B	Setting inhibited	8'h2B	VNLVL x 0.130	8'h4B	VNLVL x 0.226
8'h0C	Setting inhibited	8'h2C	VNLVL x 0.133	8'h4C	VNLVL x 0.229
8'h0D	Setting inhibited	8'h2D	VNLVL x 0.136	8'h4D	VNLVL x 0.232
8'h0E	Setting inhibited	8'h2E	VNLVL x 0.139	8'h4E	VNLVL x 0.235
8'h0F	Setting inhibited	8'h2F	VNLVL x 0.142	8'h4F	VNLVL x 0.238
8'h10	VNLVL x 0.048	8'h30	VNLVL x 0.145	8'h50	VNLVL x 0.241
8'h11	VNLVL x 0.051	8'h31	VNLVL x 0.148	8'h51	VNLVL x 0.244
8'h12	VNLVL x 0.054	8'h32	VNLVL x 0.151	8'h52	VNLVL x 0.247
8'h13	VNLVL x 0.057	8'h33	VNLVL x 0.154	8'h53	VNLVL x 0.250
8'h14	VNLVL x 0.060	8'h34	VNLVL x 0.157	8'h54	VNLVL x 0.253
8'h15	VNLVL x 0.063	8'h35	VNLVL x 0.160	8'h55	VNLVL x 0.256
8'h16	VNLVL x 0.066	8'h36	VNLVL x 0.163	8'h56	VNLVL x 0.259
8'h17	VNLVL x 0.069	8'h37	VNLVL x 0.166	8'h57	VNLVL x 0.262
8'h18	VNLVL x 0.072	8'h38	VNLVL x 0.169	8'h58	VNLVL x 0.265
8'h19	VNLVL x 0.075	8'h39	VNLVL x 0.172	8'h59	VNLVL x 0.268
8'h1A	VNLVL x 0.078	8'h3A	VNLVL x 0.175	8'h5A	VNLVL x 0.271
8'h1B	VNLVL x 0.081	8'h3B	VNLVL x 0.178	8'h5B	VNLVL x 0.274
8'h1C	VNLVL x 0.084	8'h3C	VNLVL x 0.181	8'h5C	VNLVL x 0.277
8'h1D	VNLVL x 0.087	8'h3D	VNLVL x 0.184	8'h5D	VNLVL x 0.280
8'h1E	VNLVL x 0.090	8'h3E	VNLVL x 0.187	8'h5E	VNLVL x 0.283
8'h1F	VNLVL x 0.093	8'h3F	VNLVL x 0.190	8'h5F	VNLVL x 0.286

Description

VDC[7:0]	VCOMDC
8'h60	VNLVL x 0.289
8'h61	VNLVL x 0.292
8'h62	VNLVL x 0.295
8'h63	VNLVL x 0.298
8'h64	VNLVL x 0.301
8'h65	VNLVL x 0.304
8'h66	VNLVL x 0.307
8'h67	VNLVL x 0.310
8'h68	VNLVL x 0.313
8'h69	VNLVL x 0.316
8'h6A	VNLVL x 0.319
8'h6B	VNLVL x 0.322
8'h6C	VNLVL x 0.325
8'h6D	VNLVL x 0.328
8'h6E	VNLVL x 0.331
8'h6F	VNLVL x 0.334
8'h70	VNLVL x 0.337
8'h71	VNLVL x 0.340
8'h72	VNLVL x 0.343
8'h73	VNLVL x 0.346
8'h74	VNLVL x 0.349
8'h75	VNLVL x 0.352
8'h76	VNLVL x 0.355
8'h77	VNLVL x 0.358
8'h78	VNLVL x 0.361
8'h79	VNLVL x 0.364
8'h7A	VNLVL x 0.367
8'h7B	VNLVL x 0.370
8'h7C	VNLVL x 0.373
8'h7D	VNLVL x 0.377
8'h7E	VNLVL x 0.380
8'h7F	VNLVL x 0.383

VDC[7:0]	VCOMDC
8'h80	VNLVL x 0.386
8'h81	VNLVL x 0.389
8'h82	VNLVL x 0.392
8'h83	VNLVL x 0.395
8'h84	VNLVL x 0.398
8'h85	VNLVL x 0.401
8'h86	VNLVL x 0.404
8'h87	VNLVL x 0.407
8'h88	VNLVL x 0.410
8'h89	VNLVL x 0.413
8'h8A	VNLVL x 0.416
8'h8B	VNLVL x 0.419
8'h8C	VNLVL x 0.422
8'h8D	VNLVL x 0.425
8'h8E	VNLVL x 0.428
8'h8F	VNLVL x 0.431
8'h90	VNLVL x 0.434
8'h91	VNLVL x 0.437
8'h92	VNLVL x 0.440
8'h93	VNLVL x 0.443
8'h94	VNLVL x 0.446
8'h95	VNLVL x 0.449
8'h96	VNLVL x 0.452
8'h97	VNLVL x 0.455
8'h98	VNLVL x 0.458
8'h99	VNLVL x 0.461
8'h9A	VNLVL x 0.464
8'h9B	VNLVL x 0.467
8'h9C	VNLVL x 0.470
8'h9D	VNLVL x 0.473
8'h9E	VNLVL x 0.476
8'h9F	VNLVL x 0.479

VDC[7:0]	VCOMDC
8'hA0	VNLVL x 0.482
8'hA1	VNLVL x 0.485
8'hA2	VNLVL x 0.488
8'hA3	VNLVL x 0.491
8'hA4	VNLVL x 0.494
8'hA5	VNLVL x 0.497
8'hA6	VNLVL x 0.500
8'hA7	VNLVL x 0.503
8'hA8	VNLVL x 0.506
8'hA9	VNLVL x 0.509
8'hAA	VNLVL x 0.512
8'hAB	VNLVL x 0.515
8'hAC	VNLVL x 0.518
8'hAD	VNLVL x 0.521
8'hAE	VNLVL x 0.524
8'hAF	VNLVL x 0.527
8'hB0	VNLVL x 0.530
8'hB1	VNLVL x 0.533
8'hB2	VNLVL x 0.536
8'hB3	VNLVL x 0.539
8'hB4	VNLVL x 0.542
8'hB5	VNLVL x 0.545
8'hB6	VNLVL x 0.548
8'hB7	VNLVL x 0.551
8'hB8	VNLVL x 0.554
8'hB9	VNLVL x 0.557
8'hBA	VNLVL x 0.560
8'hBB	VNLVL x 0.563
8'hBC	VNLVL x 0.566
8'hBD	VNLVL x 0.569
8'hBE	VNLVL x 0.572
8'hBF	VNLVL x 0.575

Description

VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC
8'h80	VNLVL x 0.386	8'hB0	VNLVL x 0.530	8'hE0	VNLVL x 0.675
8'h81	VNLVL x 0.389	8'hB1	VNLVL x 0.533	8'hE1	VNLVL x 0.678
8'h82	VNLVL x 0.392	8'hB2	VNLVL x 0.536	8'hE2	VNLVL x 0.681
8'h83	VNLVL x 0.395	8'hB3	VNLVL x 0.539	8'hE3	VNLVL x 0.684
8'h84	VNLVL x 0.398	8'hB4	VNLVL x 0.542	8'hE4	VNLVL x 0.687
8'h85	VNLVL x 0.401	8'hB5	VNLVL x 0.545	8'hE5	VNLVL x 0.690
8'h86	VNLVL x 0.404	8'hB6	VNLVL x 0.548	8'hE6	VNLVL x 0.693
8'h87	VNLVL x 0.407	8'hB7	VNLVL x 0.551	8'hE7	VNLVL x 0.696
8'h88	VNLVL x 0.410	8'hB8	VNLVL x 0.554	8'hE8	VNLVL x 0.699
8'h89	VNLVL x 0.413	8'hB9	VNLVL x 0.557	8'hE9	VNLVL x 0.702
8'h8A	VNLVL x 0.416	8'hBA	VNLVL x 0.560	8'hEA	VNLVL x 0.705
8'h8B	VNLVL x 0.419	8'hBB	VNLVL x 0.563	8'hEB	VNLVL x 0.708
8'h8C	VNLVL x 0.422	8'hBC	VNLVL x 0.566	8'hEC	VNLVL x 0.711
8'h8D	VNLVL x 0.425	8'hBD	VNLVL x 0.569	8'hED	VNLVL x 0.714
8'h8E	VNLVL x 0.428	8'hBE	VNLVL x 0.572	8'hEE	VNLVL x 0.717
8'h8F	VNLVL x 0.431	8'hBF	VNLVL x 0.575	8'hEF	VNLVL x 0.720

Setting VDC[7:0] to any of 8'hF0 to 8'hFF is prohibited.

Restriction

NVM Control Command

NVM Access Control (E0h)

E0h	NVM Access Control											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	X	1	1	1	0	0	0	0	0	E0h
1st parameter	W / R	1	X	0	0	0	0	0	0	0	NVAE	00h
2nd parameter	W / R	1	X	0	FTT	0	0	0	0	0	0	00h
3rd parameter	W / R	1	X	0	0	0	TEM [0]	0	0	VERIF LGWR	VERIF LGER	00h
4th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h

Description

NVAE

NVM access enable register. NVM access is enabled when NVAE=1.

FTT

NVM access control register. When FTT=1, NVM write operation or NVM erase operation starts. After NVM write and verify operations, FTT is returned to 0.

VERIFLGER

When data is written to NVM, this bit returns erase-verify result after erase-erase verify operation.

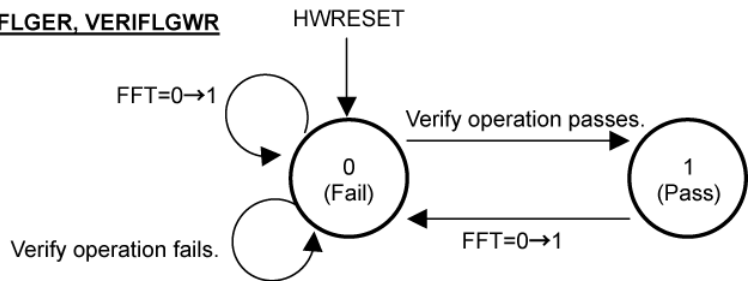
This bit is read-only bit. The data written to this bit is disregarded. When data is written to NVM, erase-verify operation is performed first after erase operation. Then, the result is returned.
Erase-verify operation passes: VERIFLGER = 1.
Erase verify operation fails: VERIFLGER = 0.

VERIFLGWR

After data is erased from NVM, this bit returns write verify result after write-write verify operation.

This bit is read-only bit. The data written to this bit is disregarded. After data has been erased from NVM, write-verify operation is performed after write operation. Then, the result is returned.
Write-verify operation passes: VERIFLGWR = 1.
Write verify operation fails: VERIFLGWR = 0.

VERIFLGER, VERIFLGWR



<table>
<tr><td>Description</td><td>TEM[0]
Sets the data output from the TE pin.
<table><tr><th>TEM[0]</th><th>TE output</th></tr><tr><td>0</td><td>Tearing Effect</td></tr><tr><td>1</td><td>Data automatically written to NVM is verified. (VERIFLGER & VERIFLGWR)
TE = 0: Verification result is NG.
TE = 1: Verification result is OK.</td></tr></table>Note: The TE pin output level is fixed to “Low” in Sleep mode and set_tear_off command is issued.</td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

set_DDB_write_control (E1h)

E1h	set_DDB write_control											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	X	1	1	1	0	0	0	0	1	E1h
1st parameter	W / R	1	X	0	0	0	0	0	0	WCIFID	WCDDB	0xh
2nd parameter	W / R	1	X	DDB0 [7]	DDB0 [6]	DDB0 [5]	DDB0 [4]	DDB0 [3]	DDB0 [2]	DDB0 [1]	DDB0 [0]	XXh
3rd parameter	W / R	1	X	DDB1 [7]	DDB1 [6]	DDB1 [5]	DDB1 [4]	DDB1 [3]	DDB1 [2]	DDB1 [1]	DDB1 [0]	XXh
4th parameter	W / R	1	X	DDB2 [7]	DDB2 [6]	DDB2 [5]	DDB2 [4]	DDB2 [3]	DDB2 [2]	DDB2 [1]	DDB2 [0]	XXh
5th parameter	W / R	1	X	DDB3 [7]	DDB3 [6]	DDB3 [5]	DDB3 [4]	DDB3 [3]	DDB3 [2]	DDB3 [1]	DDB3 [0]	XXh
6th parameter	W / R	1	X	0	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	XXh
Description	**WCDDB** WCDDB = 1: This bit enables to write data to ID1[15:0] and ID2[15:0]. Data that is set in ID1[15:0] and ID2[15:0] can be written to NVM. A8:read_DDB_continue can't write data. WCDDB = 0: This bit disables to write data to ID1[15:0] and ID2[15:0]. Set WCDDB = 0 except when data is written to NVM. **WCIFID** WCIFID = 1: This bit enables to write data to IFID[6:0]. Data that is set in IFID[6:0] can be written to NVM. A8:read_DDB_continue can't write data. WCDDB = 0: This bit disables to write data to IFID[6:0]. Set WCIFID = 0 except when data is written to NVM.											
Restriction												

NV Memory Load Control (E2h)

E2h	NV Memory Load Control											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	–	0	x	1	1	1	0	0	0	1	0	E2h
1st parameter	W / R	1	x	0	0]	LD[5]	LD[4]	LD[3]	LD[2]	LD[1]	LD[0]	XXh
Description	**LD[7:0]** Sets command to execute data load from the NV Memory during each sequence. LD[x] = 0 executes data load from the NV Memory to each command. In this case, a setting value before data load is overwritten. LD[x] = 1 does not execute data load from the NV Memory to each command. In this case, a setting value before data load is not overwritten. **Loading control commands in NV Memory Load operation** LD[0] User Command: A1h LD[1] Manufacturer Command: B3h, B6h, B8h, B9h LD[2] Manufacturer Command: C0h, C1h, C3h, C4h, C5h, C6h LD[3] Manufacturer Command: C8h, C9h, CAh LD[4] Manufacturer Command: D0h, D1h, D2h, D3h, D4h LD[5] Manufacturer Command: D5h											
Restriction												

Test mode

Test mode 13(E3h)

E3h	Test mode 13										
	W / R	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	-	0	1	1	1	0	0	0	1	1	E3h
1st parameter	R	1	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	0	0	0	0	0	0	0	0	00h
4th parameter	R	1	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameter.										

Test mode 14(E4h)

E4h	Test mode 14										
	W / R	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	-	0	1	1	1	0	0	1	0	0	E4h
1st parameter	R	1	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	0	0	1	0	0	0	1	0	22h
4th parameter	R	1	1	0	1	0	1	0	1	0	AAh
5th parameter	R	1	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameter.										

Test mode 15(E5h)

E5h	Test mode 15										
	W / R	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	-	0	1	1	1	0	0	1	0	1	E5h
1st parameter	R	1	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameter.										

Test mode 16(E6h)

E6h	Test mode 16										
	W / R	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	-	0	1	1	1	0	0	1	1	0	E6h
1st parameter	R	1	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameter.										

Test mode 17(F3h)

F3h	Test mode 17										
	W / R	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	-	0	1	1	1	1	0	0	1	1	F3h
1st parameter	R	1	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	0	0	0	1	0	0	0	1	11h
4th parameter	R	1	0	0	1	0	0	1	0	1	25h
Description	Test mode command. Do not access this command and its parameter.										

Read Mode In for DBI Only (F5h)

F5h	Read Mode In for DBI Only										
	W / R	DCX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	1	1	1	1	0	1	0	1	F5h
Description	When DBI is selected, Manufacturer Command read mode is entered. When Manufacturer command is input after this command, a parameter is output in synchronization with a falling edge of SCL. To exit the read mode, input the F6h command. In read sequence, CSX should not be raised between read command and read parameter, and between read parameters before all parameters are read. If a pause is invoked between read command and read parameter, write sequence is executed and data is overwritten.										

Read Mode Out for DBI Only (F6h)

F6h	Read Mode Out for DBI only										
	W / R	DCX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	1	1	1	1	0	1	1	0	F6h
Description	Input this command to execute the read mode entered by the F5h command.										

Test mode 18(FAh)

FAh	Test mode 18										
	W / R	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	-	0	1	1	1	1	1	0	1	0	FAh
1st parameter	R	1	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameters.										

Test mode 19(FBh)

FBh	Test mode 19										
	W / R	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	-	0	1	1	1	1	1	0	1	1	FBh
1st parameter	R	1	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameters.										

Test mode 20(FDh)

FDh	Test mode 20										
	W / R	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	-	0	1	1	1	1	1	1	0	1	FDh
1st parameter	R	1	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	0	0	0	0	0	0	0	0	00h
4th parameter	R	1	0	0	0	0	0	0	0	0	00h
5th parameter	R	1	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameters.										

Test mode 21(FEh)

FEh	Test mode 21										
	W / R	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Command	-	0	1	1	1	1	1	1	1	0	FEh
1st parameter	R	1	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	0	0	0	0	0	0	0	0	00h
4th parameter	R	1	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameters.										

Reset

The R61529 is set to its internal initial setting during a reset period initiated by a RESET input. During the RESET period, no command is accepted from the host processor. The source driver unit and the power supply circuit unit are also reset to the respective initial states when RESET signal is input to the R61529.

Command Default Values

The default values of commands are shown in the “Default Modes and Values” table in Command List. See “Default Modes and Values.” The command setting is initialized to the default value when a Hardware Reset is executed.

Table 49 Initial State of Input/Output pins (T.B.D.)

Pin name	Input/Output Pin Initial State	Pin name	Input/Output Pin Initial State
VDD	1.5V	C11P	VCI
VREFM	-1.5V	C11M	GND
VSP	VCI	C12P	VCI
VSN	GND	C12M	GND
VPLVL	GND	C13P	VCI
VNLVL	GND	C13M	GND
VCL	GND	C14P	VCI
VGH	VCI	C14M	GND
VGL	GND	C21P	VCI
		C21M	GND
		C22P	VCI
		C22M	GND
VGS	GND	C23P	VCI
VCOMDC	GND	C23M	GND
VCOM	GND	C24P	VCI
S1-S960	GND	C24M	GND
G1-G480	GND	C41P	VCI
		C41M	GND
		C42P	VCI
		C42M	GND
DB23-DB0	Hi-Z		
DIN	Hi-Z		
DOUT			
TE	GND		
LEDPWM	GND		

Frame Memory

The frame memory retains image data of up to 3,686,400 bits (480 x 320 x 24 bits).

Address Mapping from Memory to Display

Normal Display On or Partial Mode On

In this mode, a content of the frame memory within an area where column pointer is 0000h to 13F and page pointer is 0000h to 1DF is displayed.

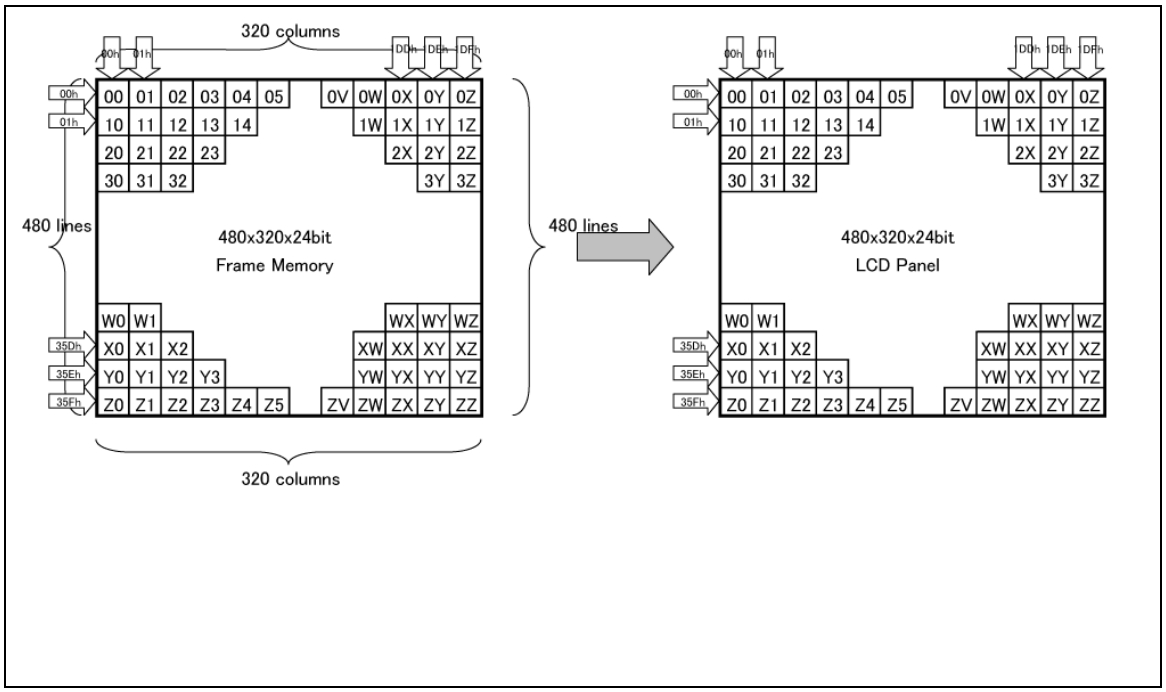


Figure 117

Write/Read Direction from/to Host Processor

Below figure illustrates data stream from the host processor.

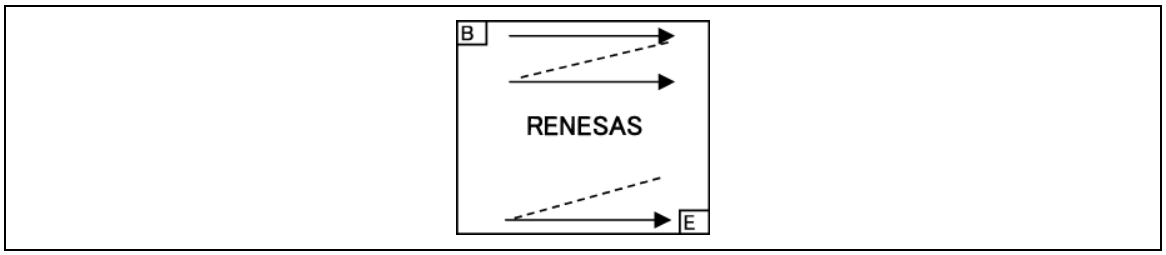


Figure 118

The data is written in the order illustrated above. The Counter which dictates write position on the physical memory is controlled by "set_address_mode (36h)" command Bits B5, B6, B7 as illustrated below.

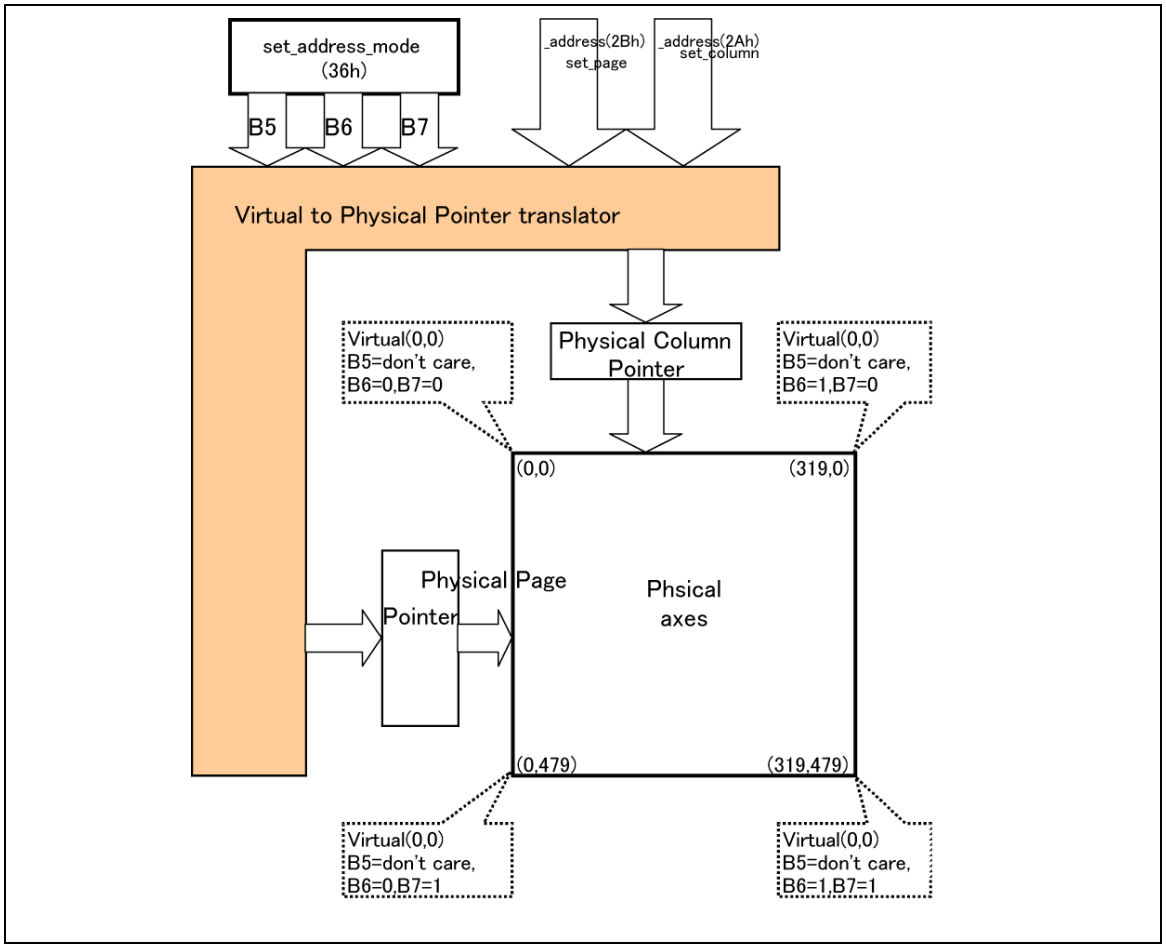


Figure 119

Table 50

B5	B6	B7	Column Address	Page Address
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (479-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (479-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (479-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (479-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

For each image orientation, the controls on the column and page counters apply as below.

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by set_address_mode (36h) bits B7, B6 and B5. The write order for each pixel unit is as follows.

Table 51

D23	D22	D21	D20	D19	D18	D17	D16
R7	R6	R5	R4	R3	R2	R1	R0

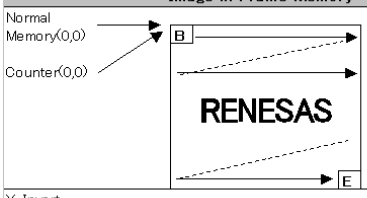
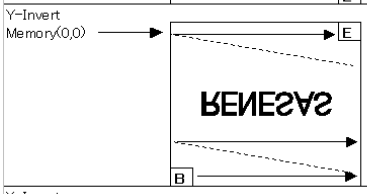
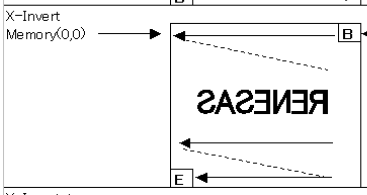
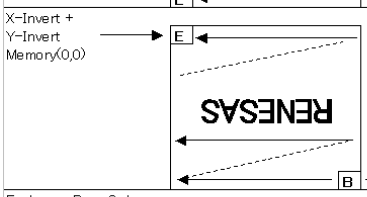
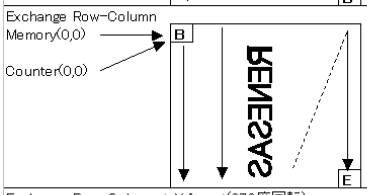
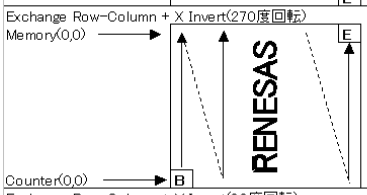
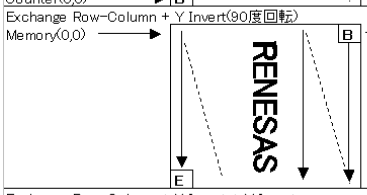
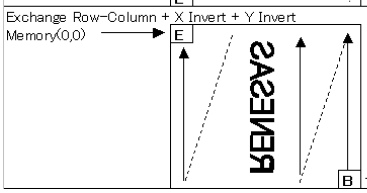
D15	D14	D13	D12	D11	D10	D9	D8
G7	G6	G5	G4	G3	G2	G1	G0

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

Table 52 Address pointer (counter) operation

Condition	Column counter	Page counter	Note
When commands write_memory_start (2Ch) and read_memory_start (2Eh) are received.	Back to Start Column	Back to Start Page	
Execute Pixel Read/Write	Increment by 1	No change	
When column counter value is larger than ”End Column”	Back to Start Column	Increment by 1	
When column counter value is larger than ”End Column” and page counter value is larger than “End Page”	STOP	STOP	Entry Mode(B3h) WEMODE=0
	Back to Start Column	Back to Start Page	Entry Mode(B3h) WEMODE=1

One pixel unit represents 1 column and 1 page counter value on the Frame Memory. See the next page for the resultant image for each orientation setting.

Image in Frame Memory	B5	B6	B7
	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0
	1	0	1
	1	1	0
	1	1	1

Only B5=0 can be used in DSI

Figure 120

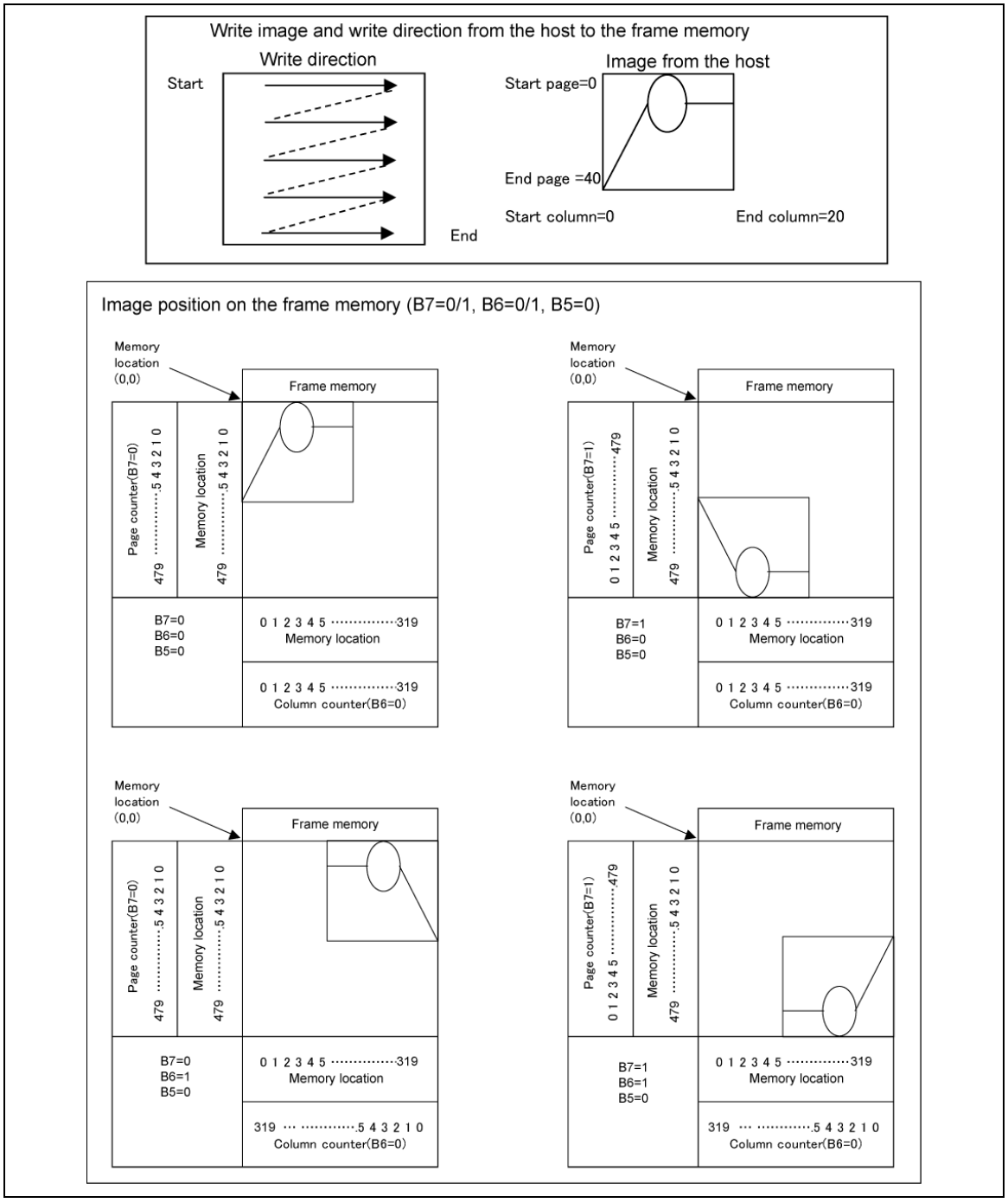


Figure 121

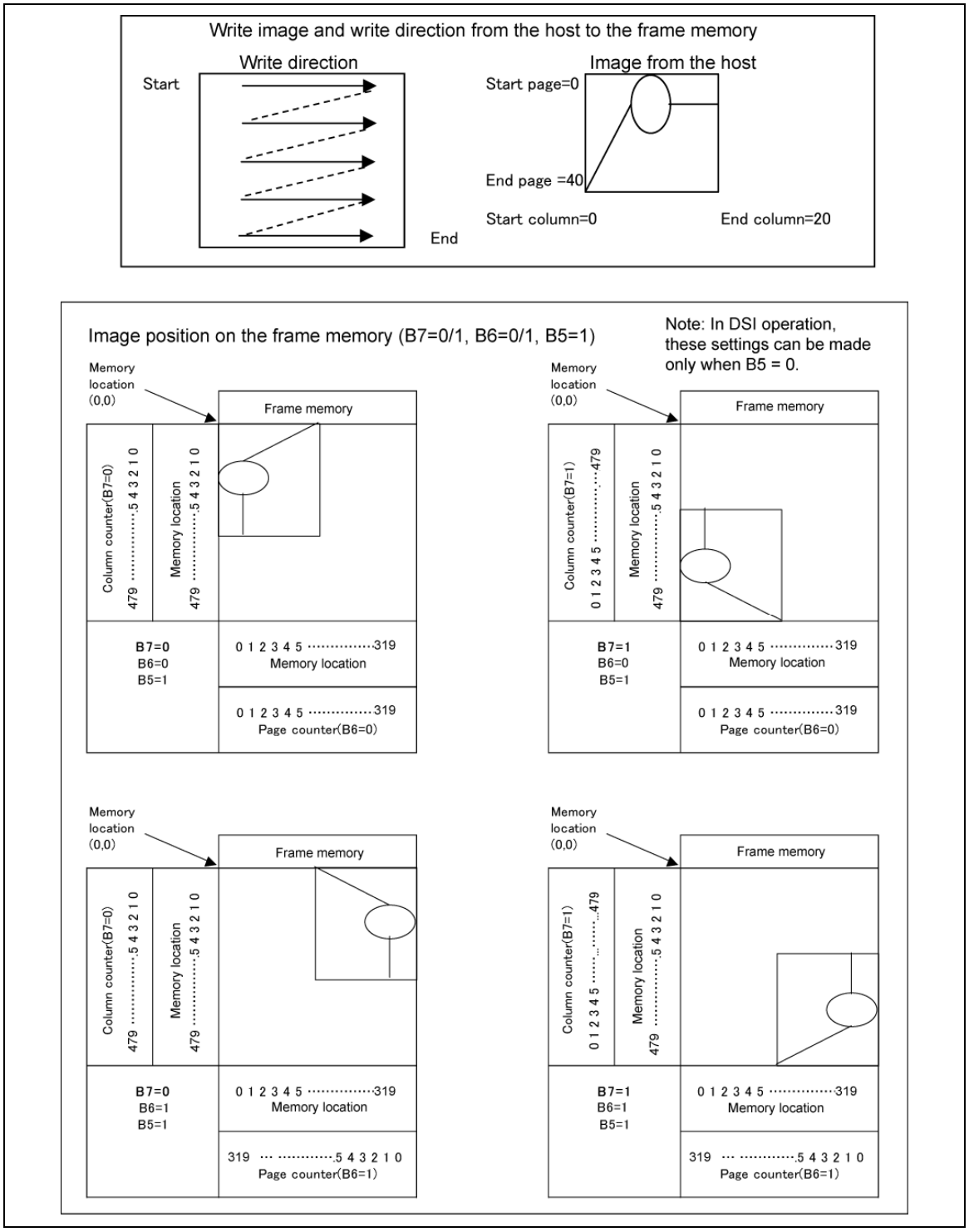


Figure 122

Internal reference clock generating function (T.B.D.)

Scan Mode Setting

The R61529 allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the R61529 and the LCD panel.

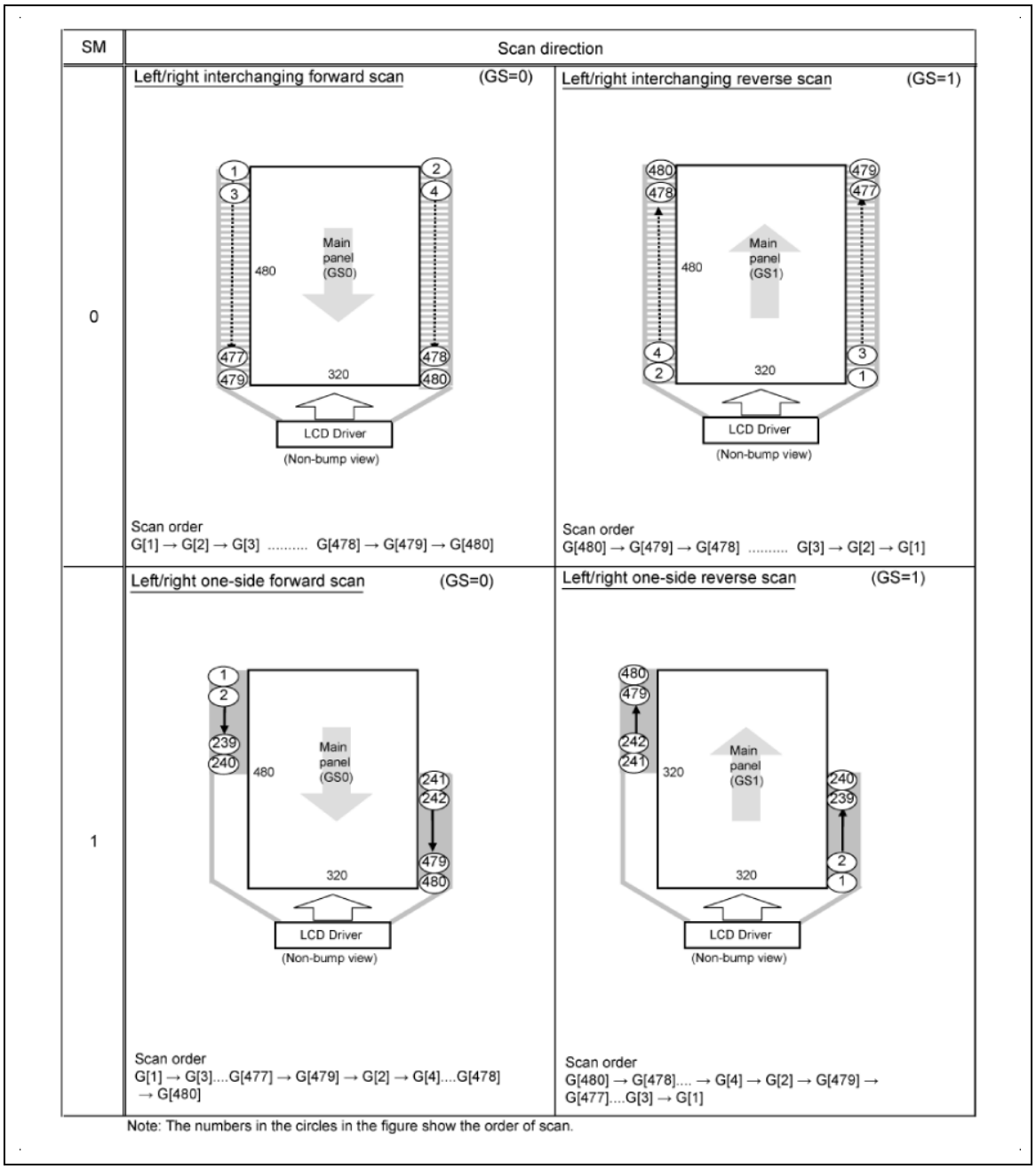


Figure 123

Frame Frequency Adjustment Function

The R61529 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting Display Timing Setting (RTN bits) without changing the oscillation frequency.

It is possible to set a low frame frequency for saving power consumption when displaying a still picture and set a high frame frequency when displaying video image.

Also, the R61529 has frame-frequency adjustment parameters which can set frame frequency according to display modes (Normal, partial and Idle modes).

Relationship between the Liquid Crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following equation. The frame frequency can be changed by setting the number of clocks per 1 line period (RTN).

Equation for calculating frame frequency

$$FrameFrequency = \frac{osc}{Number\ of\ Clocks/line \times (NL + FP + BP)}[Hz]$$

fosc: Internal operation clock frequency (14MHz)
Number of clocks per line: RTN
Line: number of lines to drive the LCD: NL
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when Maximum Frame Frequency = 60 Hz

OSC : fosc / 12 = 1.16Hz (DIV[3:0] = 4'h7 (an example of Divider setting: 1/12))
Number of lines: 480 lines
1H period: 39 clock cycles (RTN = 6'h27)
Front porch: 8 lines
Back porch: 8 lines

$$\therefore f_{FLM} = \frac{14MHz}{39clocks \times \frac{1}{12} \times (480 + 8 + 8)} \approx 60Hz$$

In the conditions described here, the frame frequency can be changed as follows by setting RTN

TE Pin Output Signal

Tearing Effect Line signal can be output from TE pin as frame memory data transfer synchronous signals. TE signal is trigger for frame memory write operation to enable data transfer in synchronization with the scanning operation. Tearing Effect Output signal is turned on/off by set_tear_off (34h) and set_tear_on (35h) commands.

Table 53

TEON (represents status of 35h command)	TELOM (35h1st parameter)	TE pin output
0	*	GND
1	0	TE (Mode1)
1	1	TE (Mode2)

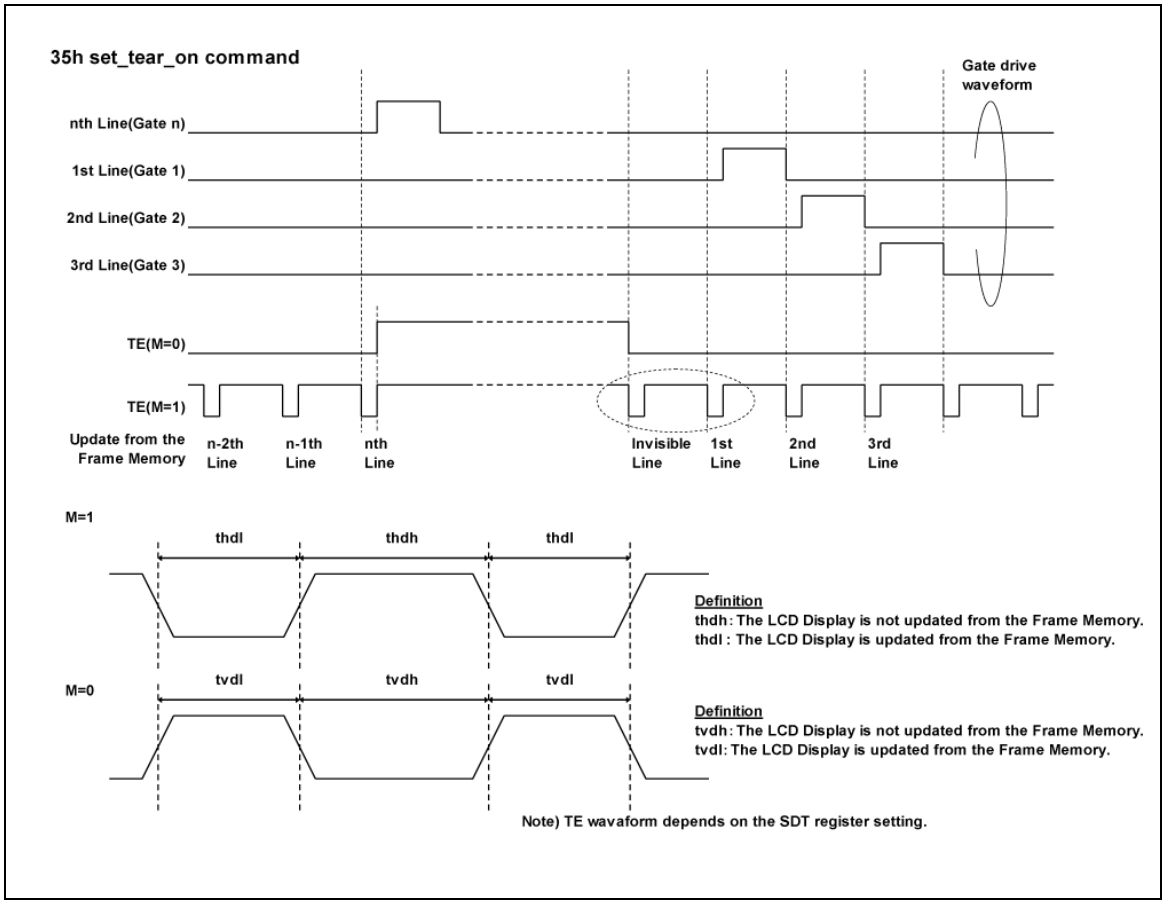


Figure 124

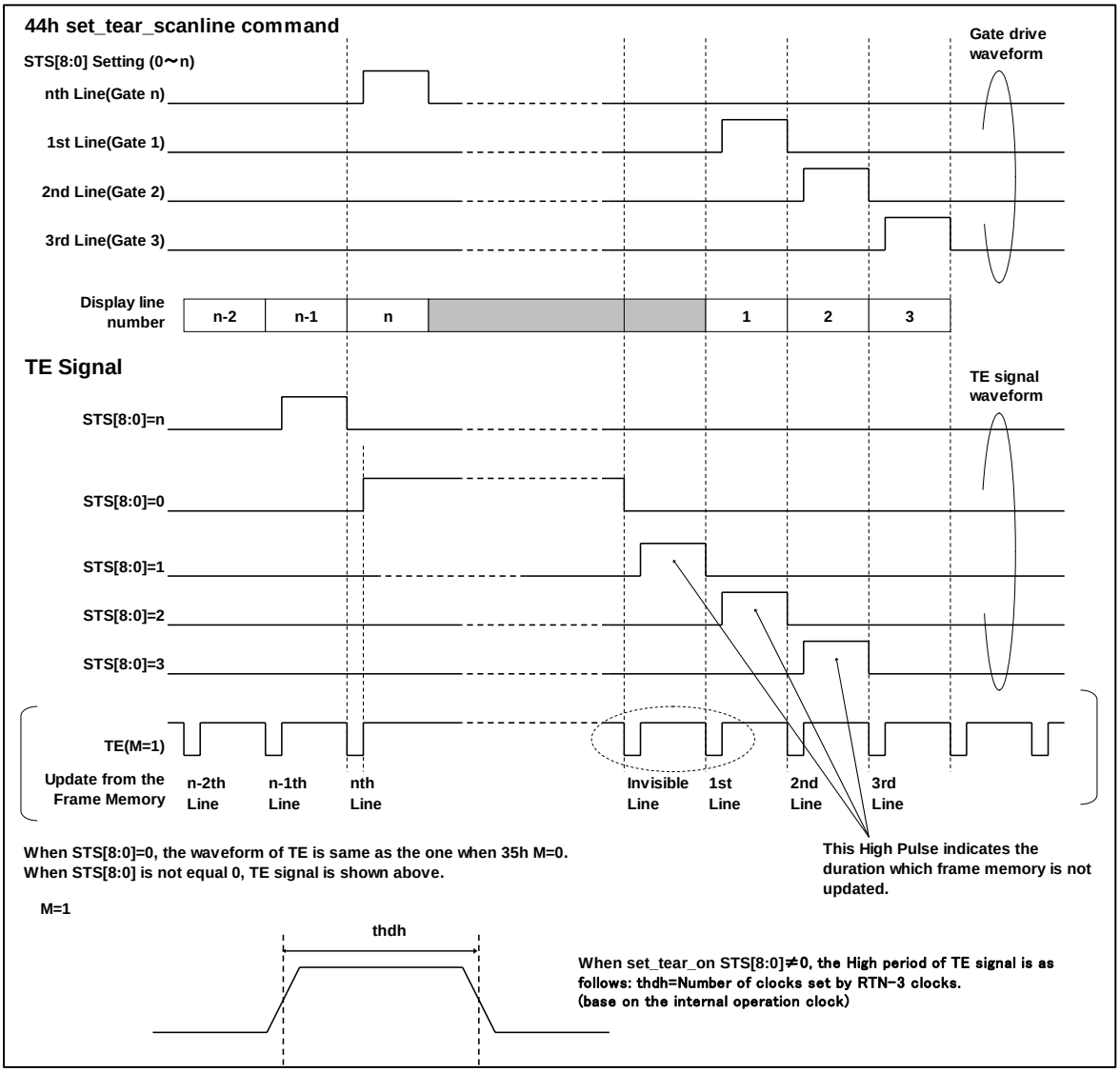


Figure 125

Self-Diagnostic Functions (T.B.D.)

The R61529 supports the self-diagnostic functions. Set get_diagnostic_result (0Fh) 1st parameter's D6 bit according to the following flow chart.

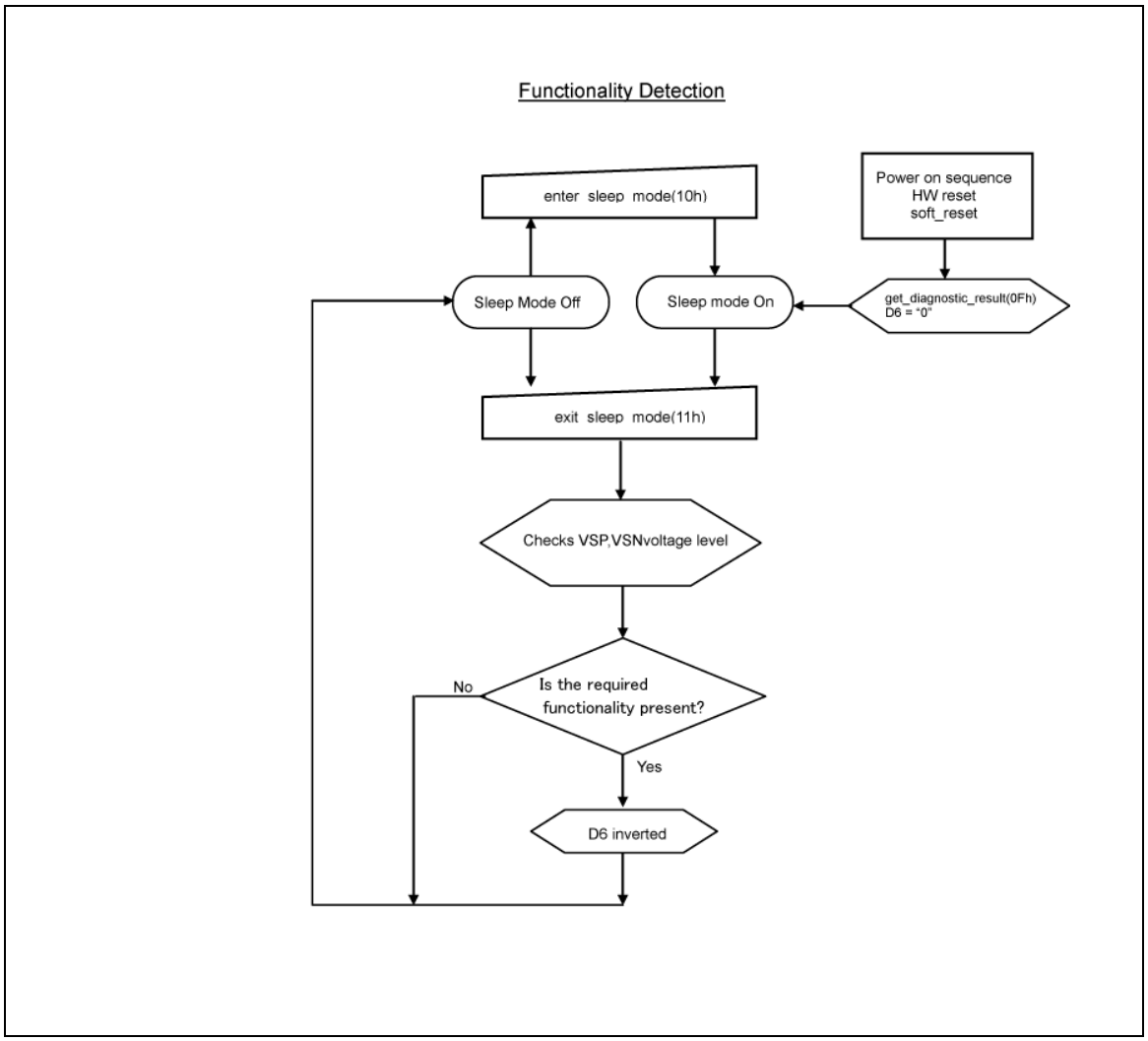


Figure 126 Functionality Detection

Dynamic Backlight Control Function (T.B.D.)

The R61529 supports BLC (backlight control) function to control backlight brightness and process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image.

The display image is dynamically controlled by the BLC function. The availability of this function ranges from moving pictures such as TV image to still pictures such as menu. The histogram of display data is analyzed by BLC function, according to the brightness range of backlight set by parameters. The brightness of backlight and image processing coefficient are calculated so that image data is optimized. Backlight power is reduced without changing display image.

Notes: 1. The BLC setting is enabled by BLCON bit setting (B8h).
2. The effects of BLC function on power efficiency and display quality depend on image data and the setting. Check display quality on the panel.

- Control backlight dynamically according to the image histogram.
- PWM pin for LED backlight adjustment
- PWM signal control register set by the host processor. Backlight dimmer is adjusted by calculating internally-decided PWM value and maximum PWM value from the host processor.

System Configuration

1. The PWM signal is used to directly control the R61529 and LED driver IC. The LED driver IC is controlled entirely via the R61529.

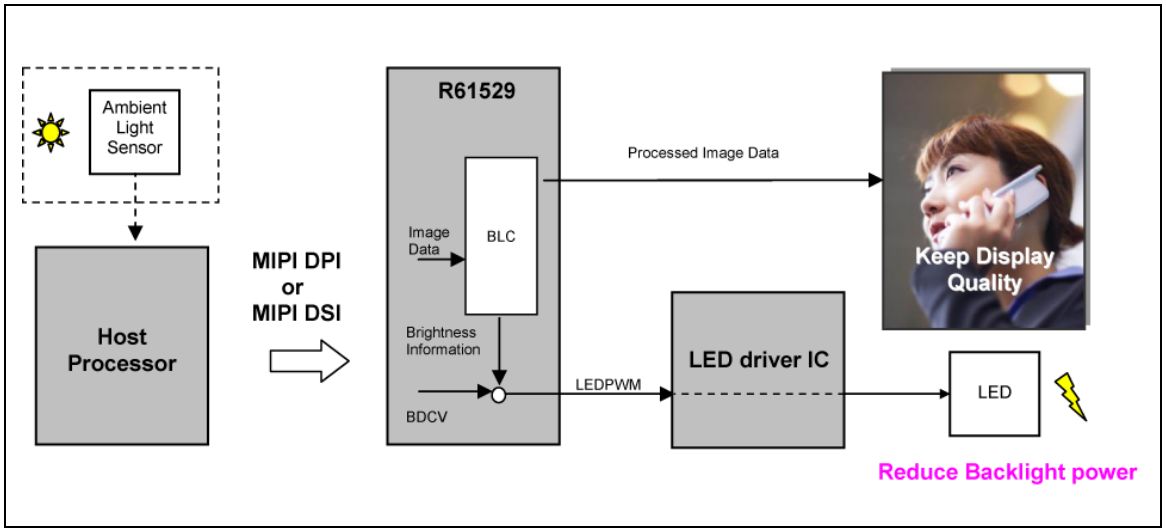


Figure 127

2. The host processor reads LED brightness information internally generated by BLC processing from the R61529 via MIPI DSI. Then, the LED driver IC is controlled from the host processor. There is the time difference between brightness adjustment by PWM and displaying data processed from the R61529. Check the effect on the image.

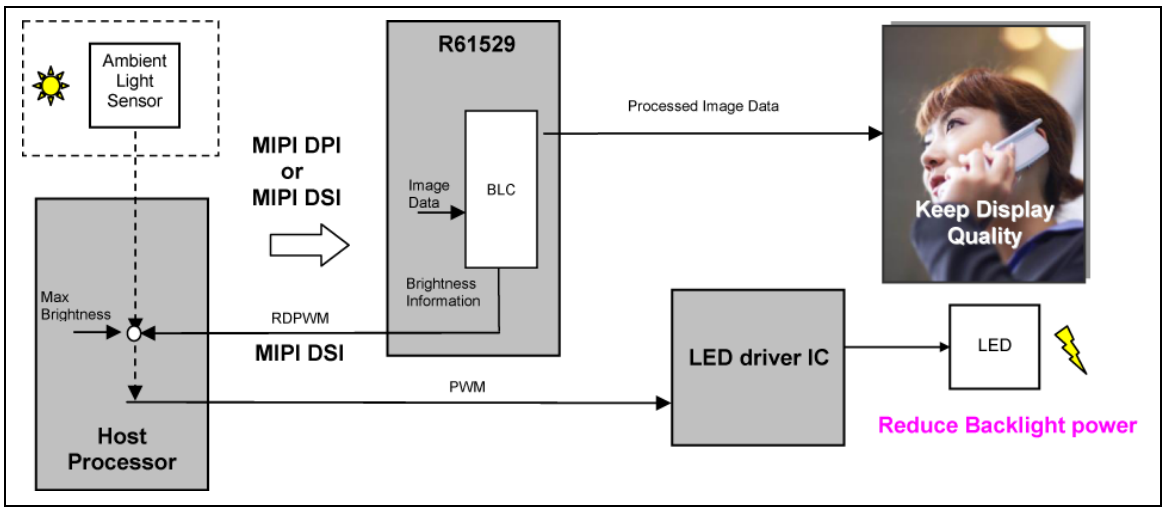


Figure 128

BLC Parameter Setting

The backlight control function has the following two functions:

- Image processing and backlight control processing
- Retain the grayscale of the display image that has turned white

These functions are set by the following registers:

(1) BLC operating threshold (THREW)

(2) Amount of change of threshold grayscale value per frame (PITCHW)

(3) Difference between two grayscale values counted by the histogram counter (CGAPW)

(4) Backlight brightness adjustment range (ULMTW and LLMTW)

(5) Gamma conversion table (TBL_MIN and TBLx[7:0])

(6) Interpolation to prevent display image from turning white (COEFK)

(1) THREW[4:0]

This parameter sets the ratio (percentage) of the maximum number of pixels that makes display image white (= data 255) to the total of pixels by image processing. The ratio can be set from zero percent to sixty two percent in units of two percent. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (Dth) that makes display image white is set so that the number of the pixels set by this parameter does not change.

To reduce the power by about 30 percent, set the above ratio to thirty percent (THREW = 5'h0F). When the value set by this parameter exceeds the range of Dth to be mentioned later, the priority is given to the range of threshold grayscale value (Dth).

According to the relationship between threshold grayscale value (Dth) and gamma conversion table (see (5)), the rate of backlight brightness reduction (= the rate of power reduction) and image correction factor are set.

- The larger THREW value tends to enhance the effect of reducing backlight power, and increases the image correction factor. In this case, the effect on display image increases (See note 1).
- The smaller THREW value tends to reduce the effect of reducing backlight power, and decreases the image correction factor. In this case, the effect on display image decreases (See note 1).

Notes: 1. The tendency for backlight power reduction and the effect on image by BLC function depend on image data. Check display quality on the panel.
2. The result of the histogram analysis is enabled from the next frame.

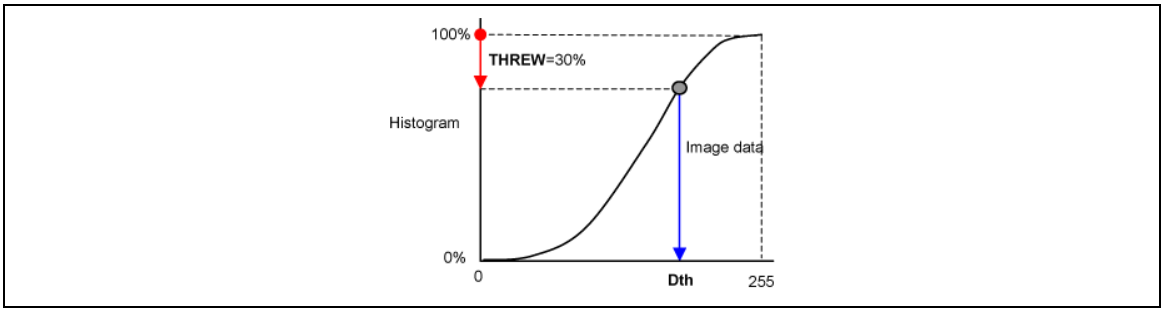


Figure 129

(2) PITCHW[3:0]

This parameter sets the amount of change of threshold grayscale value (Dth) that makes display image white per frame in units of one eighth of the grayscale. When the target (Dth) is changed by the histogram change of input image including video image, this parameter can adjust the amount of changing threshold grayscale value (Dth). Therefore, this parameter is effective in reducing sharp change of backlight brightness. Make sure that CGAPW[4:0] ≥ PITCHW[3:0].

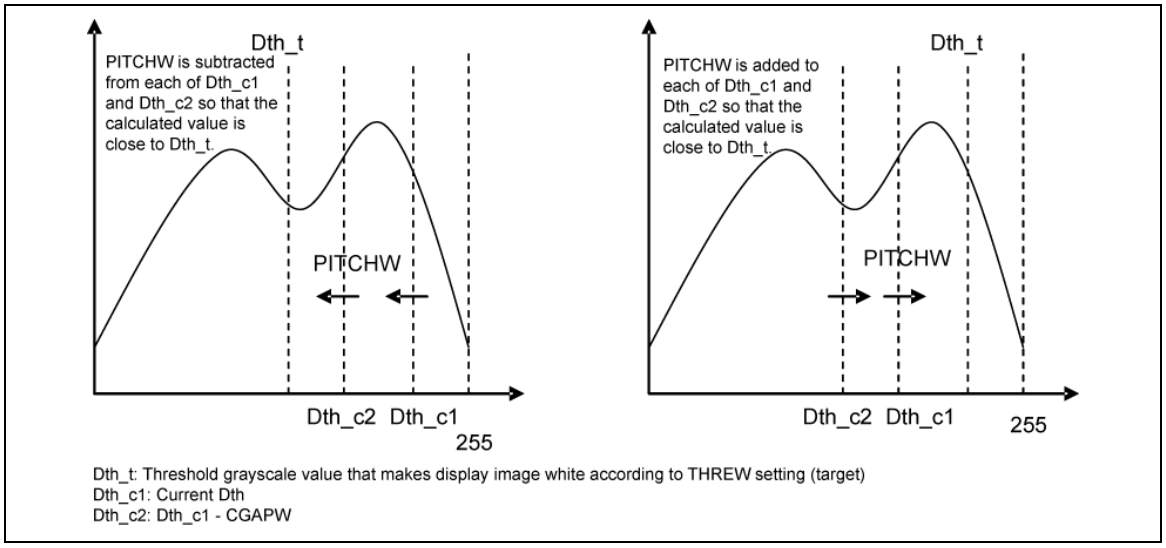


Figure 130

(3) CGAPW[4:0]

The difference of the two grayscales (Dth_c1 and Dth_c2) counted by the present threshold counter is set in units of one eighth of the grayscale. This parameter is effective in slowing the change of threshold grayscale value (Dth). So, the speed of the change of Dth is adjusted to reduce subtle changes and flickers. Make sure that CGAPW[4:0] ≥ PITCHW[3:0].

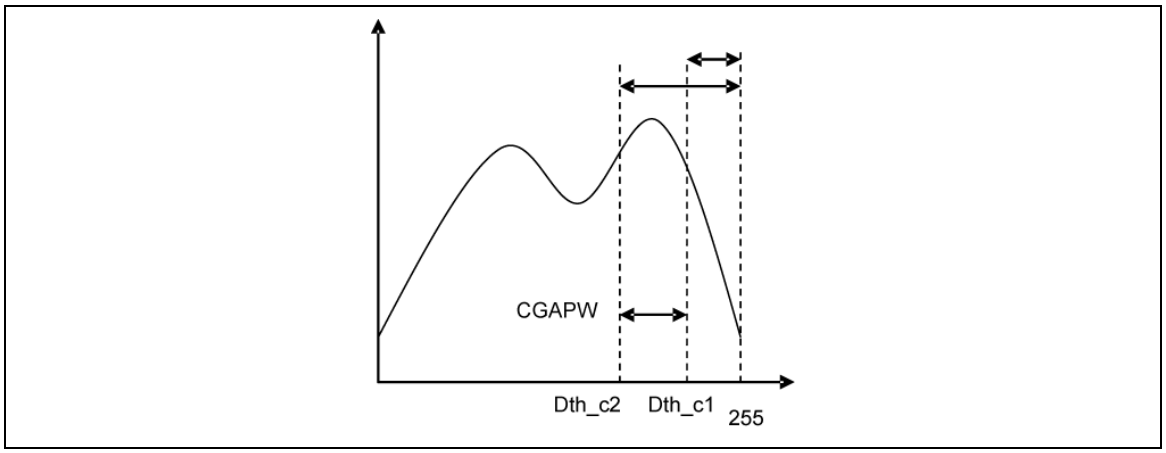


Figure 131

(4) ULMTW[7:0], LLMTW[7:0]

The possible range of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale. ULMTW and LLMTW set the maximum grayscale and the minimum grayscale, respectively. Dth can be changed within the range set by ULMTW and LLMTW.

When there is no effect on saving power consumption due to a large number of pixels displaying white color, that is, in cases such as GUI, the R61529 can save power consumption by setting ULMTW lower than the maximum grayscale if saving power consumption precedes the display quality.

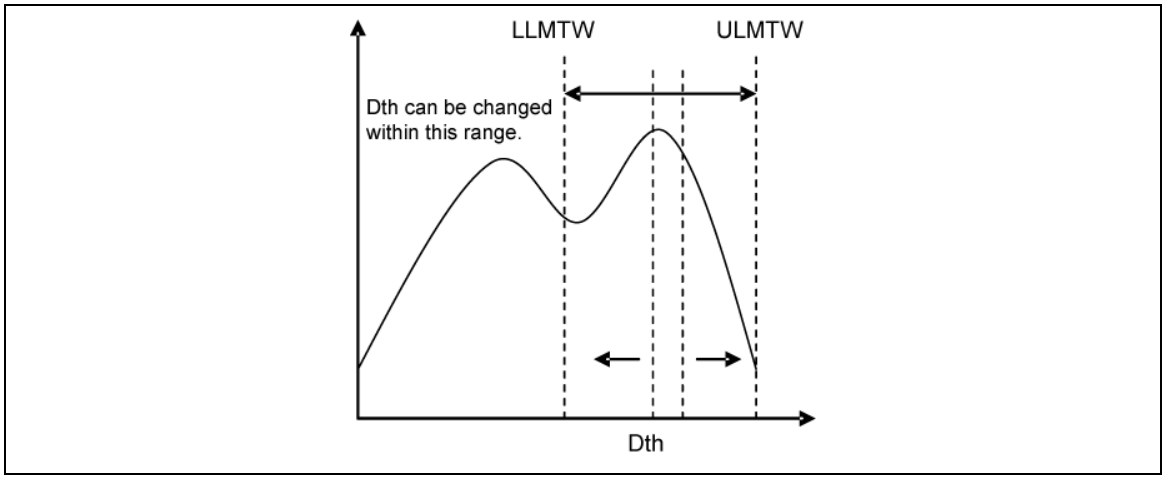


Figure 132

(5) TBL_*[7:0]

The reference values used for interpolation calculation in the gamma conversion table are set by 8-bit TBL_*[7:0]. Interpolation is performed as follows: First, four grayscale values are specified by TBL_*[7:0]. Then, the output data corresponding to the input data to thirty one grayscale values specified at even interval between the adjacent two grayscale values of the four grayscale values specified by TBL_*[7:0] is calculated by linear interpolation.

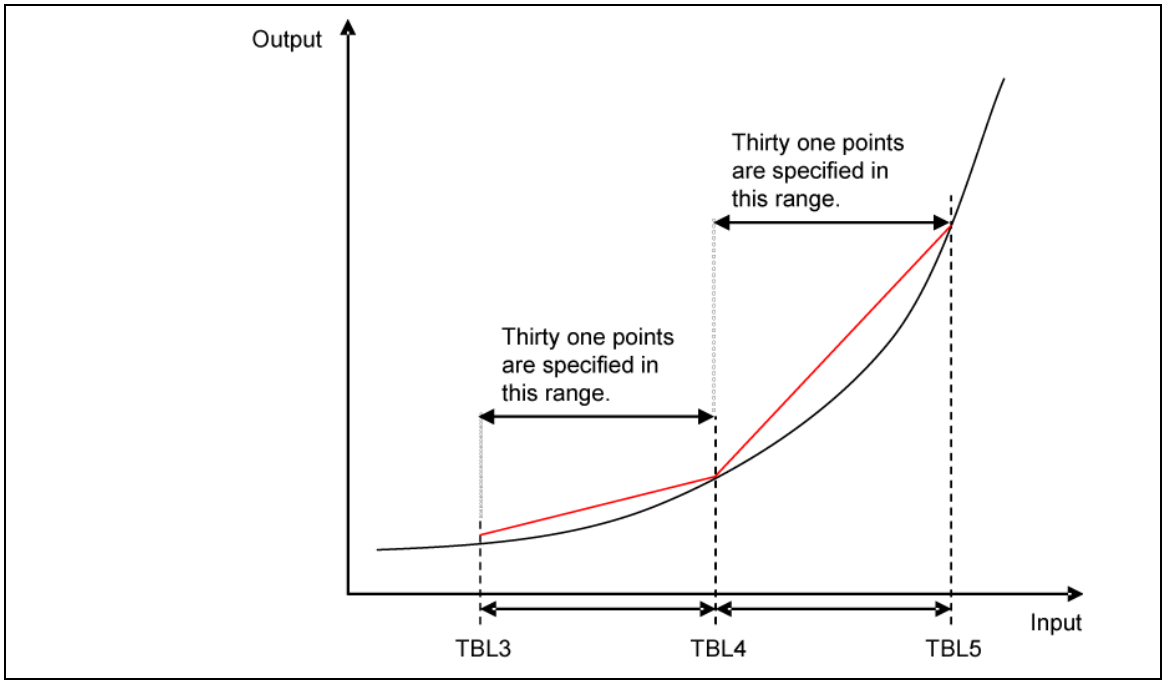


Figure 133

The table setting value is calculated by the following formula according to panel gamma value.

Table setting value = 255 x (table input grayscale / 255) ^ gamma

As the input table grayscale, the above calculation formula is applied to grayscales 127, 159, 191, and 223 to calculate the table values. The values are set as TBL*. The following table is applied to the case that gamma is set to 2.2.

Table 54

Register	TBL3	TBL4	TBL5	TBL6
Table input grayscale	127	159	191	223
Table setting value	55	90	135	190

(6) COEFK[4:0]

This register sets the range of the grayscale that prevents display image from turning white, according to the ratio of the grayscale to the grayscale number that makes data white. The ratio can be set from 0 percent to 100 percent. The first grayscale (S) that starts grayscale interpolation to prevent display image from turning white is calculated by this register and Dth. Then, the number of grayscales between this grayscale (S) and the maximum grayscale is calculated by interpolation function, and it is used as image processing pixel value.

The larger COEFK[4:0] setting value increases the number of grayscales available for interpolation and relatively decreases the contrast between interpolation sections. As a result, the gamma value changes and the brightness decreases. Also, the color of the section changes. In the interpolation factor, there is a trade-off between contrast between interpolation section and the interpolation that the gamma value changes.

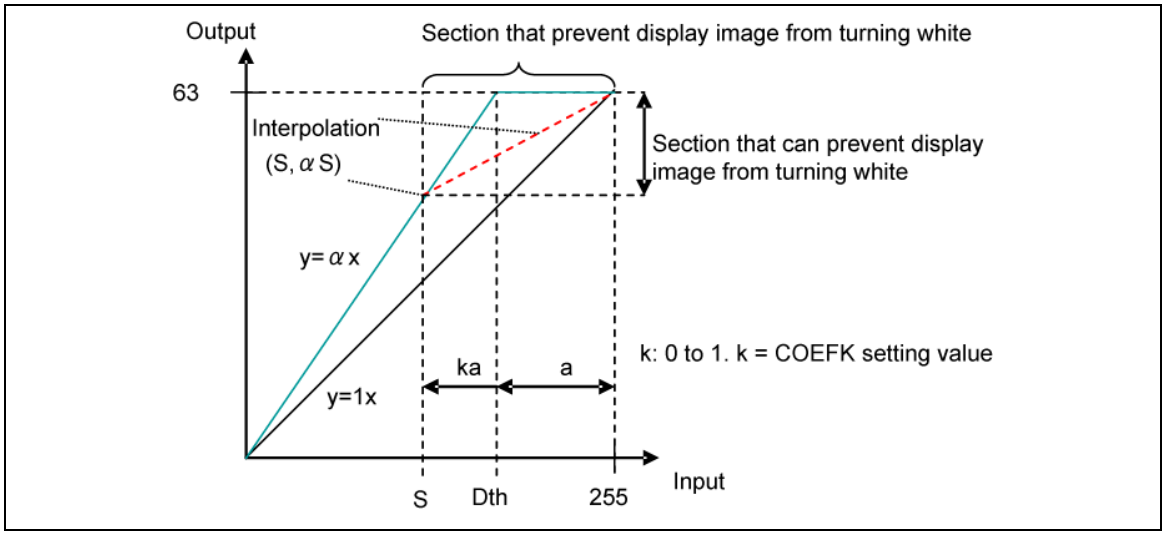


Figure 134

PWM Signal Setting

The PWM signal is output from the LEDPWM pin according to BDCV[7:0] bit settings and brightness information (8 bits) output from BLC control circuit.

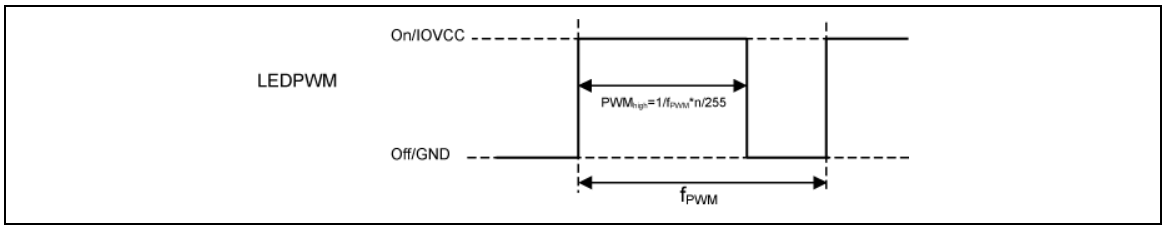


Figure 135 PWM output

Below setting is applied to interfaces except MIPI DPI.

Table 55

PWMDIV[7:0]	LEDPWM frequency
8'h00	33.3KHz see Note 2
8'h01	27.4KHz
8'h02	18.3KHz
8'h03	13.7KHz
8'h04-8'h06	Setting inhibited
8'h07	6.86KHz
8'h08-8'h0E	Setting inhibited
8'h0F	3.43KHz

PWMDIV[7:0]	LEDPWM frequency
8'h10-8'h1E	Setting inhibited
8'h1F	1.72KHz
8'h20-8'h3E	Setting inhibited
8'h3F	0.86KHz
8'h40-8'h7E	Setting inhibited
8'h7F	0.43KHz
8'h80-8'hFE	Setting inhibited
8'hFF	0.21KHz

Note: 1. The values in the table above show the typical. There shall be variance of maximum +/-5% in the actual operation.

2. Dimmer control is applied to 210/255 level at maximum when PWMDIV=8'h00 (33.3kHz).

Below setting is applied to MIPI DPI interface.

Table 56

PWMDIV[7:0]	LEDPWM frequency
8'h00	PWMCYC×1
8'h01	PWMCYC×2
8'h02	PWMCYC×3
8'h05	PWMCYC×6
8'h0B	PWMCYC×12
8'h17	PWMCYC×24
8'h2F	PWMCYC×48
8'h5F	PWMCYC×96
8'hC5	PWMCYC×198
8'hFF	PWMCYC×256
Others	Setting inhibited

PWMCYC = (PWMDIV + 1) x 255 x clock frequency (T.B.D.)

MIPI DPI: clock cycle = PCLK/4
MIPI DSI (2 lanes): clock cycle = DSICLK/32
MIPI DSI (1 lane): clock cycle = DSICLK/48

Table 57

Dimming data	$Duty_{PWM}$
8'h00	0(fixed Low)
8'h01	1/255
8'h02	2/255
8'h03	3/255
: :	: :
8'h0D	253/255
8'h0E	254/255
8'hFF	1(fixed High)

Privacy filter mode (T.B.D.)

R61529 supports a function which changes the brightness of panel according to view angle.

This function can be executed by setting xx bits of xxh command to 1.

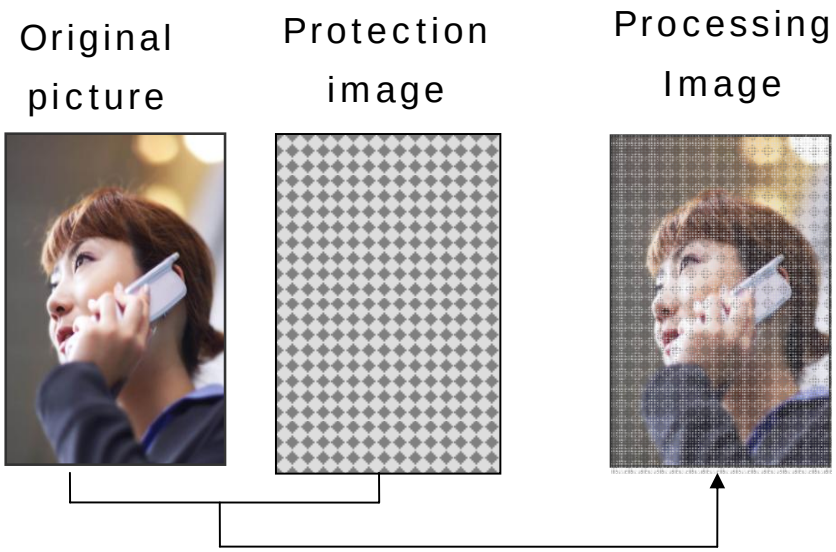


Figure 136

State Transition Diagram (Display Mode)

Definition of Display Modes

The state transition of the R61529 (display modes) compliant with MIPI DCS is as follows:

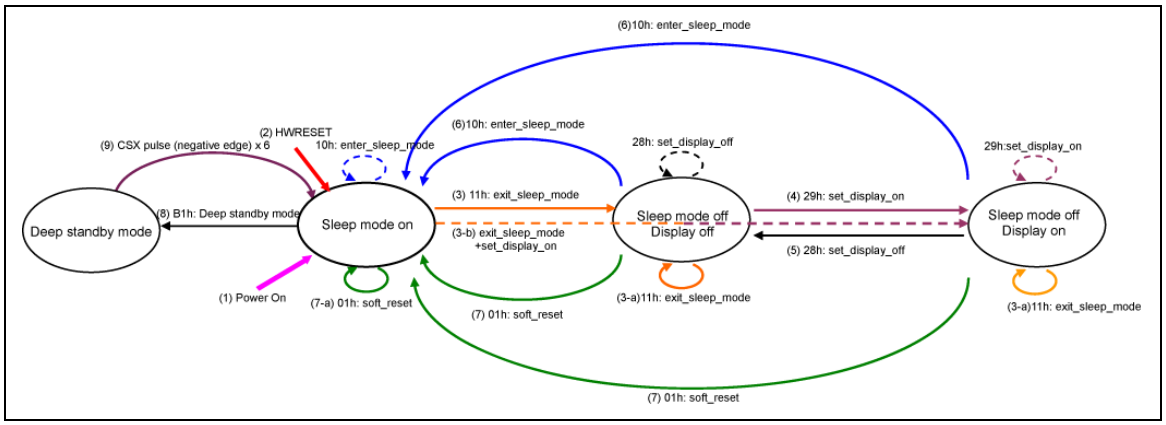


Figure 137

Table 58 Operation Mode Transition Sequence

Sequence		Command	State	
			From	To
(1)	Power On sequence	-	-	Sleep mode on
(2)	HWRESET sequence	-	-	Sleep mode on
(3)	exit_sleep_mode sequence	11h:exit_sleep_mode	Sleep mode on	Sleep out Display off
(3-a)			Sleep mode off Display off/on	Sleep mode off Display off/on
(3-b)	exit_sleep_mode + display_on sequence	11h:exit_sleep_mode	Sleep mode on	Sleep mode off Display on
(4)	set_display_on sequence	29h:set_display_on	Sleep mode off Display off	Sleep mode off Display on
(5)	set_display_off sequence	28h:set_display_off	Sleep mode off Display on	Sleep mode off Display off
(6)	enter_sleep_mode sequence	10h:enter_sleep_mode	Sleep mode off Display off/on	Sleep mode on
(7)	soft_reset sequence	01h:soft_reset	Sleep out Display off/on	Sleep mode on
(7-a)			Sleep mode on	Sleep mode on
(8)	Deep standby mode sequence	Manufacturer Command B1h: Deep standby mode	Sleep mode on	-
(9)	Exit_Deep standby mode_sequence	CSX x6, HWRESET-	-	Sleep mode on

Power On/Off Sequence

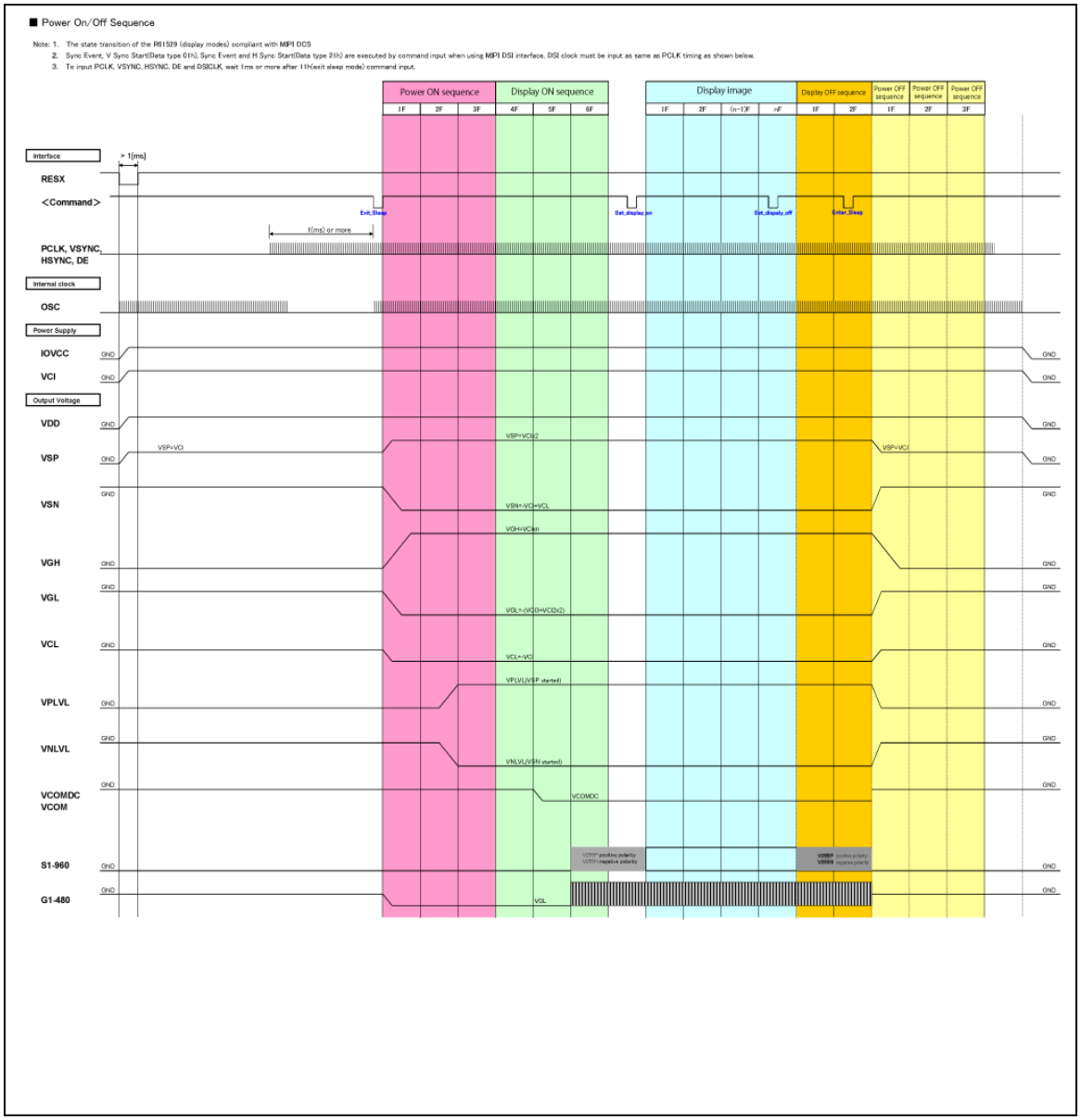


Figure 138

Power/Display On Sequence

The power/display on sequence is shown below.

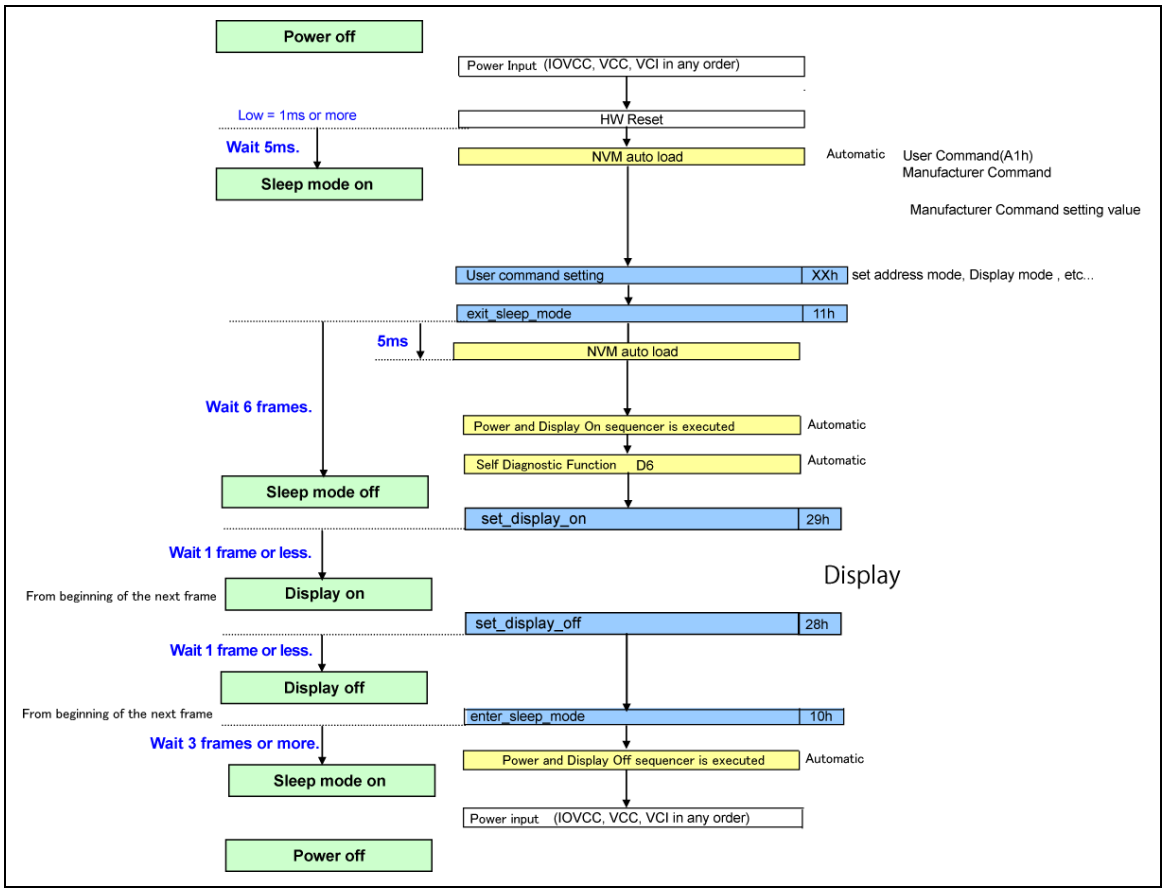


Figure 139

Note: Calculation Example of Waiting Time

1/60Hz = 16.6ms when the driver is used at frame frequency of 60Hz.

Wait for the above frame(s) or ms.

Power/Display On/Off Sequence when using MDDI interface

The power/display on sequence when using MDDI interface is shown below.

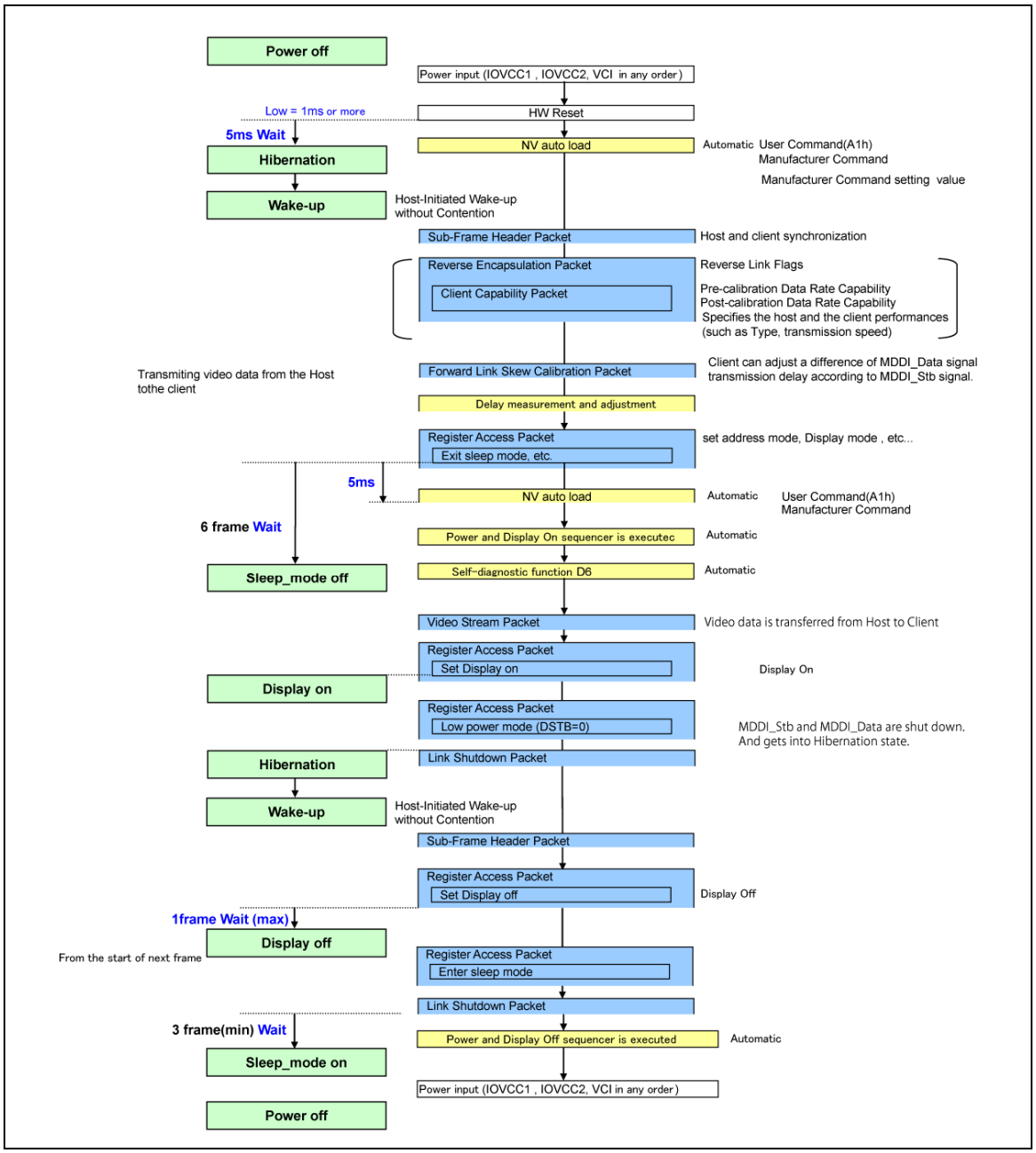


Figure 140

Gamma Correction Function

The R61529 supports γ-correction function to make the optimal colors according to the characteristics of the panel. The R61529 has registers for positive and negative polarities to allow different settings for R, G, and B dots.

γ Correction Circuit

The following figure shows a gamma correction circuit. Two ends of the 168-step ladder resistors for positive grayscale are connected to VPLVL and VGS. Those for negative grayscale are connected to VGS (GND) and VNLVL. The voltage of the level of which is evenly divided by the ladder resistors. The divided voltage is selected by selectors. The selected voltage is output via amplifiers as 12 grayscale reference voltages (V0, V4, V8, V15, V31, V79, V176, V224, V240, V247, V251, and V255). The other grayscale voltages are generated by interpolation circuits. Grayscale voltages V16 to V239 are linearly interpolated. The other grayscale voltages are nonlinearly interpolated. For details, see “Grayscale Voltage Calculation Formula”.

The 61529 incorporates RGB separate gamma correction function. There are three circuits of R, G and B in parallel behind selectors.

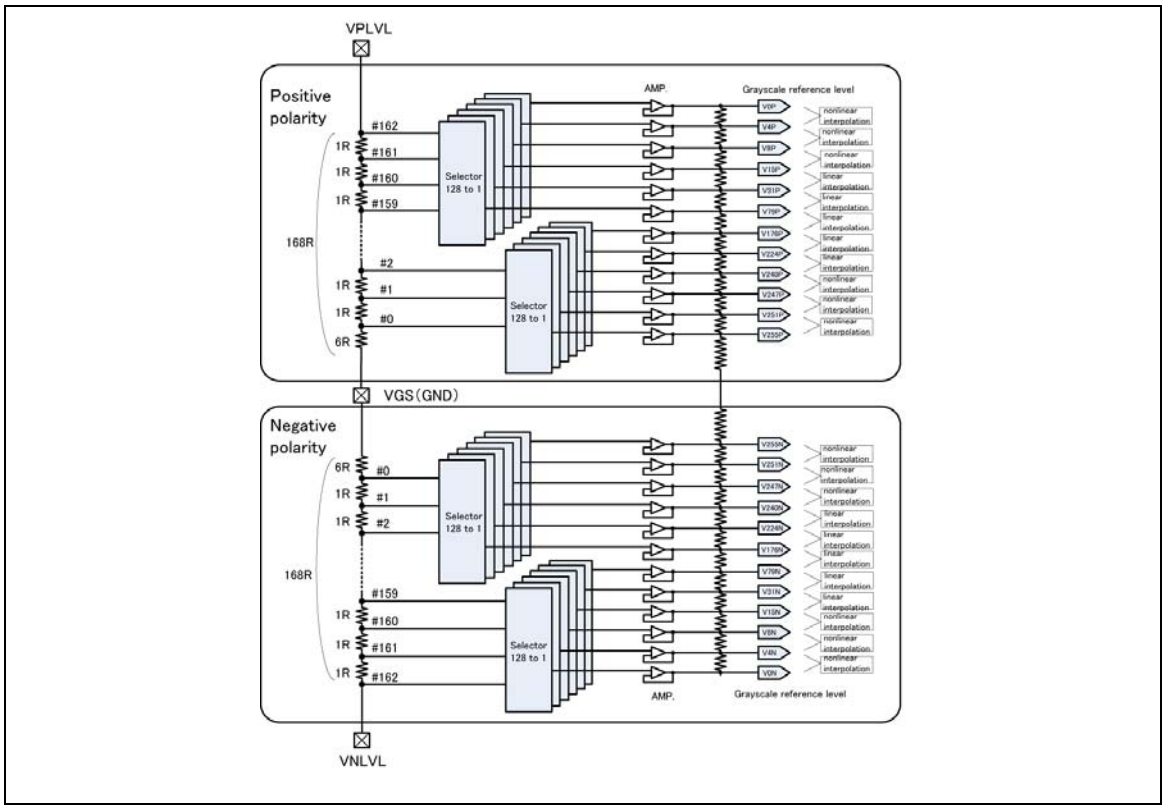


Figure 141

γ Correction register

The following table shows the γ-correction register and grayscale reference level. Each reference level is set by 7-bits register. Both positive and negative polarities are consisted by 84bits (7-bits x12 points).

Table 59

Grayscale reference level	γ correction register	
	Positive polarity	Negative polarity
V0	GSELxP0[6:0]	GSELxN0[6:0]
V4	GSELxP1[6:0]	GSELxN1[6:0]
V8	GSELxP2[6:0]	GSELxN2[6:0]
V15	GSELxP3[6:0]	GSELxN3[6:0]
V31	GSELxP4[6:0]	GSELxN4[6:0]
V79	GSELxP5[6:0]	GSELxN5[6:0]
V176	GSELxP6[6:0]	GSELxN6[6:0]
V224	GSELxP7[6:0]	GSELxN7[6:0]
V240	GSELxP8[6:0]	GSELxN8[6:0]
V247	GSELxP9[6:0]	GSELxN9[6:0]
V251	GSELxP10[6:0]	GSELxN10[6:0]
V255	GSELxP11[6:0]	GSELxN11[6:0]

Note: “X” in register name indicates “A” of “Gamma Setting A Set”, “B” of “Gamma Setting B Set,” or “C” of “Gamma Setting C Set.”

The relationship between γ Correction register setting and select level (Reference level select table)

The following table shows the relationship between γ-correction register setting and select level.

Table 60

Register	Register setting value	Grayscale reference level to be selected	Select level
GSELxP0[6:0] GSELxP1[6:0] GSELxP2[6:0] GSELxP3[6:0] GSELxP4[6:0] GSELxP5[6:0]	7'h00	#162	ΔV× (1-0/168)
	7'h01	#161	ΔV× (1-1/168)
	7'h02	#160	ΔV× (1-2/168)
	7'h03	#159	ΔV× (1-3/168)
	7'h04	#158	ΔV× (1-4/168)
	7'h05	#157	ΔV× (1-5/168)
	:	:	:
GSELxN0[6:0] GSELxN1[6:0] GSELxN2[6:0] GSELxN3[6:0] GSELxN4[6:0] GSELxN5[6:0]	:	:	:
	7'h7A	#40	ΔV× (1-122/168)
	7'h7B	#39	ΔV× (1-123/168)
	7'h7C	#38	ΔV× (1-124/168)
	7'h7D	#37	ΔV× (1-125/168)
	7'h7E	#36	ΔV× (1-126/168)
	7'h7F	#35	ΔV× (1-127/168)

Note: "ΔV" in the list above indicates "VPLVL-VGS (positive)" or VGS-VNLVL (negative).

Table 61

Register	Register setting value	Grayscale reference level to be selected	Select level
GSELxP6[6:0] GSELxP7[6:0] GSELxP8[6:0] GSELxP9[6:0] GSELxP10[6:0] GSELxP11[6:0]	7'h00	#0	ΔV× (0+6) /168
	7'h01	#1	ΔV× (1+6) /168
	7'h02	#2	ΔV× (2+6) /168
	7'h03	#3	ΔV× (3+6) /168
	7'h04	#4	ΔV× (4+6) /168
	7'h05	#5	ΔV× (5+6) /168
	:	:	:
GSELxN6[6:0] GSELxN7[6:0] GSELxN8[6:0] GSELxN9[6:0] GSELxN10[6:0] GSELxN11[6:0]	:	:	:
	7'h7A	#122	ΔV× (122+6) /168
	7'h7B	#123	ΔV× (123+6) /168
	7'h7C	#124	ΔV× (124+6) /168
	7'h7D	#125	ΔV× (125+6) /168
	7'h7E	#126	ΔV× (126+6) /168
	7'h7F	#127	ΔV× (127+6) /168

Note: "ΔV" in the list above indicates "VPLVL-VGS (positive)" or VGS-VNLVL (negative).

Grayscale Voltage Calculation Formula

Table 62

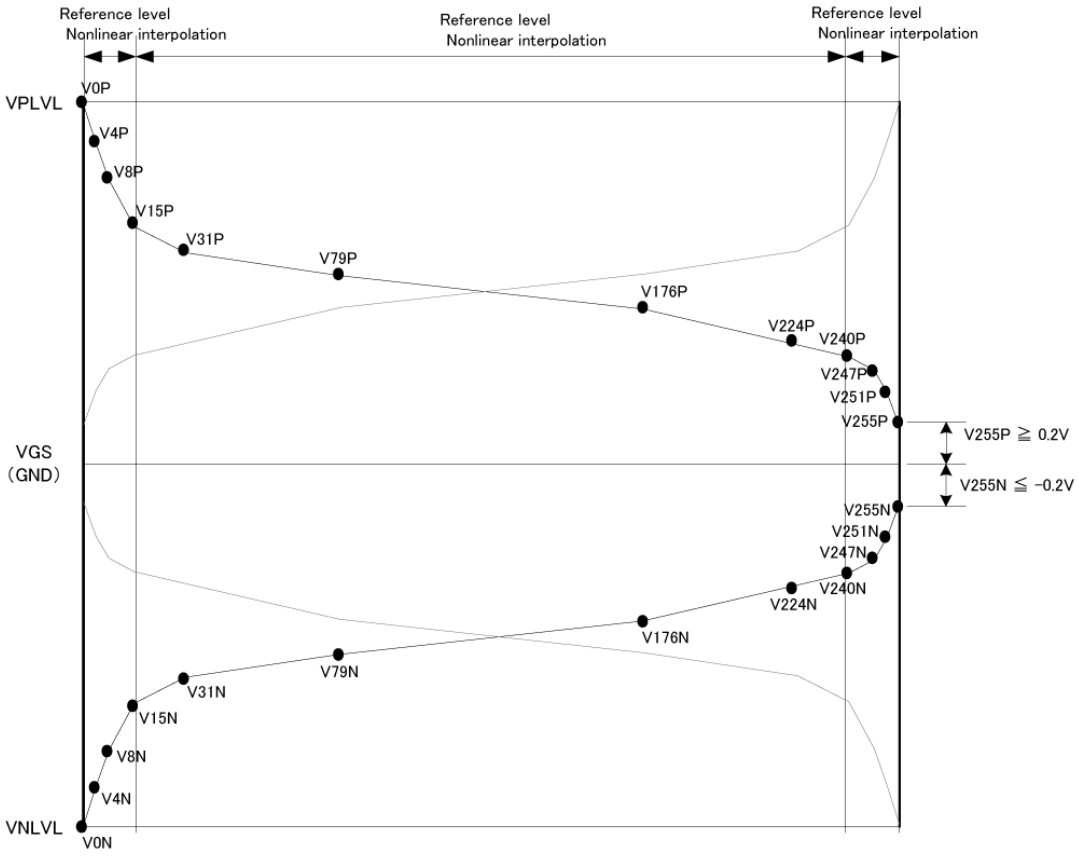
Grayscale voltage	Formula	Grayscale voltage	Formula
V0	See "Reference level select table"	V33	(V31*2+V35*2)/4
V1	(V0-V4)*18/26+V4	V34	(V31+V35*3)/4
V2	(V0-V4)*11/26+V4	V35	(V31-V79)*24/27+V79
V3	(V0-V4)*5/26+V4	V36	(V35*3+V39)/4
V4	See "Reference level select table"	V37	(V35*2+V39*2)/4
V5	(V4-V8)*10/14+V8	V38	(V35+V39*3)/4
V6	(V4-V8)*6/14+V8	V39	(V31-V79)*21/27+V79
V7	(V4-V8)*3/14+V8	V40	(V39*3+V43)/4
V8	See "Reference level select table"	V41	(V39*2+V43*2)/4
V9	(V8-V15)*13/16+V15	V42	(V39+V43*3)/4
V10	(V8-V15)*10/16+V15	V43	(V31-V79)*18/27+V79
V11	(V8-V15)*8/16+V15	V44	(V43*3+V47)/4
V12	(V8-V15)*6/16+V15	V45	(V43*2+V47*2)/4
V13	(V8-V15)*4/16+V15	V46	(V43+V47*3)/4
V14	(V8-V15)*2/16+V15	V47	(V31-V79)*15.5/27+V79
V15	See "Reference level select table"	V48	(V47*3+V51)/4
V16	(V15*3+V19)/4	V49	(V47*2+V51*2)/4
V17	(V15*2+V19*2)/4	V50	(V47+V51*3)/4
V18	(V15+V19*3)/4	V51	(V31-V79)*13/27+V79
V19	(V15-V31)*12/17+V31	V52	(V51*3+V55)/4
V20	(V19*3+V23)/4	V53	(V51*2+V55*2)/4
V21	(V19*2+V23*2)/4	V54	(V51+V55*3)/4
V22	(V19+V23*3)/4	V55	(V31-V79)*10.5/27+V79
V23	(V15-V31)*7/17+V31	V56	(V55*3+V59)/4
V24	(V23*3+V27)/4	V57	(V55*2+V59*2)/4
V25	(V23*2+V27*2)/4	V58	(V55+V59*3)/4
V26	(V23+V27*3)/4	V59	(V31-V79)*8.5/27+V79
V27	(V15-V31)*3/17+V31	V60	(V59*3+V63)/4
V28	(V27*3+V31)/4	V61	(V59*2+V63*2)/4
V29	(V27*2+V31*2)/4	V62	(V59+V63*3)/4
V30	(V27+V31*3)/4	V63	(V31-V79)*6.5/27+V79
V31	See "Reference level select table"	V64	(V63*3+V67)/4
V32	(V31*3+V35)/4	V65	(V63*2+V67*2)/4

Grayscale voltage	Formula	Grayscale voltage	Formula
V66	(V63+V67*3)/4	V99	(V79-V176)*19.25/24.25+V176
V67	(V31-V79)*4.5/27+V79	V100	(V99*3+V103)/4
V68	(V67*3+V71)/4	V101	(V99*2+V103*2)/4
V69	(V67*2+V71*2)/4	V102	(V99+V103*3)/4
V70	(V67+V71*3)/4	V103	(V79-V176)*18.25/24.25+V176
V71	(V31-V79)*3/27+V79	V104	(V103*3+V107)/4
V72	(V71*3+V75)/4	V105	(V103*2+V107*2)/4
V73	(V71*2+V75*2)/4	V106	(V103+V107*3)/4
V74	(V71+V75*3)/4	V107	(V79-V176)*17.25/24.25+V176
V75	(V31-V79)*1.5/27+V79	V108	(V107*3+V111)/4
V76	(V75*3+V79)/4	V109	(V107*2+V111*2)/4
V77	(V75*2+V79*2)/4	V110	(V107+V111*3)/4
V78	(V75+V79*3)/4	V111	(V79-V176)*16.25/24.25+V176
V79	**See "Reference level select table"**	V112	(V111*3+V115)/4
V80	(V79*3+V83)/4	V113	(V111*2+V115*2)/4
V81	(V79*2+V83*2)/4	V114	(V111+V115*3)/4
V82	(V79+V83*3)/4	V115	(V79-V176)*15.25/24.25+V176
V83	(V79-V176)*23.25/24.25+V176	V116	(V115*3+V119)/4
V84	(V83*3+V87)/4	V117	(V115*2+V119*2)/4
V85	(V83*2+V87*2)/4	V118	(V115+V119*3)/4
V86	(V83+V87*3)/4	V119	(V79-V176)*14.25/24.25+V176
V87	(V79-V176)*22.25/24.25+V176	V120	(V119*3+V123)/4
V88	(V87*3+V91)/4	V121	(V119*2+V123*2)/4
V89	(V87*2+V91*2)/4	V122	(V119+V123*3)/4
V90	(V87+V91*3)/4	V123	(V79-V176)*13.25/24.25+V176
V91	(V79-V176)*21.25/24.25+V176	V124	(V123*3+V127)/4
V92	(V91*3+V95)/4	V125	(V123*2+V127*2)/4
V93	(V91*2+V95*2)/4	V126	(V123+V127*3)/4
V94	(V91+V95*3)/4	V127	(V79-V176)*12.25/24.25+V176
V95	(V79-V176)*20.25/24.25+V176	V128	(V79-176)*12/24.25+V176
V96	(V95*3+V99)/4	V129	(V128*3+V132)/4
V97	(V95*2+V99*2)/4	V130	(V128*2+V132*2)/4
V98	(V95+V99*3)/4	V131	(V128+V132*3)/4

Grayscale voltage	Formula	Grayscale voltage	Formula
V132	(V79-176)*11/24.25+V176	V165	(V164*3+V168)/4
V133	(V132*3+V136)/4	V166	(V164*2+V168*2)/4
V134	(V132*2+V136*2)/4	V167	(V164+V168*3)/4
V135	(V132+V136*3)/4	V168	(V79-176)*2/24.25+V176
V136	(V79-176)*10/24.25+V176	V169	(V168*3+V172)/4
V137	(V136*3+V140)/4	V170	(V168*2+V172*2)/4
V138	(V136*2+V140*2)/4	V171	(V168+V172*3)/4
V139	(V136+V140*3)/4	V172	(V79-176)*1/24.25+V176
V140	(V79-176)*9/24.25+V176	V173	(V172*3+V176)/4
V141	(V140*3+V144)/4	V174	(V172*2+V176*2)/4
V142	(V140*2+V144*2)/4	V175	(V172+V176*3)/4
V143	(V140+V144*3)/4	**V176**	**See "Reference level select table"**
V144	(V79-176)*8/24.25+V176	V177	(V176*3+V180)/4
V145	(V144*3+V148)/4	V178	(V176*2+V180*2)/4
V146	(V144*2+V148*2)/4	V179	(V176+V180*3)/4
V147	(V144+V148*3)/4	V180	(V176-V224)*25.5/27+V224
V148	(V79-176)*7/24.25+V176	V181	(V180*3+V184)/4
V149	(V148*3+V152)/4	V182	(V180*2+V184*2)/4
V150	(V148*2+V152*2)/4	V183	(V180+V184*3)/4
V151	(V148+V152*3)/4	V184	(V176-V224)*24/27+V224
V152	(V79-176)*6/24.25+V176	V185	(V184*3+V188)/4
V153	(V152*3+V156)/4	V186	(V184*2+V188*2)/4
V154	(V152*2+V156*2)/4	V187	(V184+V188*3)/4
V155	(V152+V156*3)/4	V188	(V176-V224)*22.5/27+V224
V156	(V79-176)*5/24.25+V176	V189	(V188*3+V192)/4
V157	(V156*3+V160)/4	V190	(V188*2+V192*2)/4
V158	(V156*2+V160*2)/4	V191	(V188+V192*3)/4
V159	(V156+V160*3)/4	V192	(V176-V224)*20.5/27+V224
V160	(V79-176)*4/24.25+V176	V193	(V192*3+V196)/4
V161	(V160*3+V164)/4	V194	(V192*2+V196*2)/4
V162	(V160*2+V164*2)/4	V195	(V192+V196*3)/4
V163	(V160+V164*3)/4	V196	(V176-V224)*18.5/27+V224
V164	(V79-176)*3/24.25+V176	V197	(V197*3+V200)/4

Grayscale voltage	Formula	Grayscale voltage	Formula
V198	(V197*2+V200*2)/4	V231	(V228+V232*3)/4
V199	(V197+V200*3)/4	V232	(V224-V240)*10/17+V240
V200	(V176-V224)*16.5/27+V224	V233	(V232*3+V236)/4
V201	(V200*3+V204)/4	V234	(V232*2+V236*2)/4
V202	(V200*2+V204*2)/4	V235	(V232+V236*3)/4
V203	(V200+V204*3)/4	V236	(V224-V240)*5/17+V240
V204	(V176-V224)*14/27+V224	V237	(V236*3+V240)/4
V205	(V204*3+V208)/4	V238	(V236*2+V240*2)/4
V206	(V204*2+V208*2)/4	V239	(V236+V240*3)/4
V207	(V204+V208*3)/4	**V240**	**See "Reference level select table"**
V208	(V176-V224)*11.5/27+V224	V241	(V240-V247)*14/16+V247
V209	(V208*3+V212)/4	V242	(V240-V247)*12/16+V247
V210	(V208*2+V212*2)/4	V243	(V240-V247)*10/16+V247
V211	(V208+V212*3)/4	V244	(V240-V247)*8/16+V247
V212	(V176-V224)*9/27+V224	V245	(V240-V247)*6/16+V247
V213	(V212*3+V216)/4	V246	(V240-V247)*3/16+V247
V214	(V212*2+V216*2)/4	**V247**	**See "Reference level select table"**
V215	(V212+V216*3)/4	V248	(V247-V251)*11/14+V251
V216	(V176-V224)*6/27+V224	V249	(V247-V251)*8/14+V251
V217	(V216*3+V220)/4	V250	(V247-V251)*4/14+V251
V218	(V216*2+V220*2)/4	**V251**	**See "Reference level select table"**
V219	(V216+V220*3)/4	V252	(V251-V255)*21/26+V255
V220	(V176-V224)*3/27+V224	V253	(V251-V255)*15/26+V255
V221	(V220*3+V224)/4	V254	(V251-V255)*8/26+V255
V222	(V220*2+V224*2)/4	**V255**	**See "Reference level select table"**
V223	(V220+V224*3)/4		
V224	**See "Reference level select table"**		
V225	(V224*3+V228)/4		
V226	(V224*2+V228*2)/4		
V227	(V224+V228*3)/4		
V228	(V224-V240)*14/17+V240		
V229	(V228*3+V232)/4		
V230	(V228*2+V232*2)/4		

Example of γ setting



Note: 1. V0, V4, V8, V15, V31, V79, V176, V224, V240, V247, V251 and V255 are "Reference level" which is set by correction resistors.
2. Make sure that |V0| > |V4| > |V8| > |V15| > |V31| > |V79| > |V176| > |V224| > |V240| > |V247| > |V251| > |V255| when setting γ correction resistors.
3. Make sure that V255P ≧ 0.2V, V255N ≦ −0.2V when setting γ correction resistors.

Figure 142

The relationship between data and grayscale voltage (REV, VCMREV=0)

Table 63

Frame memory data	REV = 1		REV = 0	
	Positive polarity (PRxPxx)	Negative Polarity (PRxNxx)	Positive Polarity (PRxPxx)	Negative Polarity (PRxNxx)
8'h00	V0	V0	V255	V255
8'h01	V1	V1	V254	V254
8'h02	V2	V2	V253	V253
8'h03	V3	V3	V252	V252
8'h04	V4	V4	V251	V251
8'h05	V5	V5	V250	V250
8'h06	V6	V6	V249	V249
8'h07	V7	V7	V248	V248
8'h08	V8	V8	V247	V247
8'h09	V9	V9	V246	V246
8'h0A	V10	V10	V245	V245
8'h0B	V11	V11	V244	V244
8'h0C	V12	V12	V243	V243
8'h0D	V13	V13	V242	V242
8'h0E	V14	V14	V241	V241
8'h0F	V15	V15	V240	V240
:	:	:	:	:
8'hF0	V240	V240	V15	V15
8'hF1	V241	V241	V14	V14
8'hF2	V242	V242	V13	V13
8'hF3	V243	V243	V12	V12
8'hF4	V244	V244	V11	V11
8'hF5	V245	V245	V10	V10
8'hF6	V246	V246	V9	V9
8'hF7	V247	V247	V8	V8
8'hF8	V248	V248	V7	V7
8'hF9	V249	V249	V6	V6
8'hFA	V250	V250	V5	V5
8'hFB	V251	V251	V4	V4
8'hFC	V252	V252	V3	V3
8'hFD	V253	V253	V2	V2
8'hFE	V254	V254	V1	V1
8'hFF	V255	V255	V0	V0

Power Supply Generating Circuit

The following figure shows the configurations of LCD drive voltage generating circuit of the R61529.

Power Supply Circuit Connection Example

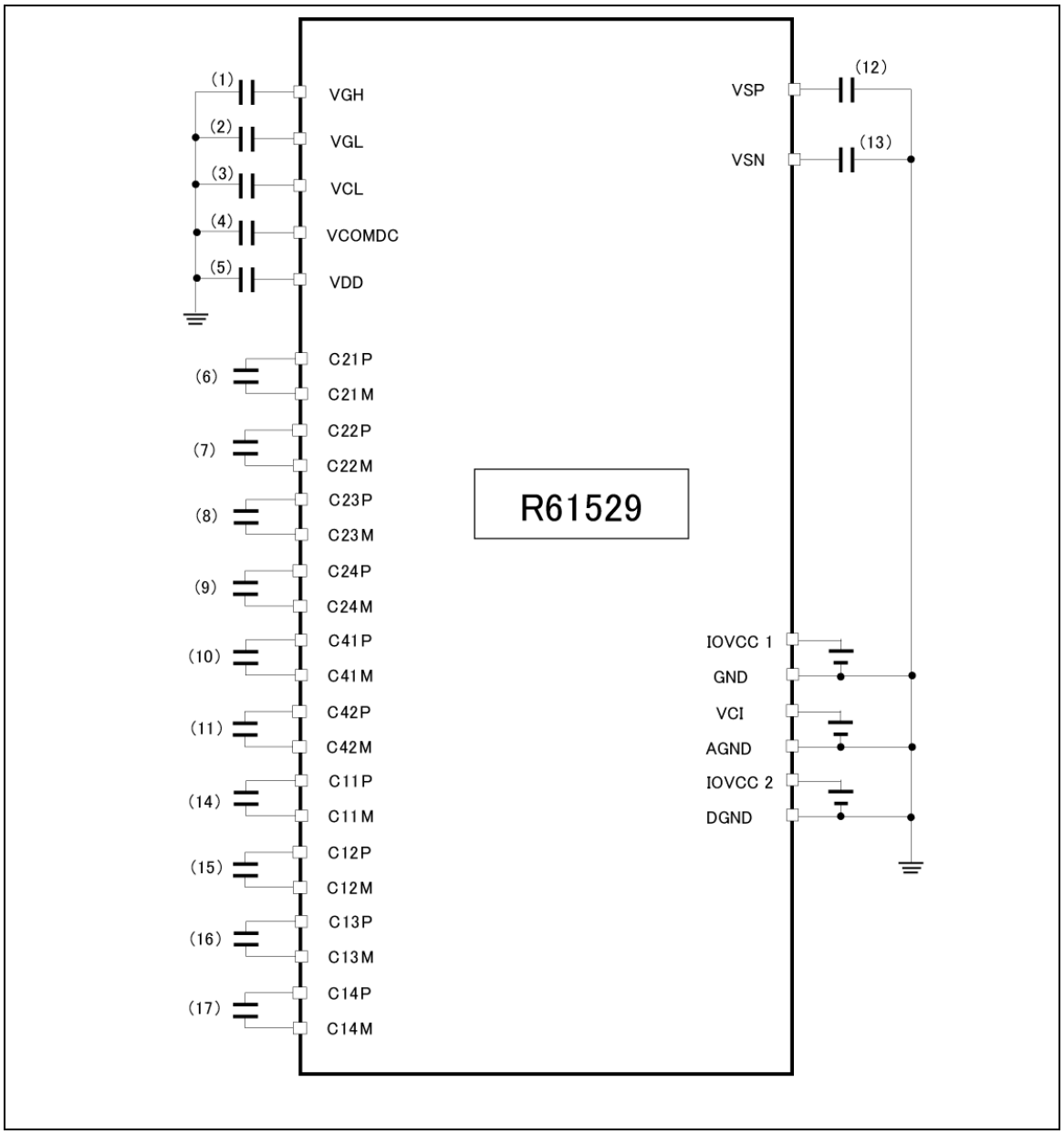


Figure 143

Specifications of External Elements Connected to the Power Supply Circuit

The specifications of external elements connected to the power-supply circuit of the R61529 are as follows. The numbers in the parentheses refer to the numbers in figure “Power Supply Circuit Connection Example”.

Table 64

Capacitor	Recommended tolerance of capacitor	Connected to
1μF (B characteristics) (TBD.)	3V	(5)VDD
	6V	(3)VCL, (4)VCOMDC, (10)C41P/M, (11)C42P/M, (14)C11P/M, (15)C12P/M, (16)C13P/M, (17)C14P/M
	10V	(12)VSP, (13)VSN
	16V	(6)C21P/M, (7)C22P/M, (8)C23P/M, (9)C24P/M
	25V	(1)VGH, (2)VGL

Note: To place bypass capacitor at spots between each power supply (VCI, IOVCC1, IOVCC2) and GND is recommended.

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61529 and the relationship between TFT display application voltage waveforms and electrical potential.

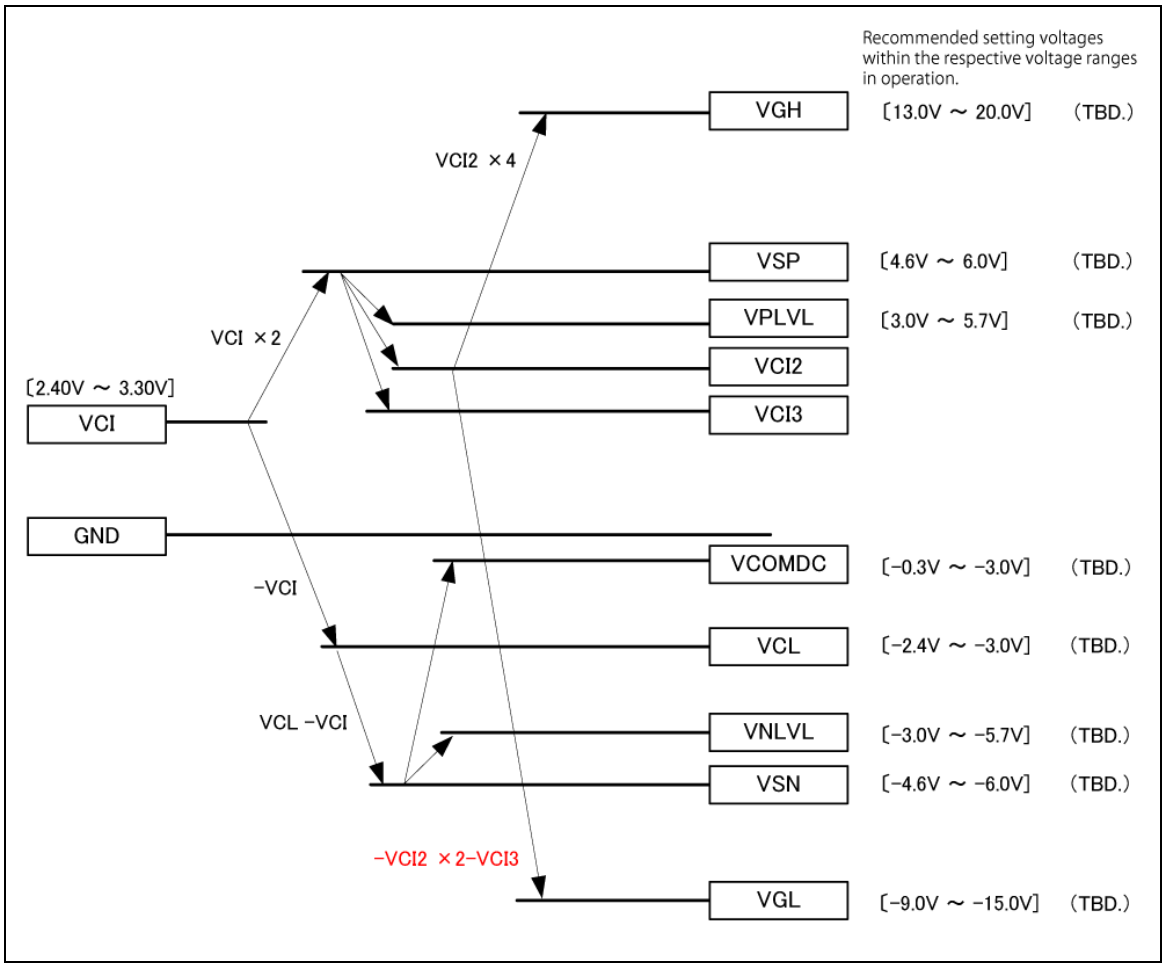


Figure 144

Note: 1. Make sure that (VSP-VPLVL) ≥ 0.3V, (VSN-VNLVL) ≤ -0.3V. Please be careful that the VSP, VSN output voltages will become lower due to current consumption in display operation. Also, this VSP and VSN output voltage depression contributes to VGH and VGL voltages depression. It may lead amplitude reduction of the voltage from IC to the panel, and the gate line drive.

2. In operation, setting voltages within the respective voltage ranges written above is recommended.
3. Make sure that VCI-VCL ≤ 6V.

Deep Standby Mode/Shut down Mode(MDDI) On/Off Sequence

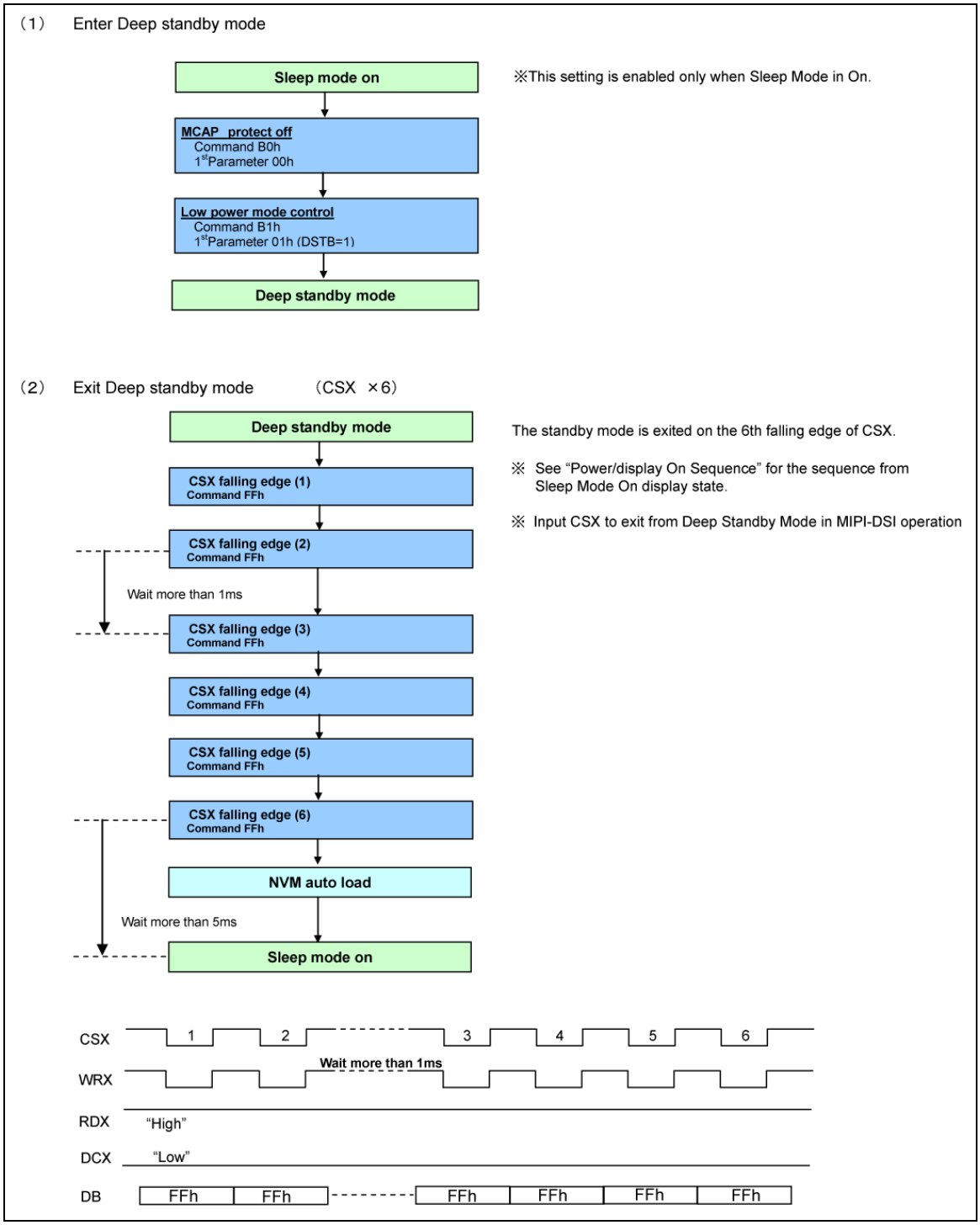


Figure 145

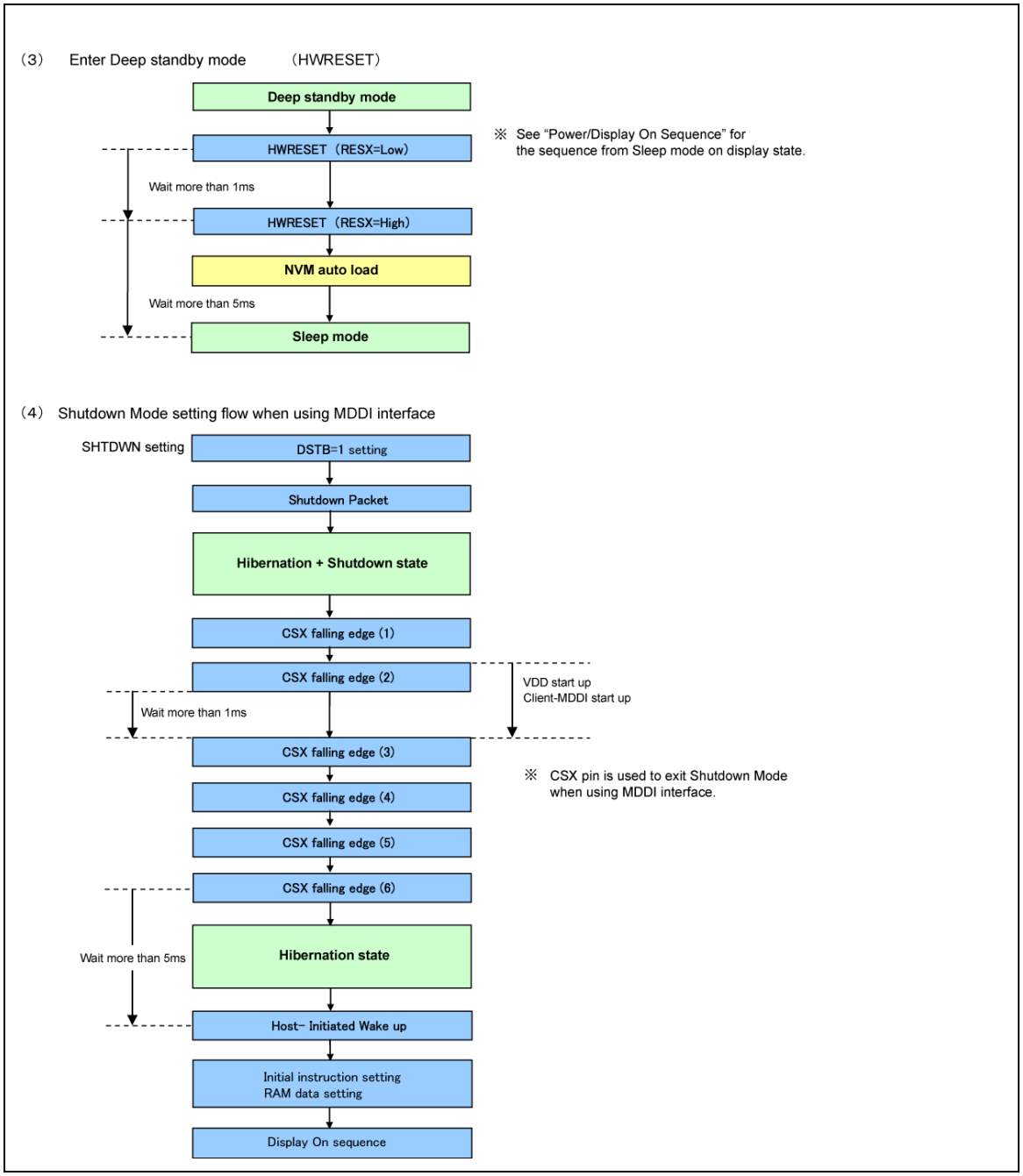


Figure 146

NVM Control (T.B.D.)

R61529 supports xxxk bit NVM.

Read data by read_DDB_start command: Supplier ID (16 bits), Supplier Elective Data (16 bits)
For storing Manufacturer Commands

To write data to the NVM, follow the sequences below.

Written data are loaded to registers when

- Power On sequence
- HW RESET sequence
- exit_sleep_mode sequence

are executed.

Data written to the NVM are hold permanently even if power supply is shut down.

Table 65 NVM operating conditions

Operation	Power supply voltage (T.B.D.)		Time	Temperature
Write/Erase	VCI	2.40～3.30V	900ms or more, after E0h: FTT=1settimg	+20℃～+30℃
	IOVCC1	1.65～3.30V		

Note: NVM data can be erased and rewritten up to 5 times per an address.

Below commands are stored in the NVM.

(T.B.D.)

NVM Write Sequence

The register values of User/Manufacturer Commands supposed to be stored in NVM are written to NVM. When “1” is written to an address, the bit of the address is set to “1”. The default status is “0”.

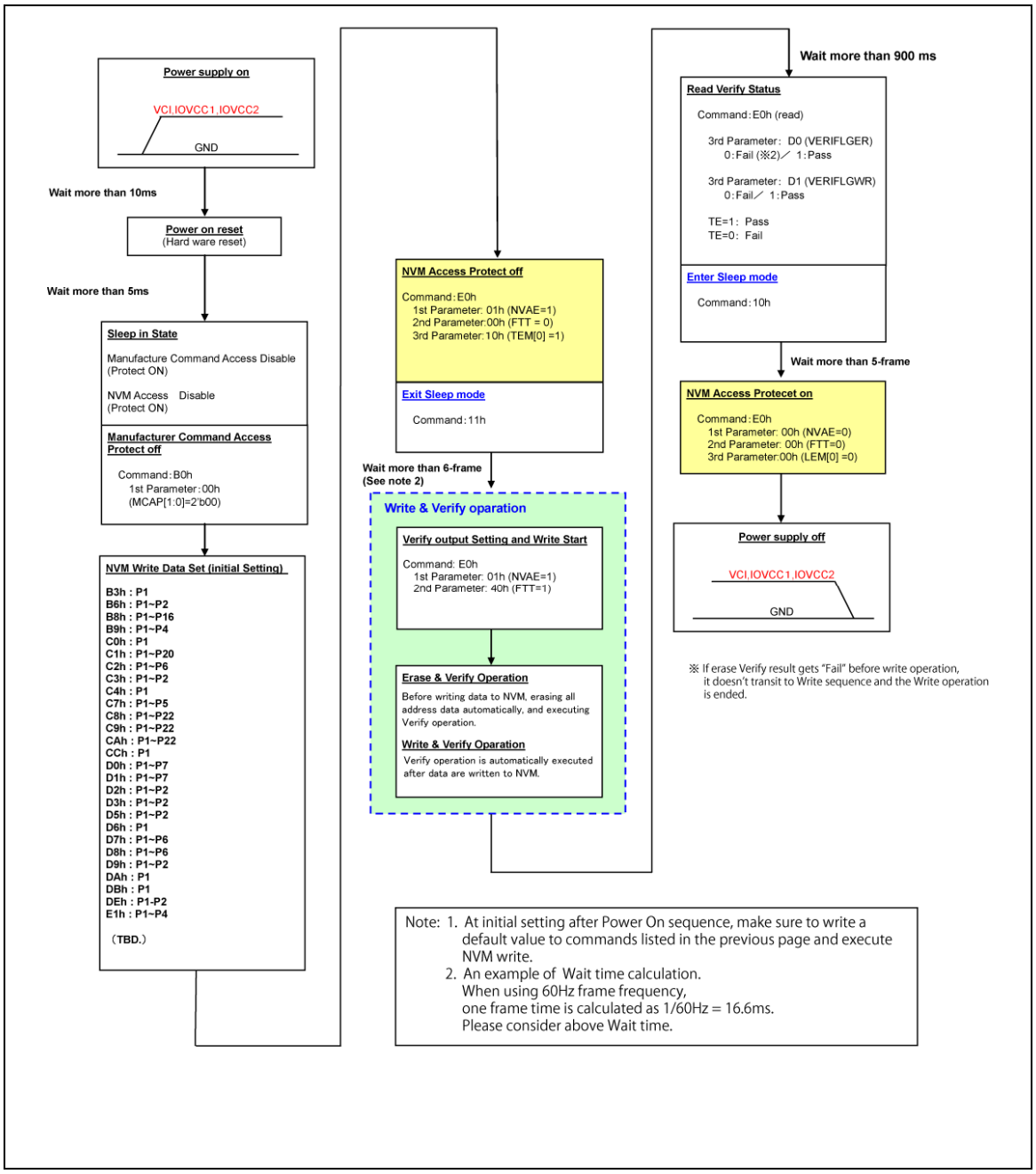


Figure 147

Absolute Maximum Rating

Table 66

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	IOVCC1, IOVCC2	V	-0.3 ~ +4.6	1, 2
Power supply voltage (2)	VCI – AGND	V	-0.3 ~ +4.6	1, 3
Power supply voltage (3)	VCI – VCL	V	-0.3 ~ +6.5	1, 4
Power supply voltage (4)	VSP – AGND	V	-0.3 ~ +6.5	1, 4
Power supply voltage (5)	AGND – VSN	V	-0.3 ~ +6.5	1, 4
Power supply voltage (6)	AGND– VGL	V	-0.3 ~ +20.0	1, 5
Power supply voltage (7)	VGH– AGND	V	-0.3 ~ +22.0	1
Power supply voltage (8)	VGH – VGL	V	-0.3 ~ +30.0	1
Input voltage	Vt	V	-0.3 ~ IOVCC1,2 + 0.3	1
Operating temperature	Topr	°C	-40 ~ +85	1, 6
Storage temperature	Tstg	°C	-55 ~ +110	1

Notes:
1. If used beyond the absolute maximum ratings, the LSI may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of LSI is not guaranteed if used in the conditions beyond the limits and it may lead to malfunction.
2. Make sure (High) IOVCC1 ≥ GND (Low), (High) IOVCC2 ≥ GND (Low).
3. Make sure (High) VCI ≥ AGND (Low).
4. Make sure (High) VSP ≥ AGND (Low), (High) VSN ≤ AGND (Low).
5. Make sure (High) AGND ≥ VGL (Low).
6. The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Electrical Characteristics (TBD.)

DC Characteristics

Table 67 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1 **(TBD.)**

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Input "High" level voltage 1 (Except RESX)		V_{IH1}	V	IOVCC=1.650V~3.300V	0.80 x IOVCC1	–	IOVCC1	1, 2
Input "Low" level voltage 1 (RESX)		V_{IL1}	V	IOVCC=1.650V~3.300V	0	–	0.20 x IOVCC1	1, 2
Input "High" level voltage 2 (RESX)		V_{IH2}	V	IOVCC=1.650V~3.300V	0.90 x IOVCC1	–	IOVCC1	1, 2
Input "Low" level voltage 2 (RESX)		V_{IL2}	V	IOVCC=1.650V~3.300V	0	–	0.10 x IOVCC1	1, 2
Output "High" level voltage 1 (DB[15:0],TE,LEDPWM)		V_{OH1}	V	IOVCC=1.650V~3.300V, IOUT=-0.1mA	0.80 x IOVCC1	–	–	1
Output "Low" level voltage 1 (DB[15:0],TE,LEDPWM)		V_{OL1}	V	IOVCC=1.650V~3.300Vm, IOUT=0.1mA	–	–	0.20 x IOVCC1	1
Input "High" level current		I_{IH}	µA	Vin=IOVCC1	–	–	10	4
Input "Low" level current		I_{IL}	µA	Vin=0V	-10	–	–	4
Current consumption (IOVCC1-GND)	Normal Mode +Sleep out			864 line drive IOVCC1=1.80V IOVCC2=VCI=2.80V fFLM=60Hz, Ta=25°C BLCON=0 when DPI is selected				
	Deep Standby mode	I_{DST1}	µA	IOVCC1=1.80V IOVCC2=VCI=2.80V Ta=25°C	-	0.1	1.0	5
LCD power supply current (VCI-GND)	Normal Mode +Sleep out	I_{CIN}	mA	TBD.	-	-	TBD.	5
	Deep Standby mode	I_{DST3}	µA	IOVCC1=1.80V IOVCC2=VCI=2.80V	-	0.1	1.0	5
Output voltage dispersion	Δ(Vn – Vn+1) ≤ 10mV	⊿Vo1	mV	-	-	-	TBD.	6
	Δ(Vn – Vn+1) ≤ 20mV	⊿Vo2	mV	-	-	-	TBD.	6
	Δ(Vn – Vn+1) ≤ 30mV	⊿Vo3	mV	-	-	-	TBD.	6
	Δ(Vn – Vn+1) ≤ 50mV	⊿Vo4	mV	-	-	-	TBD.	6
	Δ(Vn – Vn+1) ≤ 100mV	⊿Vo5	mV	-	-	-	TBD.	6
Average output variance		⊿V⊿	mV	-	-35	–	+35	7

DC Characteristics (MIPI DSI)

Table 68 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1 **(TBD.)**

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSI current consumption (IOVCC2-DGND):	HS mode	I_{HS}	mA	IOVCC1=1.800V IOVCC2=VCI=2.800V DSI 1 lane, DSICLK=120MHz DSI Data:24'h000	-	-	TBD.	5
	LP mode	I_{LP}	μA	IOVCC1=1.800V IOVCC2=VCI=2.800V Clock lane=LP11 Data lane=LP11	-	-	TBD.	5
	Deep Standby mode	I_{DST2}	μA	IOVCC1=1.800V IOVCC2=VCI=2.800V Ta=25°C	-	0.1	1.0	5

DC Characteristics (MIPI DSI DC Specifications)

Table 69 (IOVCC2= 2.40V~3.30V, Ta = -40°C ~ +85°C) (TBD.)

Item		Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
HS-RX	Differential input high threshold	VIDTH	mV		-	-	70	3
	Differential input low threshold	VIDTL	mV		-70	-	-	3
	Single-ended input low voltage	VILHS	mV		-40	-	-	
	Single-ended input high voltage	VIHHS	mV		-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV		70	-	330	1
	Differential input impedance	ZID	Ω		-	(90)	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV		-50	-	550	
	Logic 1 input voltage	VIH	mV		880	-	1350	
	I/O leakage current	ILEAK	μA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV		-50	-	50	
	Thevenin output high level	VOH	V		1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω		(110)	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV		-	-	200	
	Logic 1 contention threshold	VIHCD	mV		450	-	-	

Notes: 1. VCMRX(DC) = (VDP+VDN)/2

2. Excluding COG Resistance (Contact Resistance and ITO Wiring Resistance).
   The values are tentative.

3. Minimum110mV/-110mV HS differential swing is required for display data transfer.

DC Characteristics (MDDI)

Table 70 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1 **(TBD.)**

Item		Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
Standard receiver differential input "High" threshold voltage (DATA0P/M, STB_CLK_P/M)		V_{IT+}	mV	(DATA0_P)−(DATA0_M) (STB_CLK_P) – (STB_CLK _M)	–	0	50	–
Standard receiver differential input "Low" threshold voltage (DATA0P/M, STB_CLK_P/M)		V_{IT-}	mV	(DATA0_P)−(DATA0_M) (STB_CLK_P) – (STB_CLK _M)	-50	0	–	–
Offset receiver differential input "High" threshold voltage (DATA0P/M)		V_{IT+off}	mV		–	85	110	–
Offset receiver differential input "Low" threshold voltage (DATA0P/M)		V_{IT-off}	mV		60	85	–	–
Receiver differential input "High" Current (DATA0P/M, STB_CLK_P/M)		I_{ID+}	mA		1.5	–	2.5	1
Receiver differential input "Low" Current (DATA0P/M, STB_CLK_P/M)		I_{ID-}	mA		-2.5	–	-1.5	1
Input voltage range		V_{IRNG}	V		0.6	–	1.1	–
Driver differential output "High" Current (DATA0P/M)		I_{OD+}	mA		2.5	–	4.5	2
Driver differential output "Low" Current (DATA0P/M)		I_{OD-}	mA		-4.5	–	-2.5	2
Output voltage range		V_{ORNG}	V		0.11	–	1.60	2
Differential input impedance		ZID	Ω		80	100	125	–
Current consumption (IOVCC2-DGND)	Hibernation	I_{hib}	μA	IOVCC1=IOVCC2=VCI=2.85V, Ta=25℃	–	TBD.	TBD.	–
Current consumption (IOVCC2-DGND)	data transfer	I_{trans}	mA	IOVCC1=IOVCC2= VCI =2.85V, $1/t_{BIT}$=250Mbps, Ta=25℃	–	TBD.	TBD.	–

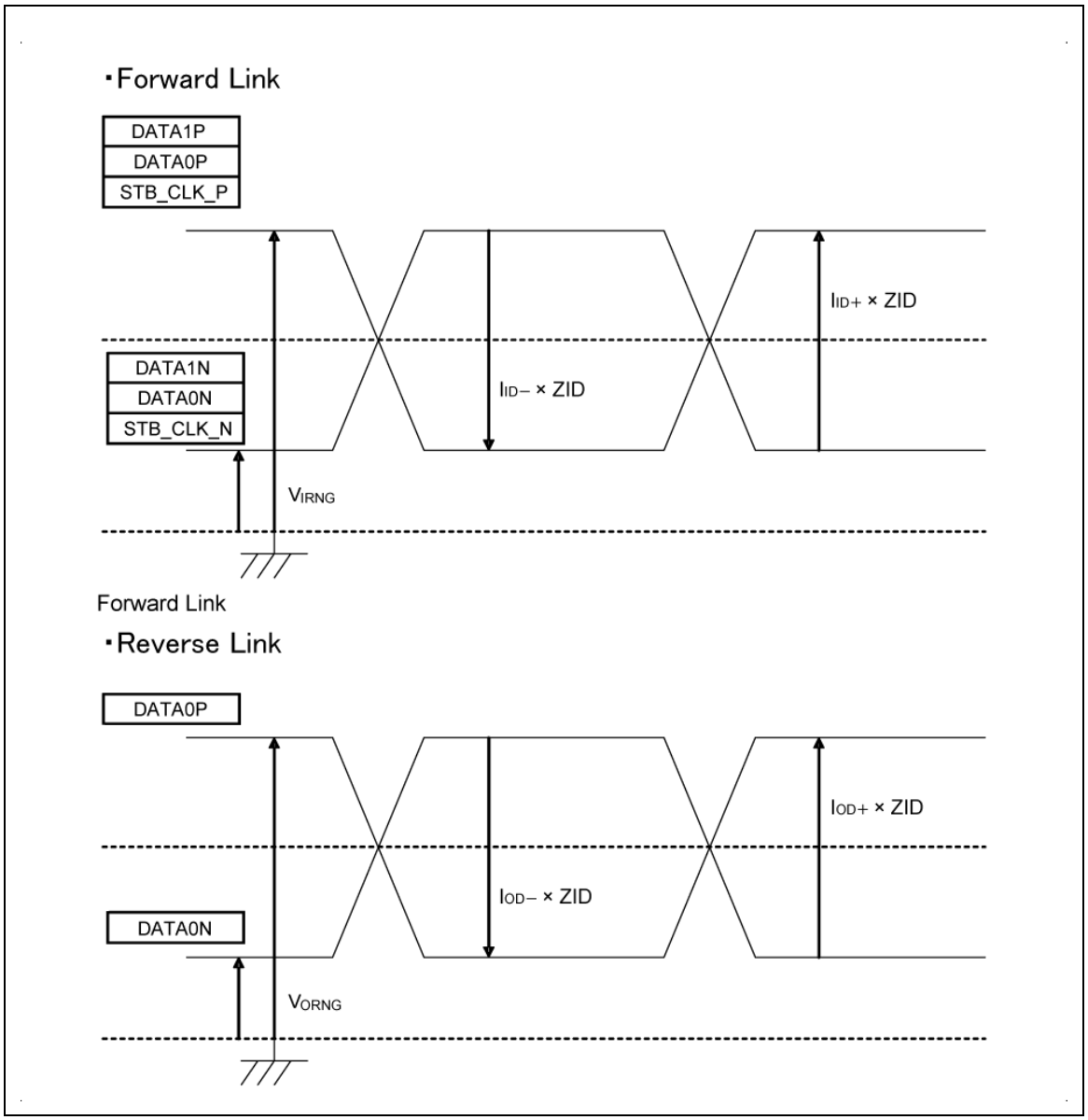


Figure 148 MDDI DC Characteristic Symbol

Step-up Circuit Characteristics

Table 71 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1 **(TBD.)**

Item		Unit	Test Condition	Min.	Typ.	Max.
Step-up output voltage	VSP	V	TBD.	TBD.	TBD.	TBD.
	VSN	V	TBD.	TBD.	TBD.	TBD.
	VCL	V	TBD.	TBD.	TBD.	TBD.
	VGH	V	TBD.	TBD.	TBD.	TBD.
	VGL	V	TBD.	TBD.	TBD.	TBD.

Power Supply Voltage Range

Table 72 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Power supply voltage	IOVCC1	V	1.65	1.80	3.30	-
	IOVCC2	V	2.40	2.80	3.30	-
	VCI	V	2.40	2.80	3.30	-

Output Voltage Range

Table 73 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Grayscale. VCOM reference voltage	VPLVL	V	VGS+0.2V	-	VSP-0.3	-
	VNLVL	V	VSN+0.3	-	VGS-0.2V	
Source driver	-	V	3.0V	-	VPLVL VNLVL	-
Step-up output voltage	VSP	V	4.6V	-	6.0V	-
Step-up output voltage	VSN	V	-4.6V	-	-6.0V	-
Step-up output voltage	VGH	V	13.0V	-	20.0V	-
Step-up output voltage	VGL	V	-9.0V	-	-15.0V	-
Voltage between VGH and VGL		V		-	30.0V	-

Clock Characteristics

Table 74 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

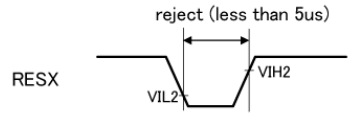
Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
RC oscillation clock	fosc	MHz	13.0	14.0	15.0	-

Reset Timing Characteristics

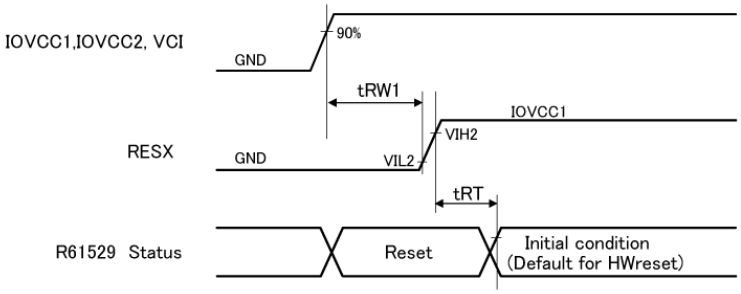
Table 75 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

Item	Symbol	Unit	Test Condition	Min.	Max.
Reset “Low” level width 1	tRW1	ms	Power On	1	–
Reset “Low” level width 2	tRW2	us	Operation	10	–
Reset time	tRT	ms		–	5

Reset reject



(1) Reset timing at Power supply ON



(2) Reset timing during operation

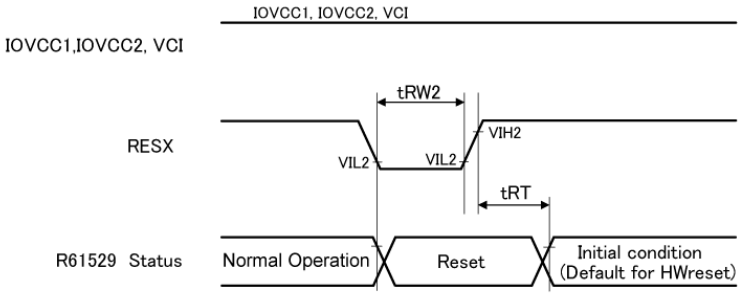


Figure 149 Reset Timing Characteristics

Liquid Crystal Driver Output Characteristics

Table 76 Source Driver (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Source driver output delay time	tdds	us	TBD.	–	–	TBD.	See note

Note: LCD driver output delay time depends on the liquid crystal panel load. Therefore, frame frequency and one line cycle needs to be specified checking image quality on the panel to be used.

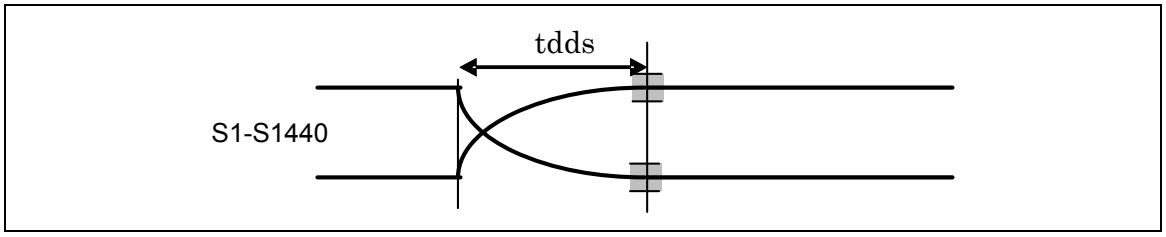


Figure 150 Liquid Crystal Driver Output Timing (TBD.)

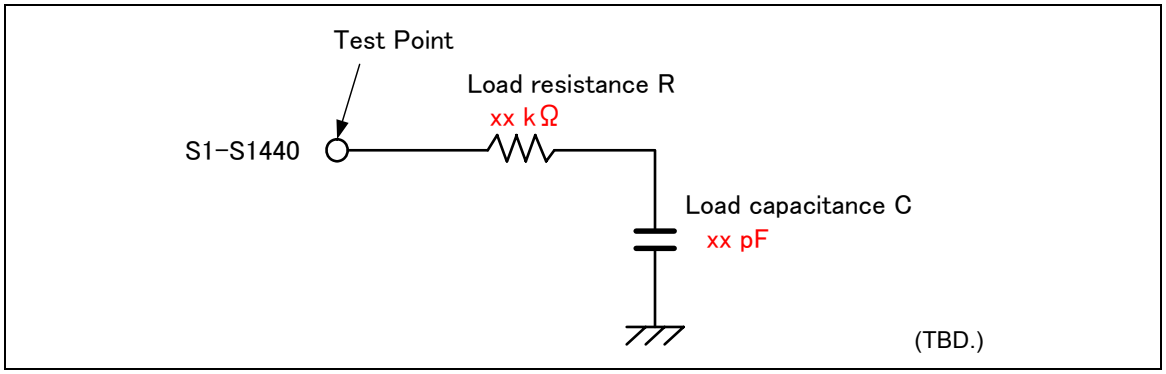


Figure 151 Load circuit for testing LCD driver output characteristics (TBD.)

MIPI DBI Type B Timing Characteristics

(VCI=IOVCC2=2.8V, IOVCC1=1.8V, Ta=-40°C ~ +85°C) see Note 1

Table 77 3/2-Transfer (IOVCC1=1.650V ~ 3.3V, Ta=-40°C ~ +85°C) (TBD.)

Item	Symbol		Unit	Test Condition	Min.	Max.
Address setup time	DCX	tast	ns		0	-
Address hold time (Write/Read)		taht	ns		10	-
Chip select setup time (Write)	CSX	tcs	ns		18	-
Chip select setup time (Read)		trcs	ns		170	-
Chip select wait time (Write/Read)		tcsf	ns		10	-
Write cycle time	WRX	twc	ns		68	-
Write control pulse ”High” period		twrh	ns		25	-
Write control pulse ”Low” period		twrl	ns		18	-
Read cycle time	RDX	trc	ns		450	-
Read control pulse ”High” period		trdh	ns		250	-
Read control pulse ”Low” period		trdl	ns		170	-
Write data setup time	DB[23:0]	twds	ns	CL Max.30pF Min.8pF	10	-
Write data hold time		twdh	ns		10	-
Read access time		tracc	ns		10	150
Output disable time		trod	ns		10	-
Rise / Fall time	-	tr/tf	ns		-	10

Table 78 1-Transfer (IOVCC1=1.650V ~ 3.3V, Ta=-40°C ~ +85°C) (TBD.)

Item	Symbol		Unit	Test Condition	Min.	Max.
Address setup time	DCX	tast	ns		0	-
Address hold time (Write/Read)		taht	ns		10	-
Chip select setup time (Write)	CSX	tcs	ns		30	-
Chip select setup time (Read)		trcs	ns		170	-
Chip select wait time (Write/Read)		tcsf	ns		20	-
Write cycle time	WRX	twc	ns		100	-
Write control pulse ”High” period		twrh	ns		30	-
Write control pulse ”Low” period		twrl	ns		30	-
Read cycle time	RDX	trc	ns		450	-
Read control pulse ”High” period		trdh	ns		250	-
Read control pulse ”Low” period		trdl	ns		170	-
Write data setup time	DB[23:0]	twds	ns	CL Max.30pF Min.8pF	15	-
Write data hold time		twdh	ns		25	-
Read access time		tracc	ns		10	150
Output disable time		trod	ns		10	-
Rise / Fall time	-	tr/tf	ns		-	15

Table 79 2-, 3- Transfer (IOVCC1=1.650V ~ 3.3V, Ta=-40°C ~ +85°C) (TBD.)

Item	Symbol		Unit	Test Condition	Min.	Max.
Address setup time	DCX	tast	ns		0	-
Address hold time (Write/Read)		taht	ns		10	-
Chip select setup time (Write)	CSX	tcs	ns		30	-
Chip select setup time (Read)		trcs	ns		170	-
Chip select wait time (Write/Read)		tcsf	ns		20	-
Write cycle time	WRX	twc	ns		60	-
Write control pulse ”High” period		twrh	ns		30	-
Write control pulse ”Low” period		twrl	ns		30	-
Read cycle time	RDX	trc	ns		450	-
Read control pulse ”High” period		trdh	ns		250	-
Read control pulse ”Low” period		trdl	ns		170	-
Write data setup time	DB[23:0]	twds	ns	CL Max.30pF Min.8pF	15	-
Write data hold time		twdh	ns		25	-
Read access time		tracc	ns		10	150
Output disable time		trod	ns		10	-
Rise / Fall time	-	tr/tf	ns		-	15

Note: 1 transfer: (1) 16-bit I/F 16bpp

3/2 transfers: (1) 16-bit I/F 18bpp, (2) 16-bit I/F 24 bpp Option 1

2 transfers: (1) 8-bit I/F 16bpp, (2) 16-bit I/F 18bpp Options 2, 3, (3) 16-bit I/F 24bpp Option 2

3 transfers: (1) 8-bit I/F 18bpp, (2) 8-bit I/F 24bpp

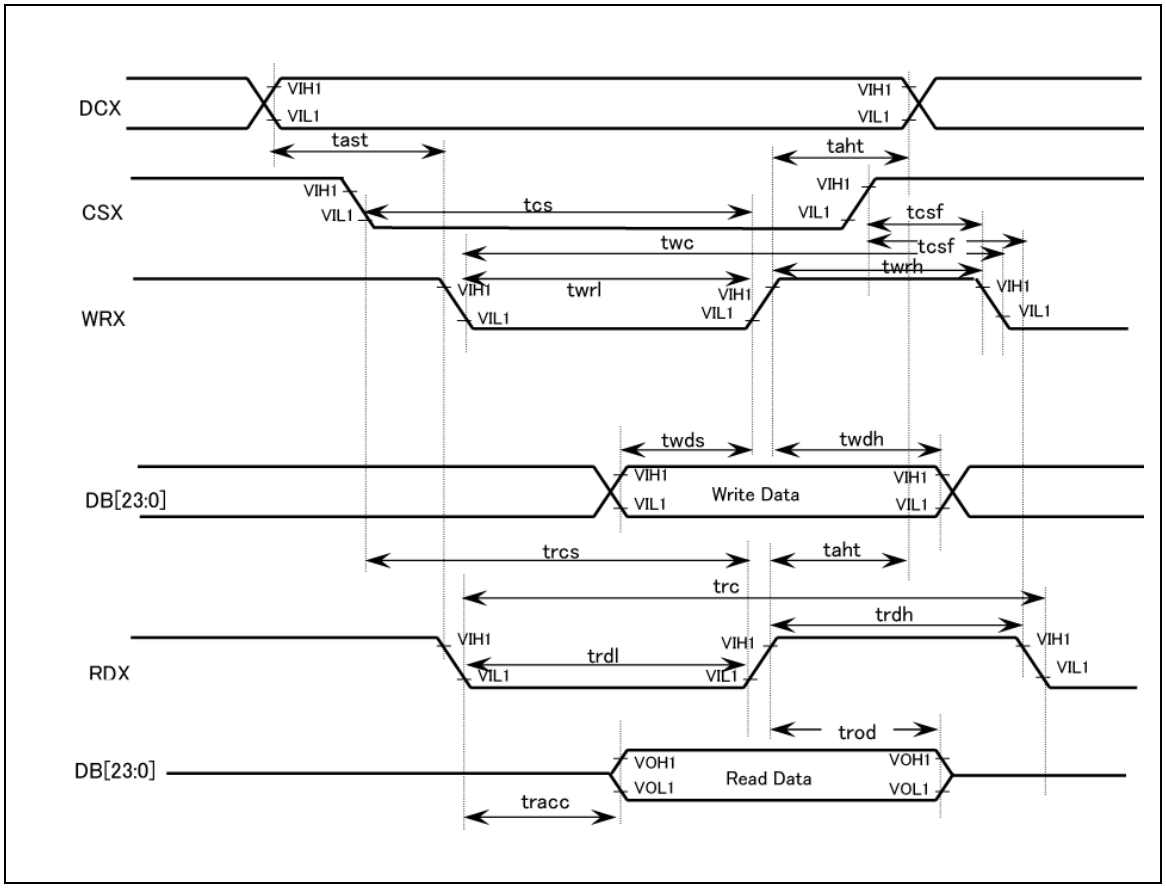


Figure 152 DBI TypeB (24/18/16/8bit) Timing

MIPI DBI Type C Timing Characteristics

Table 80 (IOVCC1=1.65V~3.30V, Ta=-40℃~+85℃) (TBD.)

Item	Symbol		Unit	Test Condition	Min.	Max.
Chip Select Set Up Time	CSX	tcss	ns		40	-
Chip Select Hold Time		tcsh	ns		40	-
Chip Select High Pulse Width		tchw	ns		100	
Address setup time	DCX	tas	ns		10	
Address hold time (Write/Read)		tah	ns		10	
Write Cycle Time	SCL (Write)	twc	ns		100	-
SCL"High"Width(Write)		twrh	ns		40	-
SCL"Low"Width(Write)		twrl	ns		40	-
Read Cycle Time	SCL (Read)	trc	ns		300	-
SCL"High"Width (Read)		trdh	ns		120	-
SCL"Low"Width(Read)		trdl	ns		120	-
Data Set Up Time	DIN	tds	ns		30	-
Data Hold Time		tdh	ns		30	-
Access Time	DOUT	tacc	ns	CL Max.30pF Min.8pF	-	110
Output Disable Time		tod	ns		10	-
Chip Select Set Up Time	-	tr/tf	ns		-	15

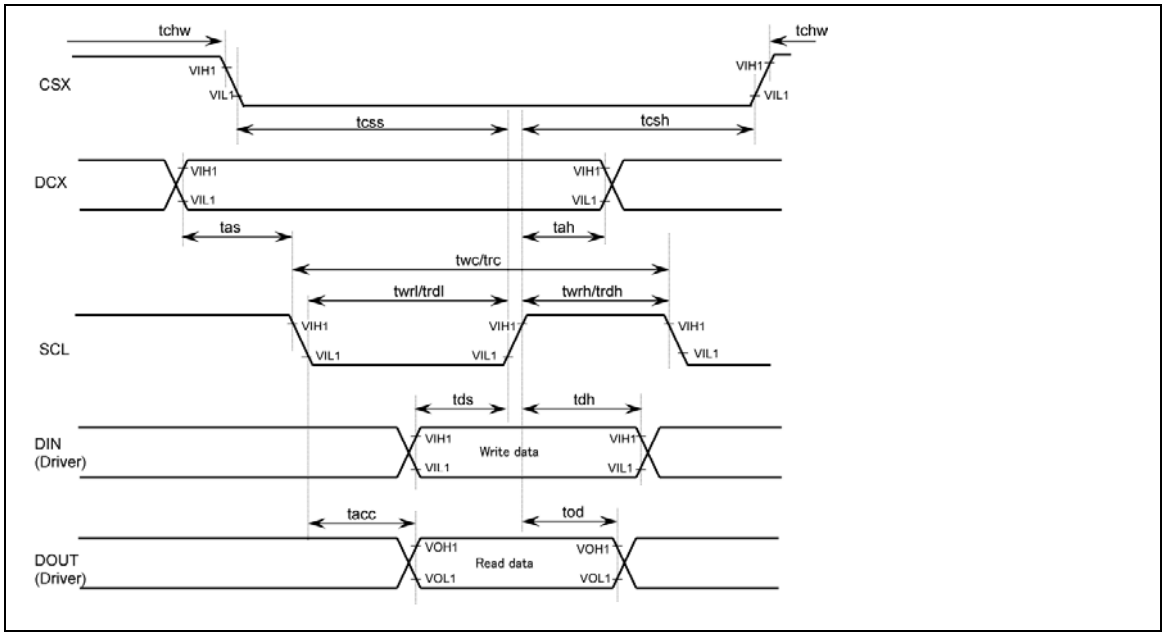


Figure 153 MIPI DBI Type C Timing

MIPI DPI Timing Characteristics (IOVCC1=1.65V~3.30V, Ta=-40℃~+85℃) (TBD)

Table 81

Item	Symbol		Unit	Test Condition	Min.	Max.
VSYNC setup time	VSYNC	tvss	ns		6	-
VSYNC hold time		tvsh	ns		8	-
HSYNC setup time	HSYNC	thss	ns		6	-
HSYNC hold time		thsh	ns		8	-
DE setup time	DE	tdes	ns		6	-
DE hold time		tdeh	ns		8	-
Pixel clock cycle time	PCLK	tpclkcyc	ns		TBD.	-
Pixel clock “Low” period		tpclkl	ns		TBD.	-
Pixel clock “High” period		tpclkh	ns		TBD.	-
Data setup time	DB[23:0]	tds	ns		6	-
Data hold time		tdh	ns		8	-
Rise / Fall time	-	tr/tf	ns		-	2

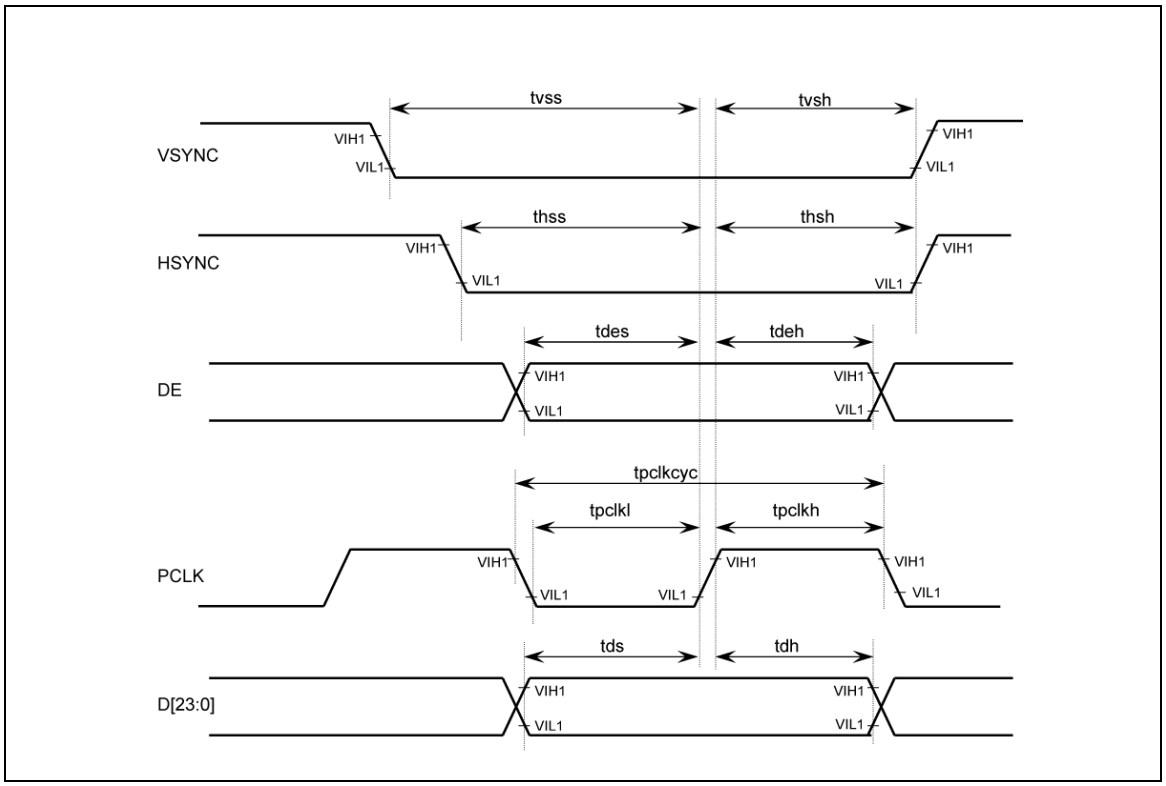


Figure 154 MIPI DPI Timing

Serial Interface Timing Characteristics (I2C)

Table 82 (IOVCC1=1.650V ~ 3.3V, Ta=-40°C ~ +85°C) (TBD.)

Item	Symbol	Unit	Min.	Typ.	Max.
Serial clock cycle time	t_{SCL}	ns	2500	-	-
Serial clock "High" period	t_{SCLH}	ns	600	-	-
Serial clock "Low" period	t_{SCLL}	ns	1300	-	-
Bus free time	t_{BUF}	ns	300	-	-
Start condition Hold time	t_{STAH}	ns	600	-	-
Restart condition setup time	t_{STAS}	ns	600	-	-
Stop condition setup time	t_{STOPS}	ns	600	-	-
Data setup time	t_{SDAS}	ns	300	-	-
Data hold time	t_{SDAH}	ns	0	-	-

Notes: 1. The line connected to the SDA pin requires an external pull-up resistor in I2C bus interface operation.
2. The output data delay time is based on the load condition compliant with I2C.

Serial Interface Operation

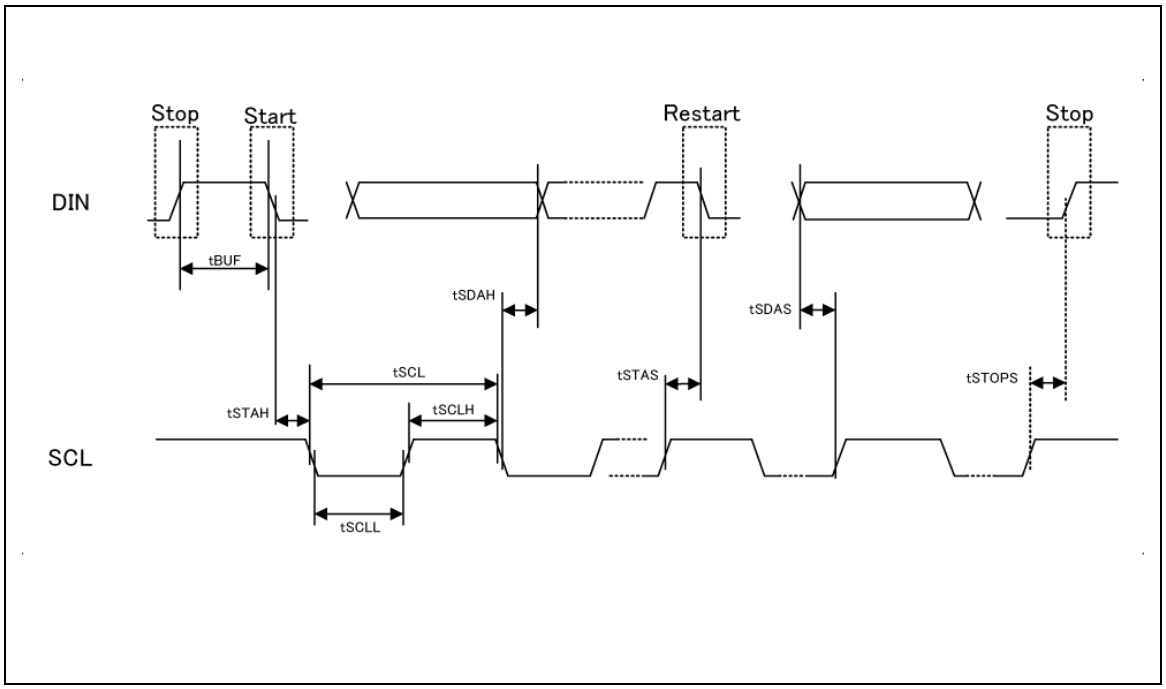


Figure 155 I2C Timing

HS-RX Clock and Data-Clock Specifications (IOVCC2=2.40V~3.30V, Ta=-40°C ~+85°C) (T.B.D.)

Table 83

Item	Symbol	Unit	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	100	-	250	4
DSICLK Cycle time	tCLKP	ns	4.0	-	10	
DSI Data Transfer Rate (Command mode)	tDSIR	Mbps	200	-	500	4
DSI Data Transfer Rate (Video mode)	tDSIR	Mbps	200	-	350	4
Data to Clock Setup Time	tSETUP	UI	0.15	-	-	
		ns	0.30	-	-	5
Clock to Data Hold Time	tHOLD	UI	0.15	-	-	
		ns	0.30	-	-	5

Note: 4. When tDSICLK≤125MHz, change auto load NV setting so that it is compliant with THS-PREPRare+THS-ZERO spec.

5. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.

LP-RX/TX Clock and Data-Clock Specifications (IOVCC2=2.40V~3.30V, Ta=-40°C ~+85°C) (T.B.D.)

Table 84

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40 ns + 4*UI	-	85ns + 6*UI	ns	
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns	
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (n*8*UI, 60 ns + n*4*UI)	-	-	ns	1,2
$T_{HS-EXIT}$	Time to drive LP-11after HS burst	100	-	-	ns	
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPTX}$				
$T_{TA-SURE}$	Time-out before new TX side starts driving	$1*T_{LPTX}$	-	$2*T_{LPTX}$		
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPTX}$				
T_{LPX}	Length of any Low-Power state period	50	-	-	ns	
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3	-	3/2		
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60 ns + 52UI	-	-	UI	3
$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	300	-	-	ns	
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI	
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns	
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of an HS transmission burst	60	-	-	ns	
T_{EOT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105 ns + n*12*UI		2
T_{LPTX1}	Length of Low-Power TX period in case of using DSI clock	-	16/fDSICLK	-	UI	4
T_{LPTX2}	Length of Low-Power TX period in case of using internal OSC clock	-	1/fosc	-	ns	

Notes: 1. If a > b then max(a, b) = a, otherwise max(a, b) = b
2. Where n = 1 for Forward-direction HS mode.

3. The R61529 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and delay. Due to the R61529 can work without the remained process if tCLK-POST is more than 256 UI.
4. The R61529 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled. Here, “fosc” is the frequency of oscillator clock, typical 14MkHz.

Timing Diagram

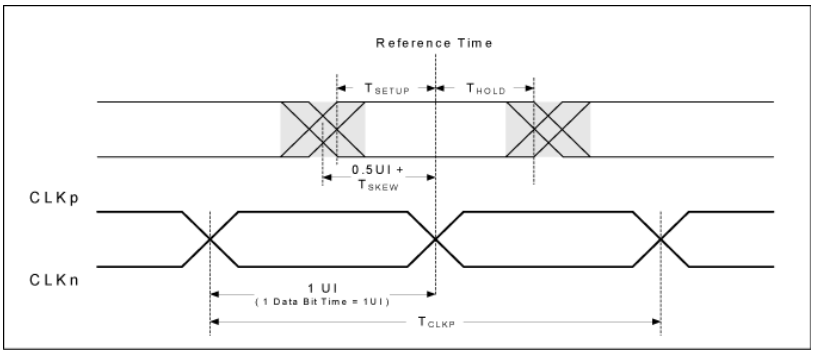


Figure 156 Data to Clock Timing Definitions

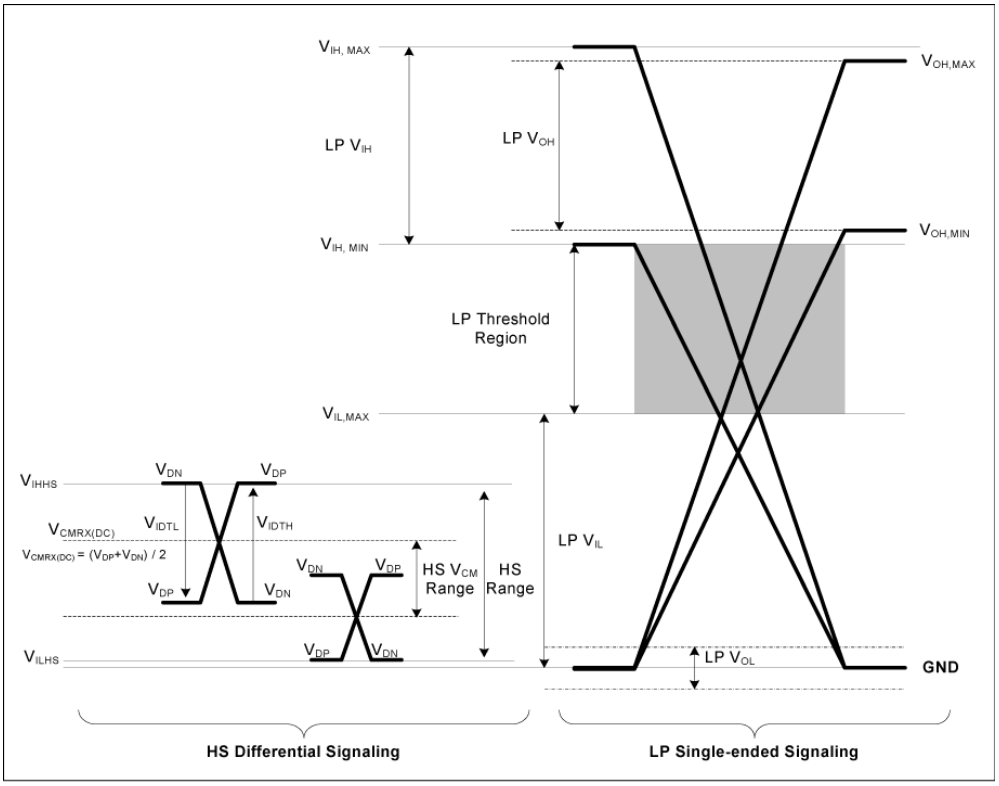


Figure 157 DSI LP mode

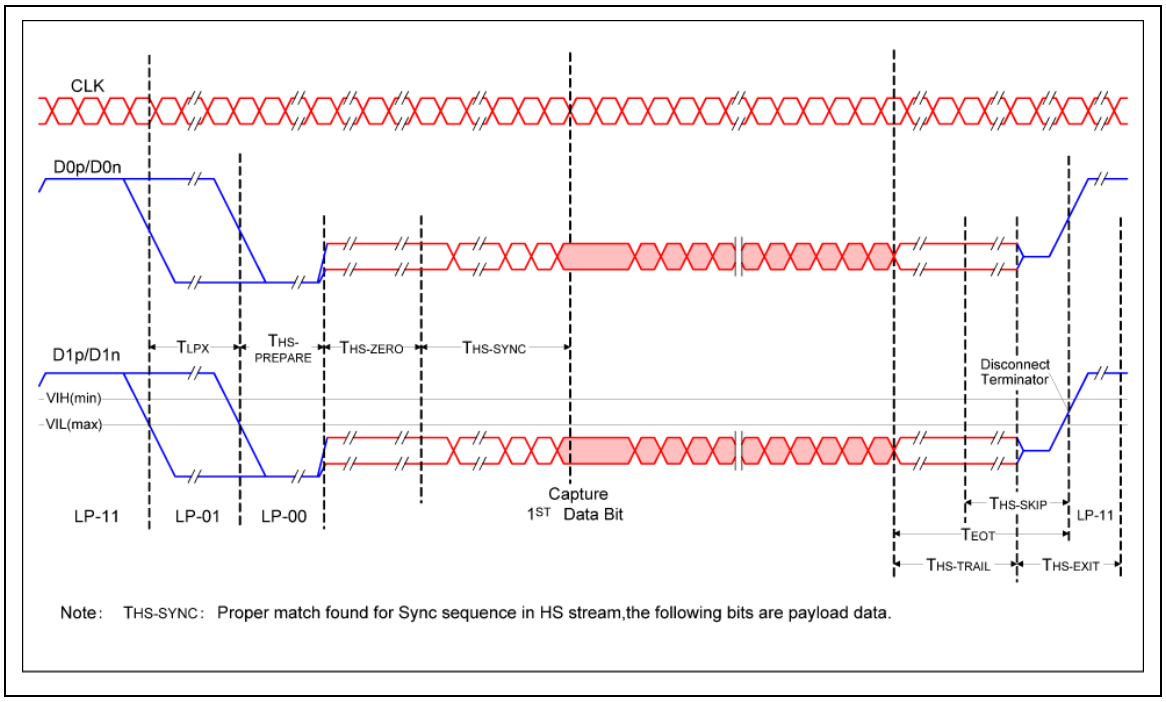


Figure 158 HS Data Transmission in Bursts

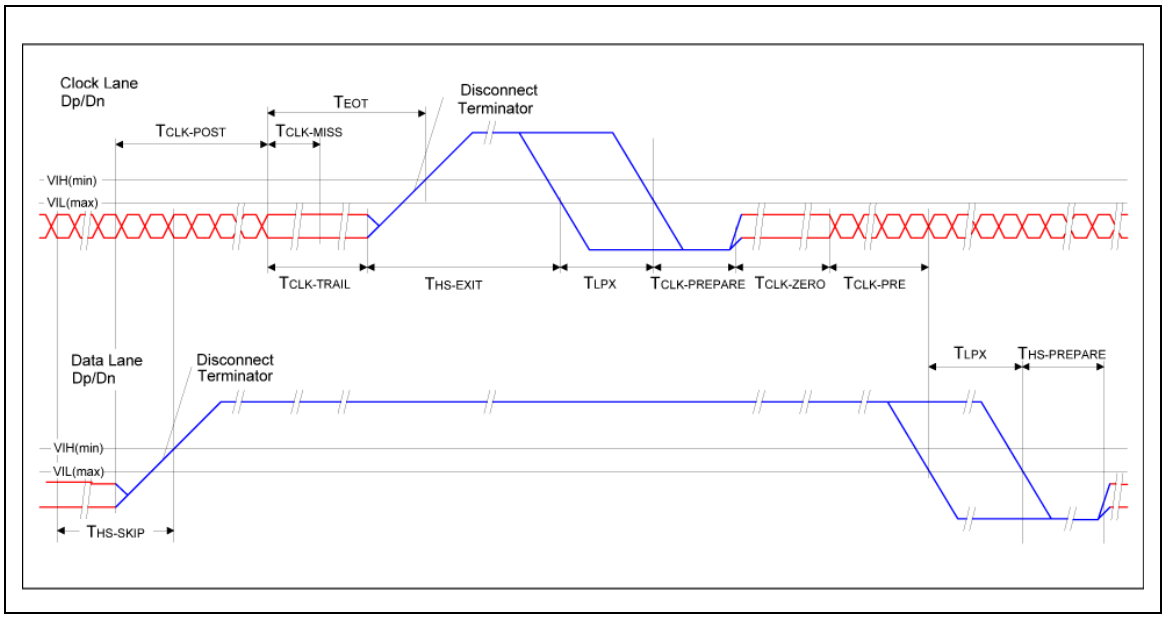


Figure 159 Switching the Clock Lane between Clock Transmission and LP mode

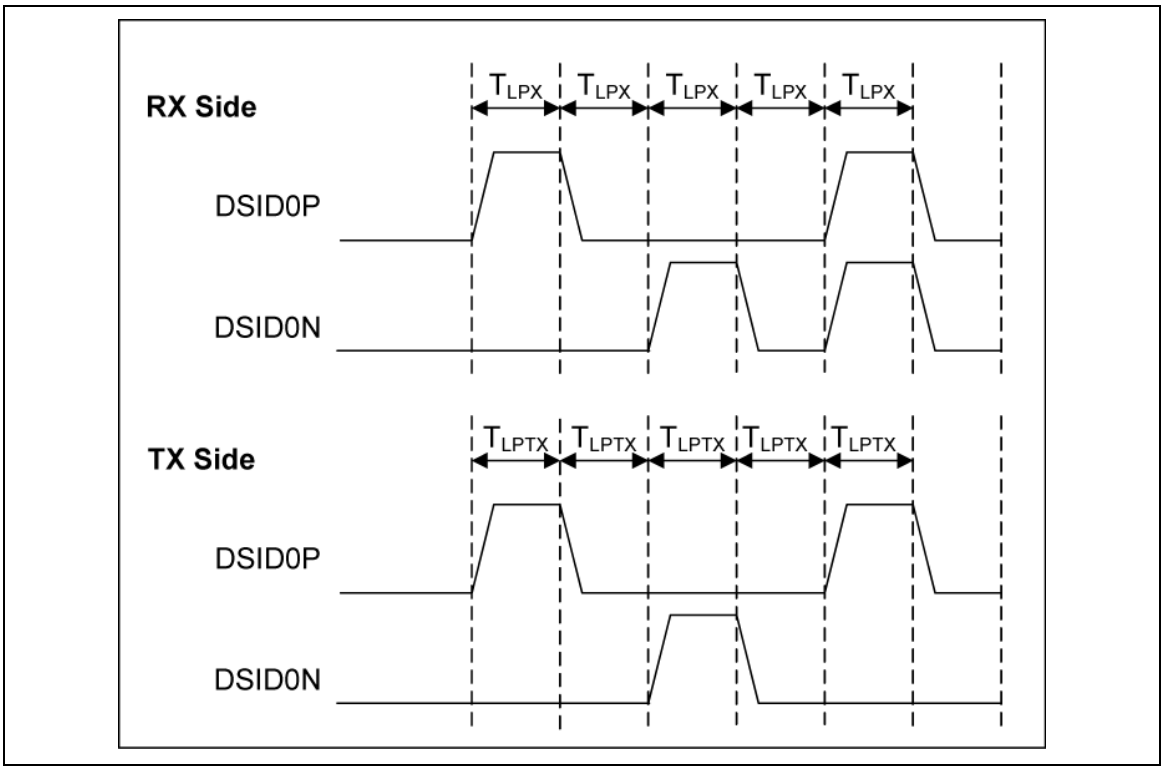


Figure 160 DSI LP mode

MDDI Interface Timing Characteristics

MDDI Receiver Timing Characteristics

(VCI= IOVCC2 = 2.40V ~ 3.30V, IOVCC1= 1.65V ~ 3.30V Ta=-40℃~+85℃) (TBD.)

Table 85

Item	Symbol	Unit	Min.	Typ.	Max.
Data transfer rate (Command mode)	1/tBIT	Mbps	10	—	400
Data transfer rate (Active Refresh mode)	1/tBIT	Mbps	10	—	250
Differential transfer input skew	|±tskew-pair-I|	ns	—	—	0.05
Data_Stb input skew	|±tdiff-skew-I|	ns	—	—	0.45*tBIT

MDDI Input Operation

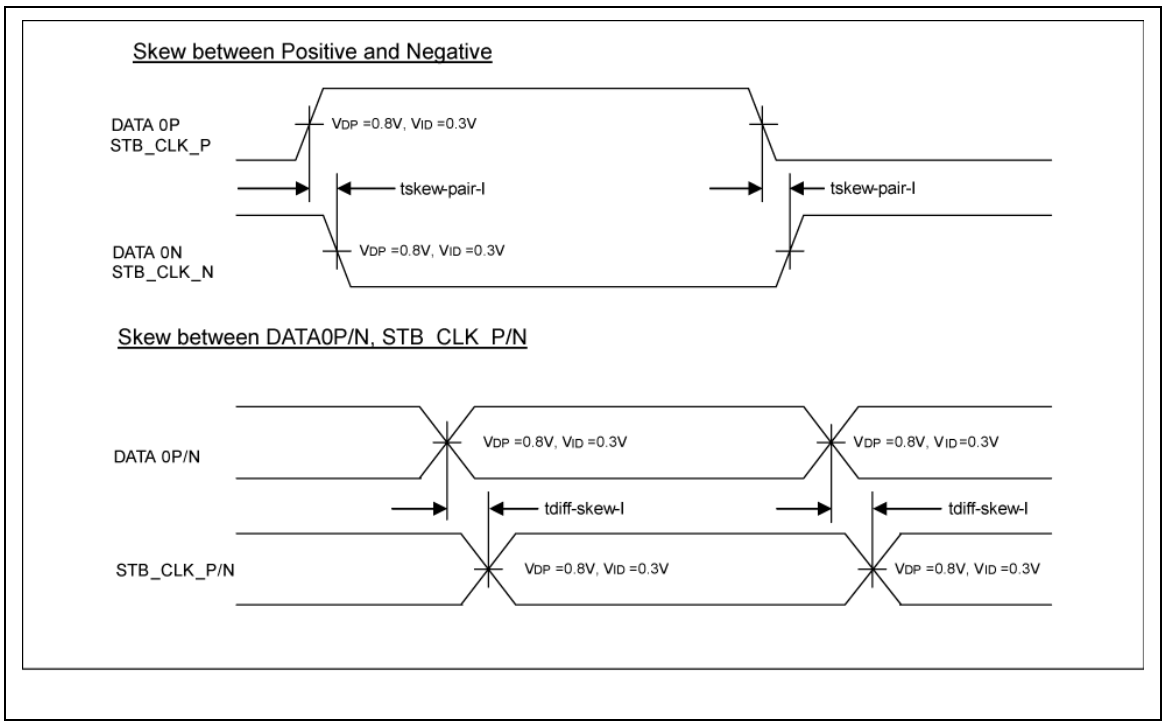


Figure 161 MDDI Input Operation

MDDI Transmitter Timing Characteristics

(VCI= IOVCC2 = 2.40V ~ 3.30V, IOVCC1= 1.65V ~ 3.30V Ta=-40℃~+85℃) (TBD.)

Table 86

Items	Symbol	Unit	Min.	Typ.	Max.
Data transfer rate(Reverse Link)	1/tBIT-Reverse	Mbps	0.15	—	12.5
Client output enable time (Turn Around 1 field)	tclient-enable	ns	0		16×tBIT-Reverse
Client output Disable time (Turn Around 2 field)	tclient-disable	ns	0		16×tBIT-Reverse

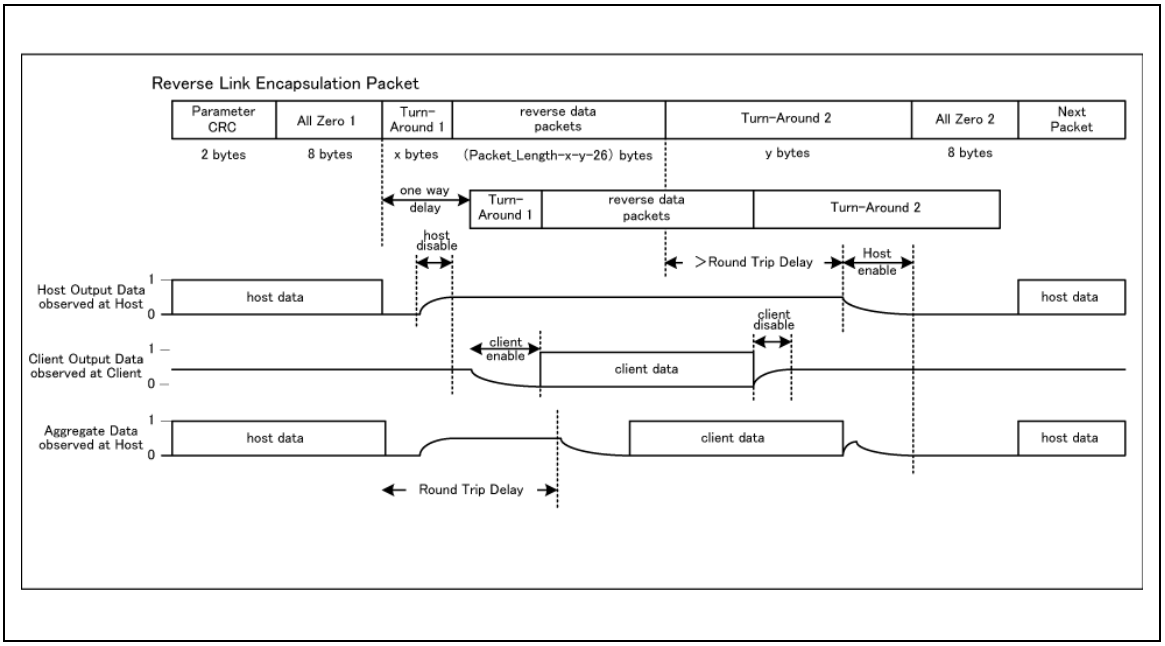


Figure 162 MDDI Output Operation Overview image

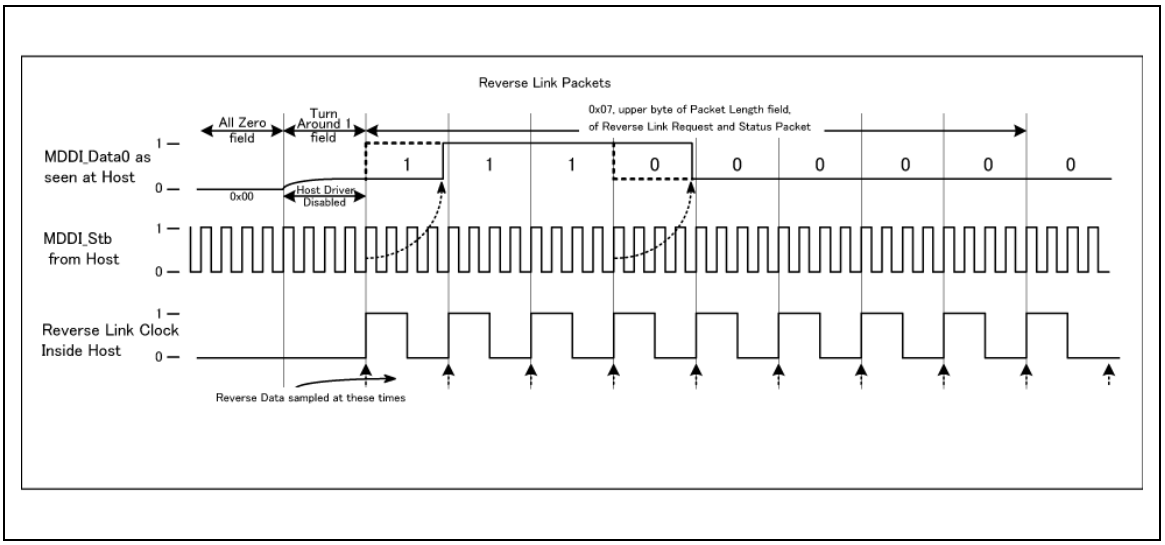


Figure 163 MDDI Output Operation Detail Image (Reverse rate Divisor[7:0]=2h case)

Notes to Electrical Characteristics

Notes: 1. DC/AC electrical characteristics of bare die and wafer are guaranteed at +85°C.

2. The following figures illustrate the configurations of input, I/O, and output pins.

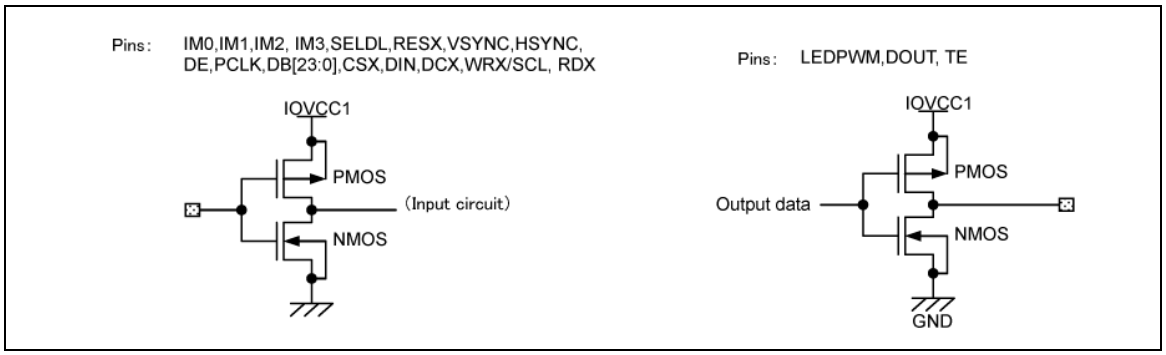


Figure 164 Pin circuit configuration

3. TEST[1:5] and VPP1 shall be fixed to ground (GND), VREFC, VDDTEST and TSC shall be fixed to ground (AGND).
4. This excludes the current in the output drive MOS.
5. This excludes the current in the input/output units. Make sure that the input level is fixed because shoot-through current increases in the input circuit when the CMOS input is at a mid-level. The current consumption is unaffected by whether the CSX pin is “high” or “low” while not accessing via interface pins.
6. The output voltage deviation is the difference in voltages between output pins that are placed side by side in the same display mode. It is a reference value.
7. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for one chip with the same display data.

Revision Record

Rev.	Date	Page No	Contents of Modification
0.00	March 29, 2010		First issue

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