Product Technical Specification

AirPrime BC127 Series

SIERRA WIRELESS®

41110693
Rev 2

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Due to the nature of wireless communications, transmission and reception of data can never be guaranteed. Data may be delayed, corrupted (i.e., have errors) or be totally lost. Although significant delays or losses of data are rare when wireless devices such as the Sierra Wireless modem are used in a normal manner with a well-constructed network, the Sierra Wireless modem should not be used in situations where failure to transmit or receive data could result in damage of any kind to the user or any other party, including but not limited to personal injury, death, or loss of property. Sierra Wireless accepts no responsibility for damages of any kind resulting from delays or errors in data transmitted or received using the Sierra Wireless modem, or for failure of the Sierra Wireless modem to transmit or receive such data.

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Revision History

Revision number	Release date	Changes
1	March 2, 2017	Initial conversion to SWI template.
2	August, 2019	General rewrite

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1: Introduction

AirPrime BC127 Series modules (BC127, BC127-HD, BC-127EXT, BC127-EXT-HD) are highly flexible, low power, small form-factor Bluetooth® Audio modules that are Bluetooth Version 5.0 Certified.

Figure 1-1: BC127 Module

Note: This is an example image and does not represent the label used on commercial shipments.

1.1 Module Variants

Note: Unless indicated otherwise, "BC127" in this document refers to the entire BC127 module series.

Table 1-1: Module Variants

Models	Description
BC127	Class 2 Bluetooth 5.0 module with integrated chip antenna
BC127-EXT	Class 2 Bluetooth 5.0 module with external antenna connection
BC127-HD	Class 2 Bluetooth 5.0 module with integrated chip antenna & support for aptX HD® audio
BC127-HD-EXT	Class 2 Bluetooth 5.0 module with external antenna connection & support for aptX HD® audio

BC127 Series modules are shipped pre-flashed with the latest Melody firmware production build. Customers must confirm with distributors at time of order that they will receive the firmware build they require. For volume orders (≥1k modules), the modules can be shipped pre-flashed with custom firmware.

1.2 General RF/Module Features

The BC127 is a low-power, small form-factor self-contained Bluetooth 5.0 (BT) module.

With an embedded software suite, the BC127 is an ideal solution for developers who want to quickly and cost-effectively integrate BT5.0 functionality into their products.

Table 1-2 lists the module's supported wireless frequencies and modes, and Table 1-3 summarizes the key electrical specifications.

Table 1-2: Supported RF Frequencies

Technology	Band	Notes
Bluetooth	2.4 GHz (2.400–2.48 GHz)	BT 5.0 Dual Mode

Table 1-3: Electrical Specifications

Specification	Notes
Transmit Power	BER/EDR Class 2 < 4 dBm, BLE < 10 dBm
RF Sensitivity	0.1% BER at -88 dBm GFSK
Operating Range	20–30 m
Supply Voltage	3.3–4.7V DC (supports Li-ion battery voltage range)
Modulation	8 DPSK, PI/4 DQPSK, GFSK
Maximum Data Rate	3 Mbps (typical 1.6 Mpbs)
Audio DAC Resolution	16 bits
Audio DAC Output Sample Rate	8–90 kHz
Audio DAC SNR	96 dB
Audio Stereo Separation	-87.7 dB
Typical Current	15 mA (music streaming)
Typical Current (Idle)	< 1 mA (connectable)

1.3 Bluetooth

The AirPrime BC127 supports 2.4 GHz Bluetooth v5.0 features. Key features include:

- Dual Mode—Bluetooth and Bluetooth Low Energy (BLE)
- Backwards compatible with 1.1, 2.0, 2.1 + EDR and 3.0
- Embedded Bluetooth Protocol Stack
- Supports HFP, A2DP, AVRCP, PBAP and SPP
- Supports IAP1/IAP2 profiles for connection to iOS devices
- Simple UART and GPIO interface for command and control
- Can connect to external codecs with I^2S, PCM, SPDIF interface
- Includes aptX-HD™ license and algorithm on HD models

1.3.1 Applications

- Wireless speakers, docks and headsets
- SmartPhone-controlled audio systems
- Automotive infotainment systems
- Medical devices
- High-quality audio streaming
- Gaming accessories and MP3 players

1.4 Hardware Interfaces

- 2/4 Wire UART serial link
- RF 50 Ω port (BC127-EXT, BC127-EXT-HD)
- RF integrated antenna (BC127, BC127-HD)
- I^2C peripheral
- GPIOs
- USB High Speed controller
- Capacitive touch sensor
- 3x LED drivers
- USB
- Analog I/O for analog voltage sense/drive
- External high current battery charger
- Internal vattery charger
- Audio peripherals:
  - I^2S/PCM, digital microphone interface (PDM)
  - SPDIF

1.5 Physical Dimensions and Connection Interface

AirPrime BC127 modules are compact, robust, fully shielded modules with the dimensions noted in Table 1-4.

Table 1-4: Module Dimensions

Parameter	Value	Tolerance	Units
Length	18	±0.10	mm
Width	11.8	±0.10	mm
Thickness	3.2	±0.20	mm
Weight	1.1	±0.10	g

AirPrime BC127 modules are LGA form-factor devices. All electrical and mechanical connections are made through peripheral half-moon castellation vias and associated land pads (Table 1-5) on the back side of the module.s

Table 1-5: LGA Pad Types

Pad Type	Quantity	Dimensions	Pitch
Signal & Ground Pads	51 peripheral pads (BC127, BC127-HD)	Refer to Figure 3-9/Figure 3-10 on page 27.	0.8mm
	54 peripheral pads (BC127-EXT, BC127-HD-EXT)		

2: Functional Specifications

2.1 Architecture

The following figures present an overview of the AirPrime BC127 module's internal architecture and external interfaces.

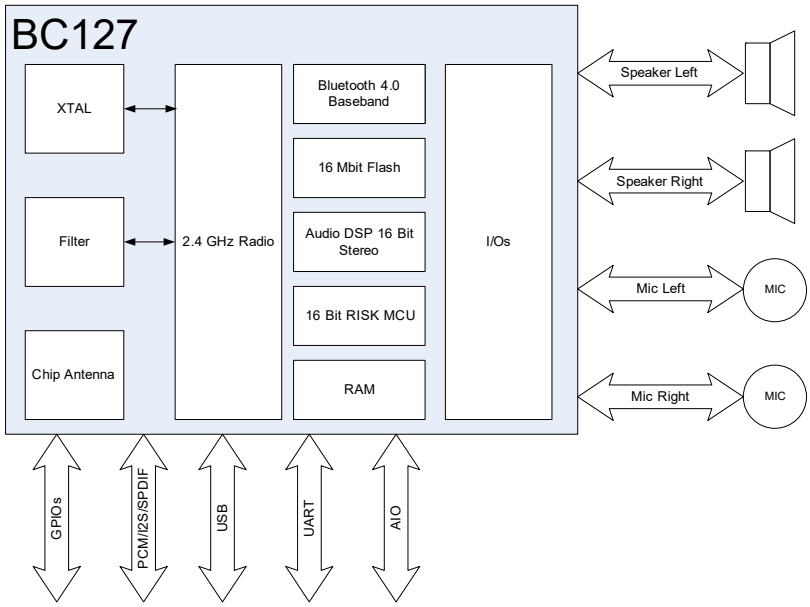

Figure 2-1: BC127 Block Diagram

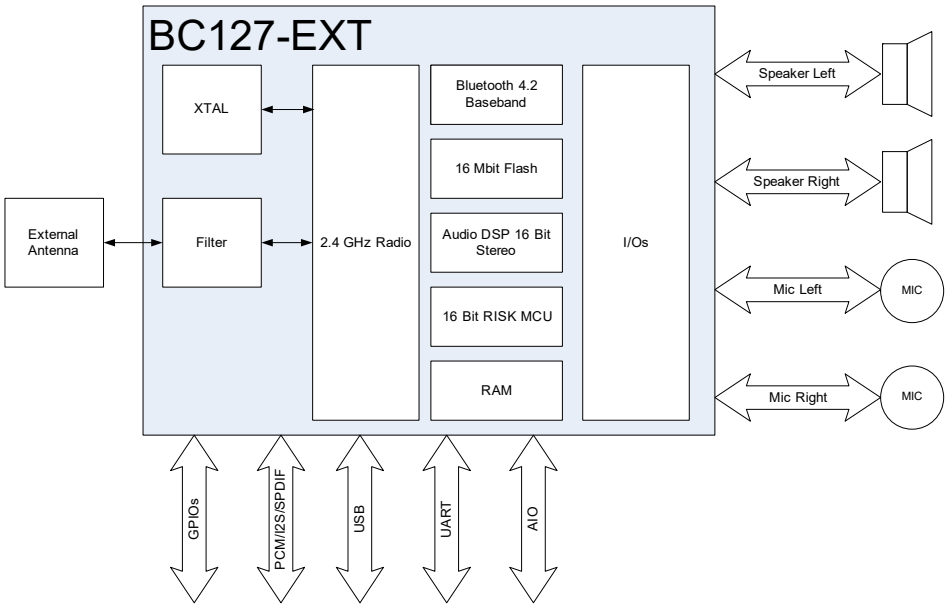

Figure 2-2: BC127-EXT Block Diagram

2.2 Features

Table 2-1 summarizes the AirPrime BC127 module's RF (Bluetooth), Power, software, and hardware capabilities.

Table 2-1: Module Capabilities

Feature	Description
Module	• FOTA (Firmware update Over The Air)

Bluetooth	• BT Dual Mode v5.0
	• Data Rates:
	  • 1 Mbps (BR)
	  • 2 Mbps (EDR)
	  • 3 Mbps (EDR)
	  • 1 Ms/s (LE)
	• BT low-energy mandatory features

Power Management	• 3.3–4.7 V DC (supports Li-ion battery voltage range)
	• LDO regulators with automated low current modes
	• 3.3 V regulated supply for external components (USB only)
	• Current Consumption:
	  • Active: 15 mA (music streaming)
	  • Idle: <1 mA (connectable)
	• Automated peripheral power management
	• Wake Functions:
	  • Wake on Reset
	  • Wake on RTC
	  • Wake on GPIO

3: Technical Specifications

3.1 Environmental

The environmental specifications for operation and storage of the AirPrime BC127 are defined in Table 3-1.

Table 3-1: Environmental Specifications

Parameter	Range
Ambient Operating Temperature	-40°C to +85°C
Ambient Storage Temperature	-40°C to +105°C (recommended)

3.2 Power Supply Ratings

The AirPrime BC127 is designed for battery-powered applications and contains an internal charging circuit that can be used to charge batteries from a fixed voltage, typically from a USB source. Table 3-2 describes the power supply pins, their recommended voltage range and functionality.

Note: Operation above the maximum specified operating voltage (Table 3-2) is not recommended and specified typical or functional operation of the device is neither implied nor guaranteed.

Table 3-2: Power Supply Pins

Pin	Name		Voltage (V)			Direction	Function
			Min	Typ	Max		
29	CHG_EXT		4.35	-	5.5	Output	Battery Charger Voltage Output when using an external bypass transistor for high current fast charging circuit. Leave Open Circuit if external charging circuit is not used.
30	VCHG	Reduced spec.	3.1	-	4.75	Input	Input voltage for charger circuit and 3V3_USB internal LDO.
		Full spec.	4.75	-	5.75		
31	VBAT_SENSE		0	-	4.3	Input	Battery Voltage Sense Input.
32	VBAT		2.8	-	4.3	Input	Main supply input powered from a battery.
33	VDD_PADS		1.7	3.3	3.6	Input	Main Digital Power Domain Reference voltage Input.
34	3V3_USB		3.2	3.3	3.4[a]	Output	Regulated 3.3 V supply available to supply peripheral devices when module is powered from VCHG.

a. VCHG input >4.25V, capable of sourcing 250 mA max.
Reduced current source capability when 4.25V > VCHG > 3.1V.

3.2.1 Power Supply Considerations operating from Battery

3.2.1.1 Example circuit

Figure 3-1 describes a typical battery-operated circuit used for headset applications.

- A single cell Li-Ion battery supplies the BC127 module's VBAT and VBAT_SENSE (connected together). If the battery has a high ESR, a filter circuit R1//C1 is required for stability.
- VDD_PADS voltage is generated from VBAT and/or VUSB using a diode OR arrangement to drive the input of an external LDO regulator as shown in Figure 3-1. This dual input approach supports the charging of discharged batteries.
- In the absence of a VCHG voltage (i.e. when the battery is charged), the BC127 is started by a rising edge on VREGEN.

  VREGEN's reference voltage is VBAT and must be driven by an external controller. Once the module has booted, the firmware takes over and latches the internal regulators and supply domains on, and then VREGEN can be released.

  Typically (in headset applications) VREGEN is connected to an external button tied to VBAT. Pushing the button and then releasing it starts the module.

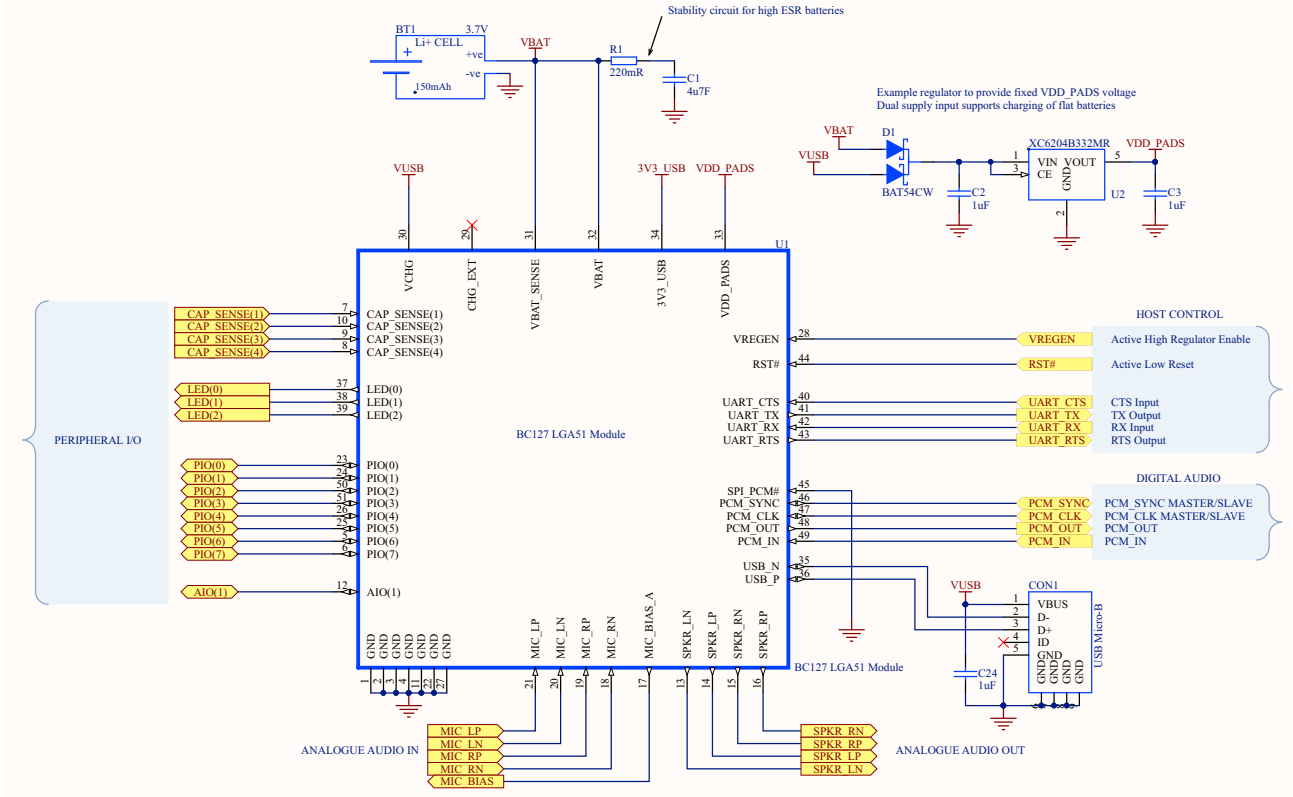

Figure 3-1: BC127 Battery Supply Internal Charger

3.2.1.2 Power-on

VREGEN can be tied to VBAT but an external delay of 5 ms is required between VBAT being powered and VREGEN being asserted high. A fast-rising edge on VREGEN must be provided to enable the module, the circuit in Figure 3-2 provides this fast-rising edge to enable the module to start when VREGEN is tied to VBAT.

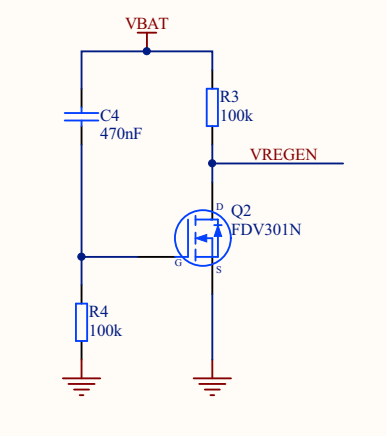

Figure 3-2: BC127 VREGEN Delay Circuit

3.2.1.3 Battery charging

To charge the battery, an external source connected to VCHG input is required, as shown in Figure 3-1. This source is provided by a USB Interface, connecting VUSB to VCHG to provide the source for the battery charging circuit.

When VCHG is connected (i.e. when wishing to charge the connected battery), the BC127 starts on the rising edge of VCHG. A minimum of 3.1V is required to start the module when started from VCHG.

The internal charger is capable of supply a maximum of 200 mA to charge the battery.

The charging functionality is set using the BATT_CONFIG command.

BATT_CONFIG=<enable charge> <critical level> <charge level> <temp level> <current>

- Parameters:
  - <enable charge>—ON to enable charging. OFF otherwise.
  - <critical level>—Critical battery level in units of 20 mV.
  - <charge level>—Charge level in mV.
  - <temp level>—Thermistor voltage limit in mV.
  - <current>—Charging current in mA in range 0 to 200.
- Usage notes:
  - <enable charge> should be OFF when not using a battery.
  - During use, the module shuts off if the battery voltage drops below <critical level>.
  - Charging will stop once the battery reaches <charge level> value.
  - Charging will stop if the thermistor voltage reaches <temp level> value.
  - Charging is disabled if <current> is set to 0.
  - The device supports various charging modes automatically.

3.2.2 Battery Charger Hardware Operating Modes

The battery charger hardware is controlled by the VM (virtual machine).

The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby—Fully charged or float charge
- Error—Charging input voltage (VCHG) is too low

The battery charger operating mode is determined by the battery voltage measured on VBAT_SENSE pin and charging current, as described in Table 3-3. The internal charger circuit can provide up to 200mA of charge current.

Table 3-3: Battery Charger Operating Modes by Battery Voltage and Current

Mode	Charger Enabled	VBAT_SENSE Voltage	Description
Disabled	No	n/a	Battery charger is fully disabled and draws no active current on any of its terminals. To enable the charger, use the AT command **BATT_CONFIG** (as noted in Battery charging on page 15).
Trickle charge	Yes	$0 < VBAT\_SENSE < V_{fast}$	• Current of approximately 10% of the fast charge current (I_{fast}) is sourced from VBAT. • V_{fast} threshold detection has hysteresis to prevent the charger from oscillating between modes.
Fast charge	Yes	$V_{fast} < VBAT\_SENSE < V_{float}$	• When VBAT_SENSE is in stated range, current sourced from VBAT increases to I_{fast}.(10–200 mA, set by BATT_CONFIG command's <current> parameter). • I_{fast}.remains constant until voltage at VBAT_-SENSE reaches V_{float}, then the charger reduces the current sourced to maintain a constant voltage on the VBAT_SENSE pin. • When the current sourced is below the termination current (I_{term}), the charging stops and the charger enters standby mode. I_{term}.is typically 10% of the fast charge current. *Note: I_{fast}.is calibrated in production test to correct for process variation in the charger circuit.*

Table 3-3: Battery Charger Operating Modes by Battery Voltage and Current (Continued)

Mode	Charger Enabled	VBAT_SENSE Voltage	Description
Standby	Yes	(I_{term}[a]) and ((V_{float} - <V_{hyst}) < VBAT_SENSE)	When the battery is fully charged, the charger enters Standby mode, but continues to supply I_{term} until the battery voltage (monitored on VBAT_SENSE) drops below (V_{float} - <V_{hyst}). When this occurs, the charger re-enters Fast charge mode.
Error	Yes	(VHG - 50 mV) < VBAT_SENSE	Charger enters error mode if the voltage on VCHG is too low to operate the charger correctly (VBAT_SENSE > VCHG - 50 mV (typical)). Charging is stopped in this mode. The charger does not require a reset to resume normal operation—it restarts automatically once the error conditions are removed.

a. I_{term} is approximately 10% of I_{fast} for a given I_{fast} setting.

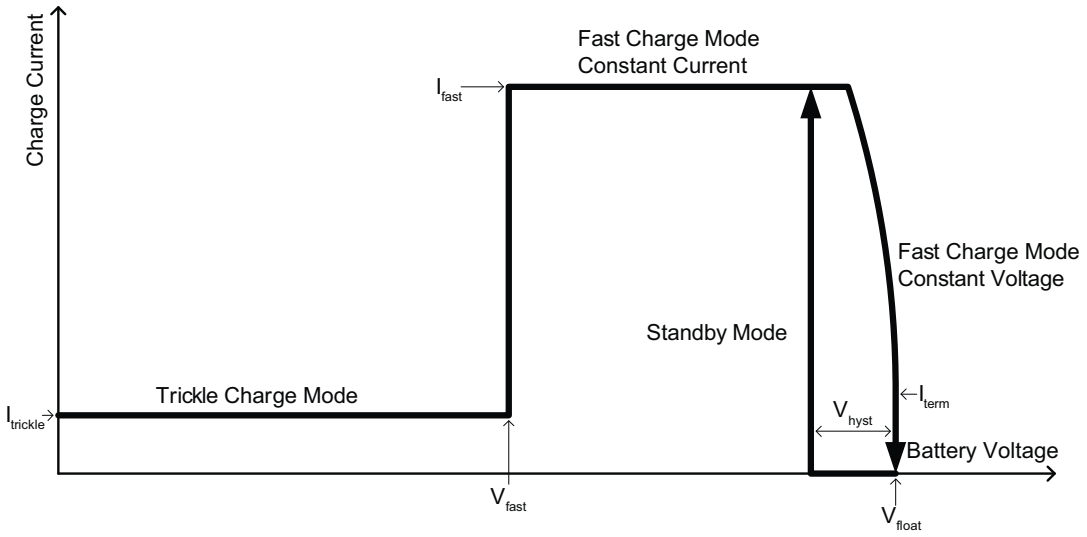

Figure 3-3: Battery Charger Mode-to-Mode Transition

Table 3-4: Transition Figure Parameter Definitions

Parameter	Value	Description
V_{hyst}	100–150 mV	
I_{fast}	0–200 mA	Max charging current as set using AT command **BATT_CONFIG**
I_{term}	~0.1 × I_{fast}	Termination current, approximately 10% of I_{fast}
V_{fast}	~2.9 V	Fixed voltage at which charger transitions from trickle to fast charge
V_{fast}	4.2 V ± 40 mV	Charger termination voltage

Figure 3-3 describes the mode-to-mode transition voltages. These voltages are fixed and calibrated by the BC127 module's internal CSR8670/CSR8675 device. Transition between modes can occur at any time.

3.2.3 Power Supply Considerations operating from a Fixed Voltage (no USB)

Figure 3-4 describes a typical circuit used by mains-powered Speaker applications, in which the BC127 module is supplied from a fixed voltage derived from a regulator within the customer's application.

- VSUPPLY in this case ranges from 2.8–4.3 V; typically 3.3 V is used to power the VBAT and VDD_PADS domains.
- 3V3_USB is not provided as an output since VCHG is not connected, however the internally circuitry does require a supply connection to the 3V3_USB pin.
- In the absence of a VCHG voltage input, the module is enabled by a rising edge on VREGEN. VREGEN reference voltage is VBAT and must be driven by an external controller. Once the module has booted, the firmware takes over and latches the internal regulators and supply domains on, and then VREGEN can be released. Typically in headset application VREGEN is connected to an external button tied to VBAT—pushing the button and then releasing starts the module. Alternatively, VREGEN is driven by a microprocessor or PIC on the customer application board.
- VREGEN can be tied to VSUPPLY but a 5 ms external delay is required between VSUPPLY being powered and VREGEN being asserted high. A fast-rising edge on VREGEN must be provided to enable the module. The circuit in Figure 3-2 provides this fast-rising edge to enable the module to start when VREGEN is tied to VBAT(VSUPPLY).

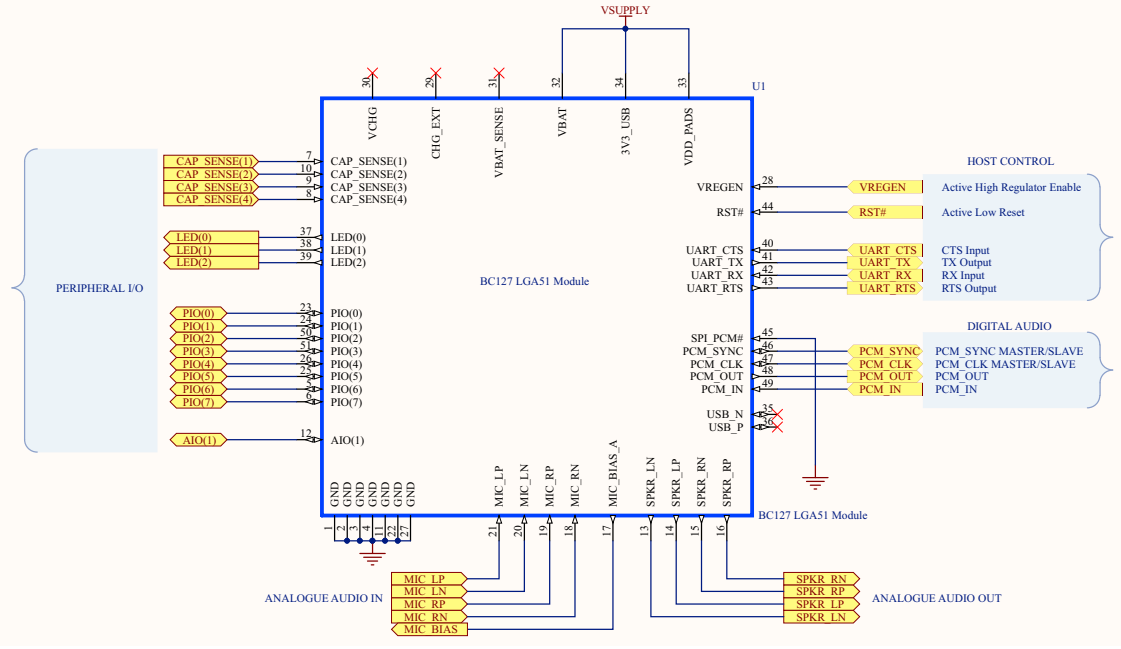

Figure 3-4: BC127 Fixed Voltage Configuration (No USB)

3.2.4 Power Supply Considerations operating from a Fixed Voltage with USB

Figure 3-5 describes a typical circuit used by USB-powered Speaker applications, in which the BC127 module is supplied from a fixed voltage derived externally from a USB source.

- VUSB from an External USB source is used to power the module.
- VCHG input voltage range is 4.75–5.75 V for full operational compliance providing 3V3_USB capable of driving up to 250 mA. Reduced operational compliance is supported down to 3.1 V where the source current from 3V3_USB is reduced (3.3 V voltage output is maintained).
- VDD_PADS is provided by a regulated voltage sourced from an external LDO on the Customer Application Board.
- 3V3_USB can be used to power external peripherals.
- When the External USB source is connected the module boots from the rising edge on VCHG. USB supplies with very fast rising edges or with limited transient current sourcing capabilities require an external filtering circuit as shown. Once the module has booted, the firmware takes over and latches the internal regulators and supply domains on.
- In this case VREGEN is not used to enable the module.

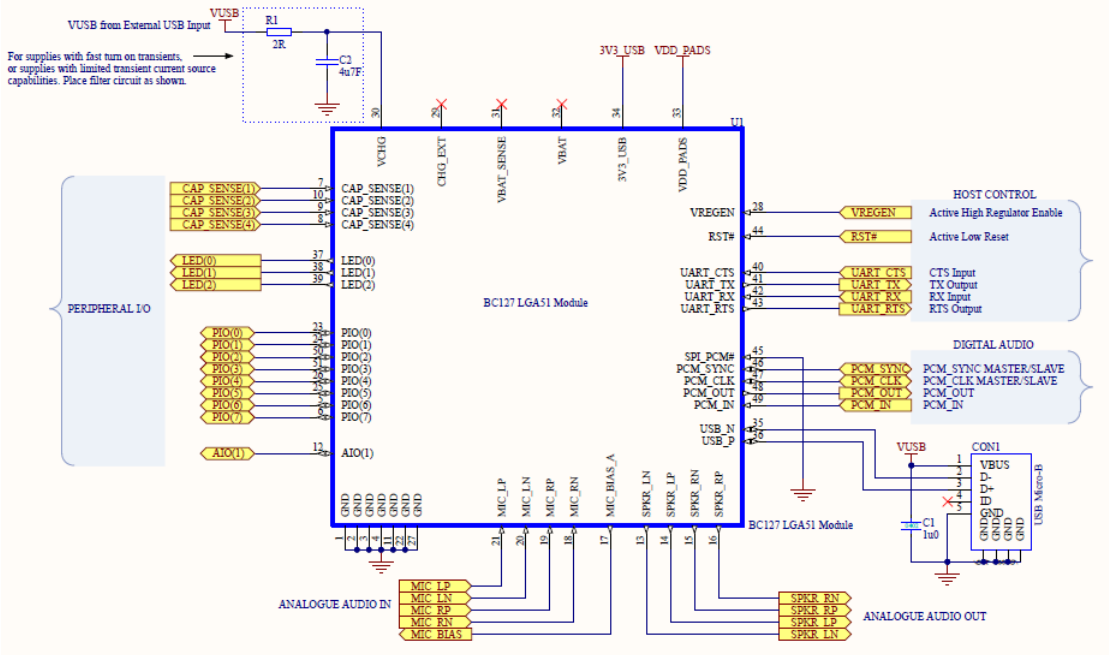

Figure 3-5: BC127 Fixed Voltage Configuration USB

The module power on sequence is sensitive to perturbation in the rising edge on the VCHG pin, the rising edge must be monotonic in the region from 1.6–3.1 V to ensure correct booting of the module. Non-monotonic transients can cause the module to latch into an undefined state and fail to power on completely. The only way to recover from this mode is to remove the supply, wait for 20 ms and reapply the supply to the device.

3.2.5 Reset

The AirPrime BC127 can be reset intentionally by two methods:

- Hardware reset via RST# pin
  - Reset—Pull the RST# low for > 5 ms to reset the module.
  - Power down—Pull RST# low for > 2.4 s to power down. A rising edge on VCHG or VREGEN is required to restart the module.
- Software reset via AT command—Send the AT command **RESET** over the UART interface to reset the module.

The AirPrime BC127 is reset unintentionally by:

- Power On/Down Reset—If the internal digital voltage domains (within the CSR8670/CSR8675 device) drop below a brownout threshold, the module will reset.
- Watchdog Reset—If the internal watchdog timer reaches an internal threshold value, the module will reset.

Note: The brownout threshold and watchdog timeout values are internal to the CSR8670/CSR8675 device and are not user-configurable.

The AirPrime BC127 includes an automatic reset protection circuit that restarts/resets the module when an unexpected reset occurs (e.g. ESD strike, lowering of RST# or watchdog timeout). This circuit enables resets from the VM without the use of external circuitry. The reset protection typically clears after 2 s (1.6 s (min) to 2.4 s (max)).

Table 3-5 describes the pull states of all digital pins upon device power-up or reset, and Table 3-6 defines the current consumption ranges for each state.

Table 3-5: Digital Pin States on Reset or after Power Up[a]

Pin Name/Group	I/O Type	State after Power Up or Reset
USB_DP	Digital bi-directional	N/A
USB_DN	Digital bi-directional	N/A
UART_RX	Digital bi-directional with PU	Strong PU
UART_TX	Digital bi-directional with PU	Weak PU
UART_CTS	Digital bi-directional with PD	Weak PD
UART_RTS	Digital bi-directional with PU	Weak PU
SPI_CS#	Digital input with PU	Strong PU
SPI_CLK	Digital input with PD	Weak PD
SPI_MISO	Digital tri-state output with PD	Weak PD
SPI_MOSI	Digital input with PD	Weak PD
SPI_PCM#	Digital bi-directional with PD	Strong PD
PCM_IN	Digital bi-directional with PD	Weak PD
PCM_OUT	Digital bi-directional with PD	Weak PD

Table 3-5: Digital Pin States on Reset or after Power Up[a] (Continued)

Pin Name / Group	I/O Type	State after Power Up or Reset
PCM_SYNC	Digital bi-directional with PD	Weak PD
PCM_CLK	Digital bi-directional with PD	Weak PD
RST#	Digital input with PU	Strong PU
PIO[7:0]	Digital bi-directional with PD	Weak PD

a. PD—Pull Down; PU—Pull Up

Table 3-6: Input and Tri-state Current Consumption

Input and Tri-state Currents	Min	Typ	Max	Unit
Strong pull up	-150	-40	-10	µA
Strong pull down	10	40	150	µA
Weak pull up	-5.0	-1.0	-0.33	µA
Weak pull down	0.33	1.0	5.0	µA

3.2.6 Role of VREGEN

Once the module has started, VREGEN acts like a standard GPIO. The function of VREGEN can be configured. Refer to the Melody Manual for the VREGEN function once the module has started.

3.2.7 Power Supply Sequencing

VBAT and VDD_PADS should be driven high at the same time, VREGEN must be delayed by at least 5 ms before driving high to enable the module (when required). RST# should be driven low for at least 20 ms to reset the module. It is not necessary to reset the module post power up.

The VBAT or VCHG ramp should be monotonic, any dips in the ramp profile in the region of 1.6–3.1 V may cause the module to power up incorrectly.

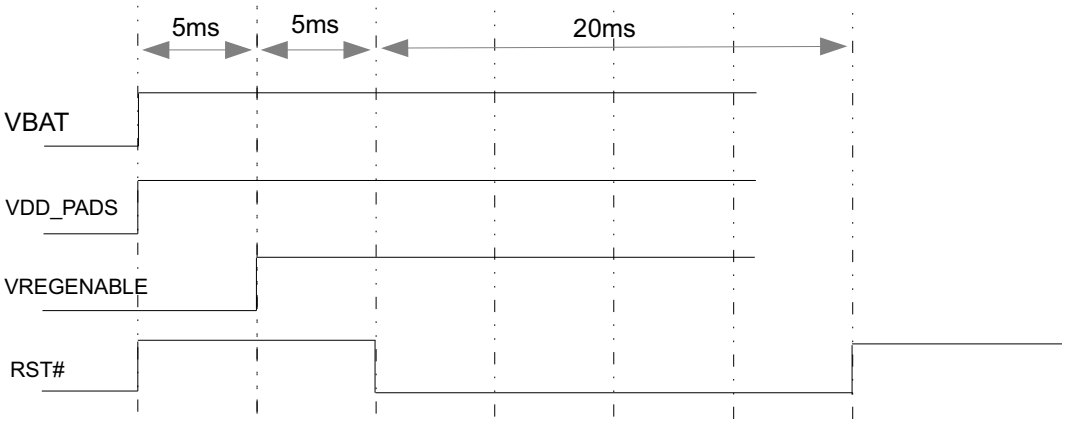

Figure 3-6: BC127 Power Supply Timing

3.2.8 Current Consumption

Table 3-7 provides current consumption measurements for the BC127's various operational modes, taken under the following conditions:

- Power supply—single 3.7 V input voltage on VBAT
- RF Tx power—0 dBm, referenced to antenna port into a 50 Ω load
- Ambient temperature—25°C
- HCI only
- No RF retransmissions in case of eSCO
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected
- AFH off

Table 3-7: Current Consumption

Role	State	Typ	Unit
N/A	Deep sleep, with host connection	62	µA
N/A	Page scan, Page=1280 ms interval; Window=11.25 ms	257	µA
N/A	Inquiry and page scan, Inquiry=1280 ms interval; Page=1280 ms interval; Window=11.25 ms	426	µA
Master	ACL Sniff=500 ms, 1 attempt, 0 timeout, DH1	151	µA
Master	ACL Sniff=1280 ms, 8 attempts, 1 timeout, DH1	137	µA
Master	SCO Sniff=100 ms, 1 attempt, PCM, HV3	9.7	mA
Master	SCO Sniff=100 ms, 1 attempt, mono audio codec, HV3	11.5	mA
Master	eSCO Setting S3, sniff=100 ms, PCM, 2EV3	7.6	mA
Master	eSCO Setting S3, sniff=100 ms, PCM, 3EV3	7.3	mA
Master	eSCO Setting S3, sniff=100 ms, mono audio codec, 2EV3	9.5	mA
Master	eSCO Setting S3, sniff=100 ms, mono audio codec, 3EV3	9.1	mA

Table 3-7: Current Consumption (Continued)

Role	State	Typ	Unit
Slave	ACL Sniff=500 ms, 1 attempt, 0 timeout, DH1	164	µA
Slave	ACL Sniff=1280 ms, 8 attempts, 1 timeout, DH1	160	µA
Slave	SCO Sniff=100 ms, 1 attempt, PCM, HV3	9.7	mA
Slave	SCO Sniff=100 ms, 1 attempt, mono audio codec, HV3	11.5	mA
Slave	eSCO Setting S3, sniff=100 ms, PCM, 2EV3	8.0	mA
Slave	eSCO Setting S3, sniff=100 ms, PCM, 3EV3	7.6	mA
Slave	eSCO Setting S3, sniff=100 ms, mono audio codec, 2EV3	9.8	mA
Slave	eSCO Setting S3, sniff=100 ms, mono audio codec, 3EV3	9.4	mA
Master	BLE Connected, 500 ms interval	158	µA
Slave	BLE Connected, 500 ms interval	157	µA
N/A	BLE Non-connectable, 1.28 s, 15 octet, 3 channels	103	µA
N/A	BLE Discoverable, 1.28 s, 15 octet, 3 channels	108	µA
N/A	BLE Connectable, 1.28 s, 15 octet, 3 channels	107	µA
N/A	BLE Scanning, 1.28 s, 11 ms, single frequency	254	µA

3.3 RF

3.3.1 Antennas

3.3.1.1 BC127/BC127-HD Antenna

The AirPrime BC127/BC127-HD includes an integrated ceramic antenna matched and optimized for performance in small PCB applications.

The module is designed to be placed on the edge or corner of the application PCB, with the following constraints:

- The area under and adjacent to the right-hand side of the module should have all ground and tracking removed as shown in Figure 3-7, and the hashed area should be cleared to the edges of the application PCB in the top right-hand corner.
- Any housing used to encapsulate the application PCB should not have any metal or metal coatings close to the antenna, to avoid detrimental detuning on the antenna and/or unwanted path loss.
- Ground vias should be placed along the edge of the cleared area to secure the ground planes on all layers together.
- The application PCB should have multiple ground vias throughout the entire area, tying ground planes together.

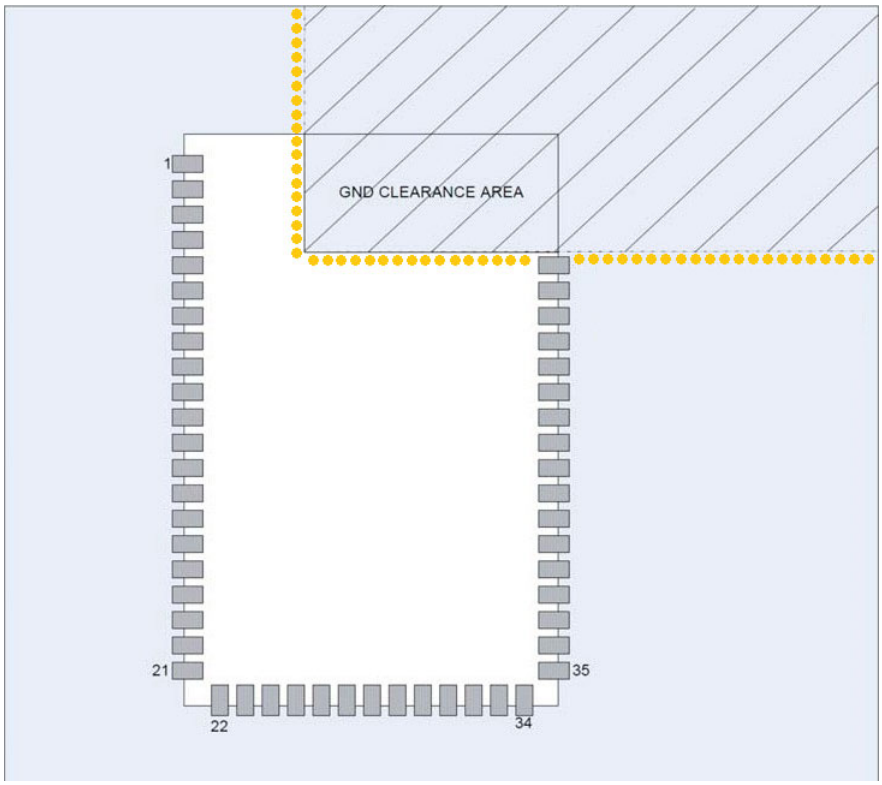

Figure 3-7: BC127/BC127-HD Application Placement Considerations

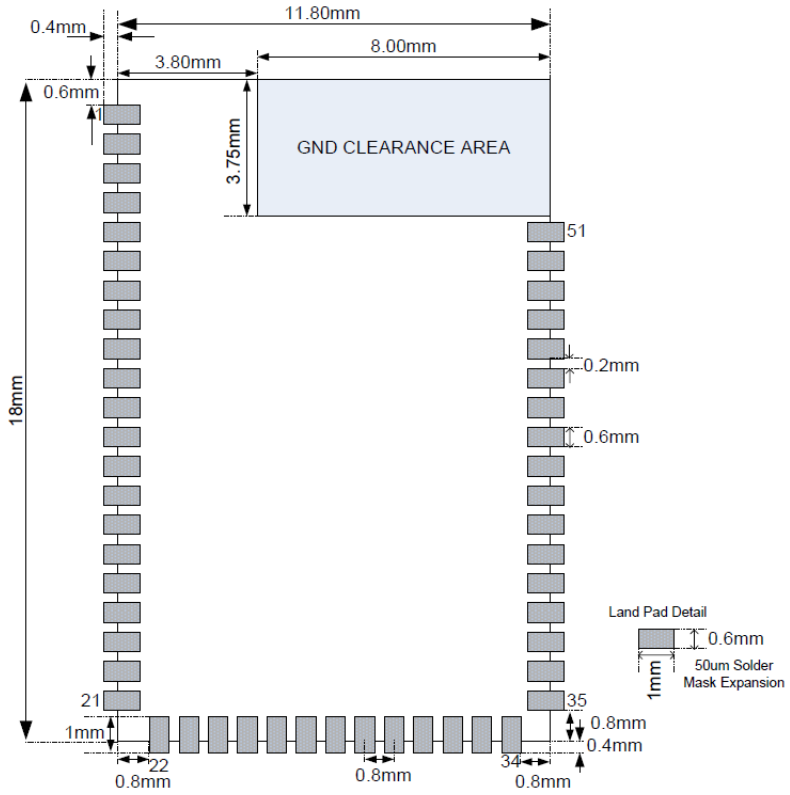

Figure 3-8: BC127 Module Footprint

3.3.1.2 BC127/BC127-HD Antenna

The BC127-EXT has an external RF port matched to 50 Ω on Pin 53, with adjacent ground pins 52 & 54. Use 50 Ω impedance transmission line techniques (stripline, microstrip or coplanar waveguide) to route from the 50 Ω pin to the application PCB antenna or external connector.

Avoid tracking RF near any sources of noise or digital interference.

3.4 Mechanical

The BC127 module's LGA footprint is a 51-pad or 54-pad array of copper pads (see Physical Dimensions and Connection Interface on page 9). The drawings below illustrate the device footprint and dimensions.

3.4.1 Mechanical Drawings

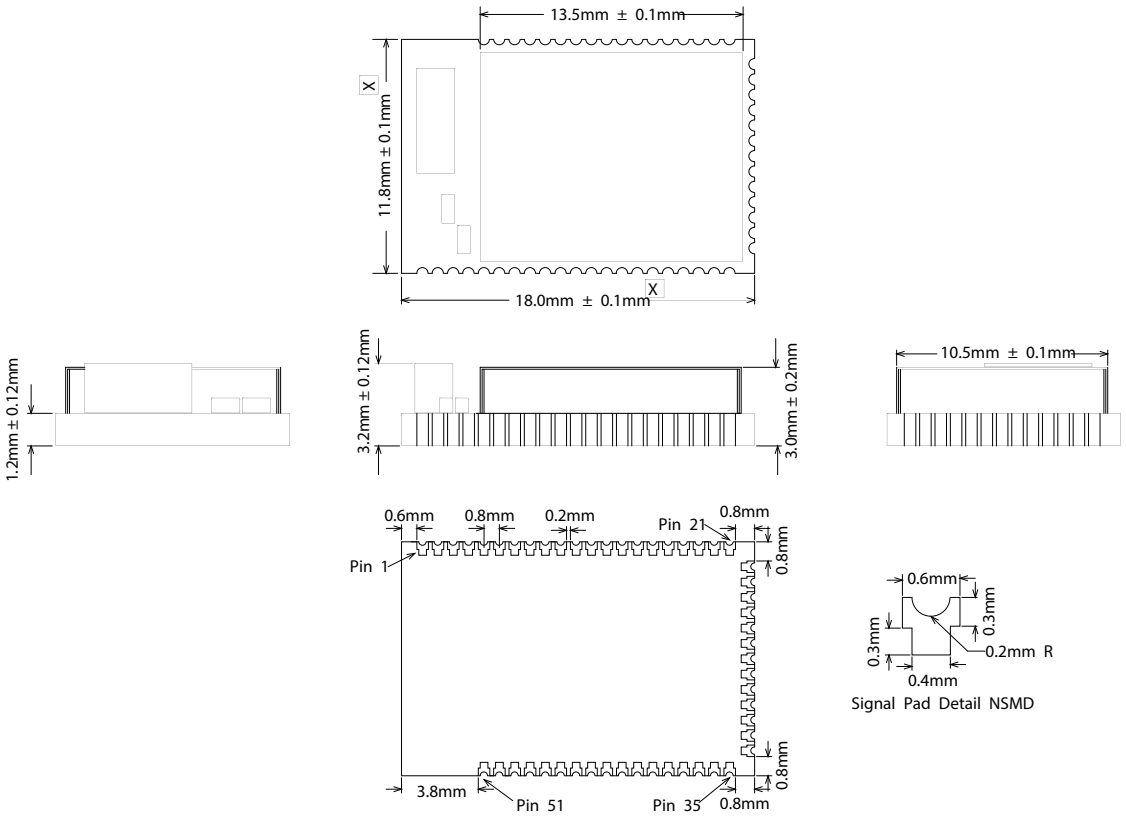

Figure 3-9: BC127, BC127-HD Mechanical Drawing

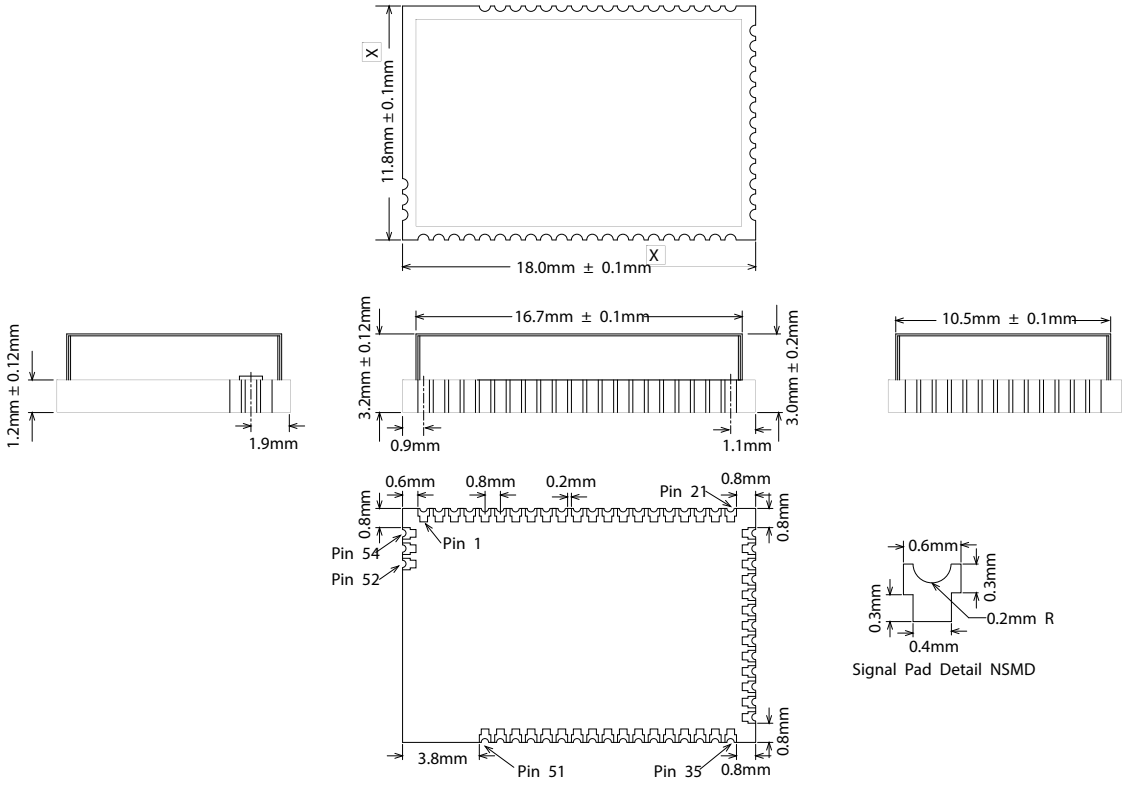

Figure 3-10: BC127-EXT, BC127-EXT-HD Mechanical Drawing

4: Interfaces Specification

4.1 Overview

This section describes the interfaces supported by the AirPrime BC127 embedded module and provides specific voltage, timing, and circuit recommendations for each interface.

4.2 UART

The AirPrime BC127 provides one UART interface for asynchronous communication between the module and a host device (e.g. a PC or host processor):

- UART0—4-wire, RS-232-compliant interface
- Full-duplex operation
- Automatic flow control
- Parity checking
- Up to 1 Mbps Baud Rate

Table 4-1: UART Interface

Pin #	Name	Description	I/O	Details
40	UART_CTS	UART Clear to Send	Input	Supply domain: VDD_PADS
41	UART_TX	UART Transmit	Output	
42	UART_RX	UART Receive	Input	
43	UART_RTS	UART Request to Send	Output	

Note: UART signals are named with respect to the module, and directions are listed with respect to the module. For example, UART_TX is an output from the module to the host.

The UART interface is configurable via the AT command **UART_CONFIG**:

- Default configuration—9600 (baudrate), 8 bit, no parity, no handshaking
- Baudrate considerations:
  - Supported rates—9600, 19200, 38400, 57600, 115200, 230400, 460800, 961200
  - Baud rates are persistent post-reset.

4.3 USB

The AirPrime BC127 provides one USB 2.0 interface:

- Full-speed (12 Mbps) device fully compliant to Universal Serial Bus Specification Revision 2.0, including the following engineering change notices (ECNs) issued by USB Implementers Forum.
  - Pull-up/pull-down Resistors ECN
  - 5 V Short Circuit Withstand Requirement Change ECN

- Integrated USB transceiver (PHY)
- Software controlled on-chip pull-up on D+
- Endpoints:
  - 2 control (1 IN, 1 OUT)
  - 14 bulk/interrupt (7 IN, 7 OUT)
  - 2 isochronous (1 IN, 1 OUT)
- Supports double buffering for isochronous (ISO) endpoints (IN/OUT)
- Supports USB suspend, resume, and remote wake-up
- 64 bytes buffer size for each bulk/interrupt endpoint
- Up to 1023 bytes buffer size for ISO endpoints

Table 4-2: USB Interface

Pin #	Name	Description	I/O	Details
35	USB_D-	USB Data negative	Input	• Supply Domain USB_3V3 • USB_VBUS connected to VCHG
36	USB_D+	USB Data positive	Input	

4.4 Audio

The Audio circuit consists of:

- Two independent 16-bit high-quality ADC channels:
  - Programmable as either microphone or line input
  - Programmable as either stereo or dual-mono input
  - Each channel is independently configurable to be either single-ended or fully differential
  - Each channel has an analog and digital programmable gain stage
- A dual differential class A-B output stage. If a single-ended audio output is required, use an external differential to single-ended converter.

The main features of the interface are:

- Stereo and mono analog input for voice band and audio band
- Stereo and mono analog output for voice band and audio band
- Support for stereo digital audio bus standards such as I^2S
- Support for IEC-60958 standard stereo digital audio bus standards (e.g. SPDIF and S3)
- Support for PCM including PCM master codecs that require an external system clock

Figure 4-1 illustrates the analog audio circuit.

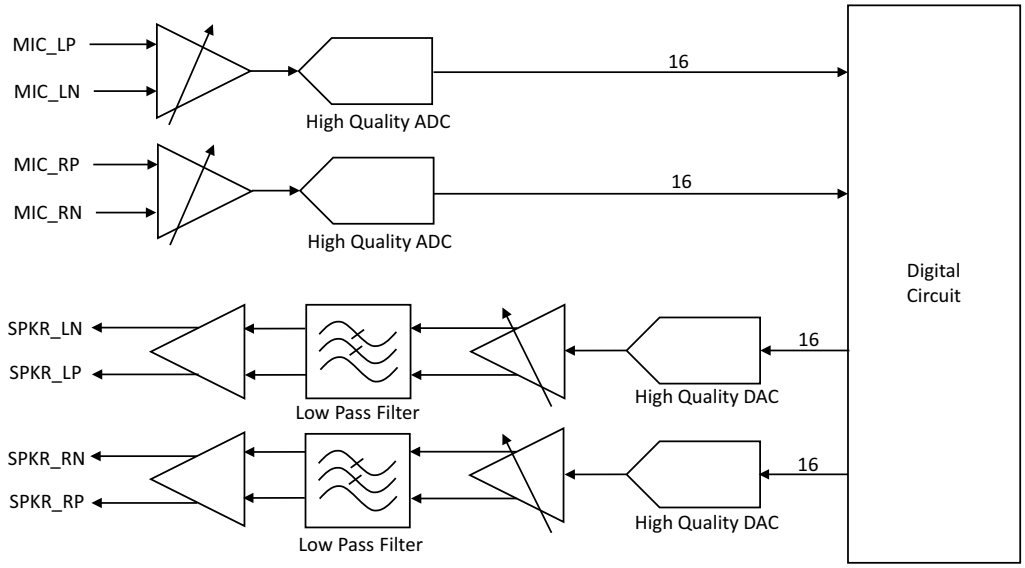

Figure 4-1: Analog Audio Circuit Diagram

4.4.1 Analog Audio Input: Microphones

Figure 4-2 and Figure 4-3 illustrate example microphone (mono and stereo) schematics:

- Stereo operation—Use both the left and right channels.
- Mono operation—Use only the left channel. Leave the right channel unconnected.
- Dual mono operation—The right channel forms the auxiliary channel. Connect as per the stereo example schematic.

By default, MIC_BIAS_A goes high for hands-free or music connections. To configure the behavior of MIC_BIAS_A (disabled, enabled always, enabled only when audio is required), refer to the Melody manual for configuration options.

MIC_BIAS_A has the following characteristics:

- Voltage—2.6 V supplied by VBAT or 3V3_USB.
- Current—70 µA to 2.8 mA, regulated by microphone bias generator, supporting 2 mA source typically required by 2 electret condensor microphones.
  If the microphone sink current is < 70 µA, the microphone output must be pre-loaded with a large value resistor to ground. (Note: The output does not require a decoupling capacitor.)
- Microphone input routed to high-impedance variable gain amplifier/buffer stage. An optional pre-amplifier is available for added gain.
  When the pre-amplifier is enabled, input impedance at MIC_LN, MIC_LP, MIC_RN and MIC_RP varies between 6 kΩ (pre-amplifier gain >0 dB) and 12 kΩ (pre-amplifier gain = 0 dB).
- R9 and R10 (shown in Figure 4-2 and Figure 4-3) set the microphone load impedance and are typically 2.2 kΩ.
- Audio input blocking capacitors—Analog audio input requires blocking capacitors to function correctly. Internal capacitors are available on some SKUs.
  - SKUs with integrated DC blocking capacitors (100 nF) used to reduce low frequency noise (e.g. wind noise) adversely affect the bass roll-off of the audio input.

- SKUs without integrated DC blocking capacitors—Customer application PCBs must include external capacitors (minimum 1 µF recommended), otherwise analog audio input will not function correctly.

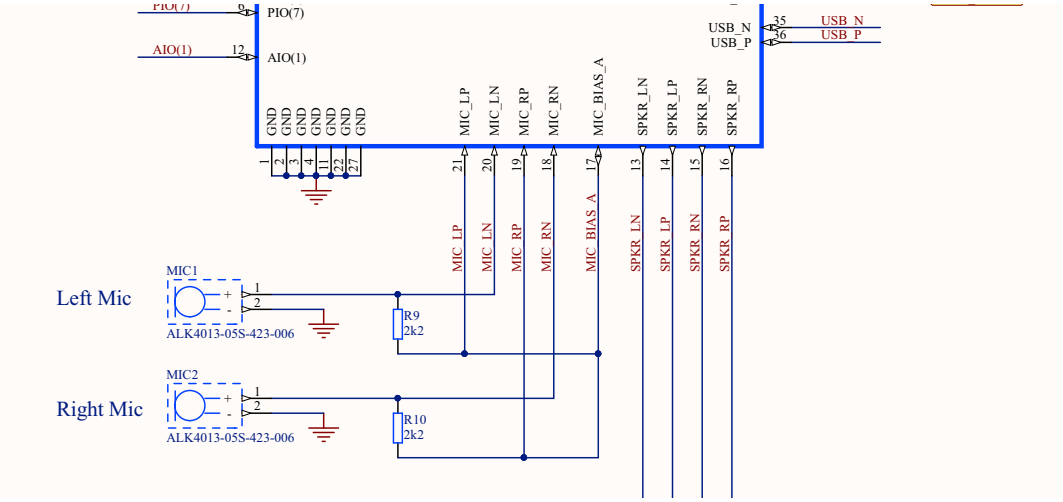

Figure 4-2: Stereo Microphone Example Schematic

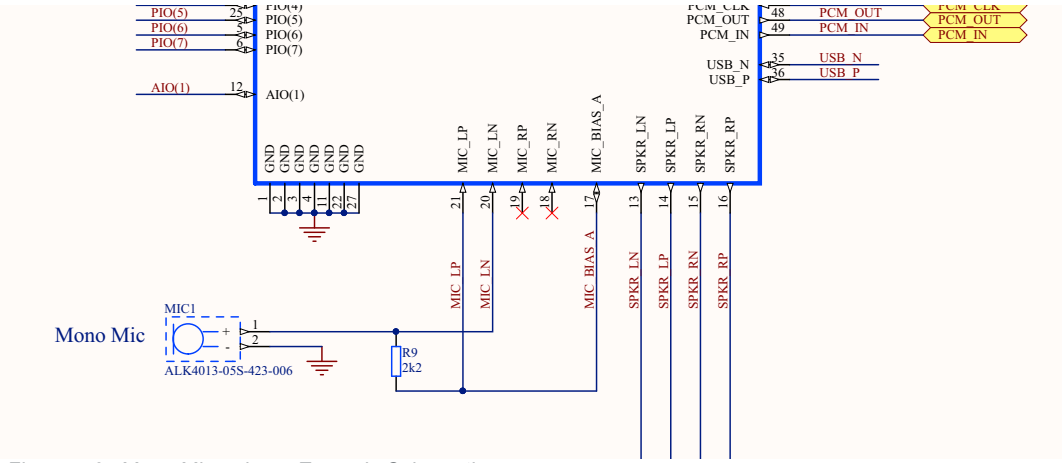

Figure 4-3: Mono Microphone Example Schematic

4.4.2 Analog Audio Input: Line In

The BC127 module supports LINE IN audio analog input signals. These can be configured by connection for single-ended or differential inputs, mono or stereo configuration.

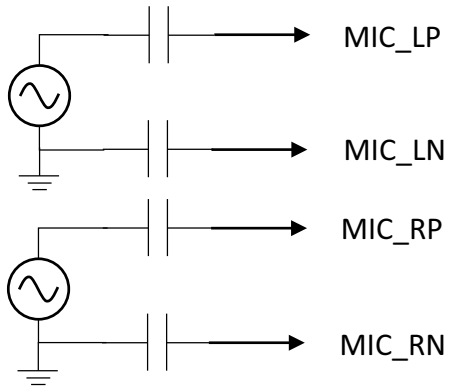

Figure 4-4: Line In single-ended input configuration

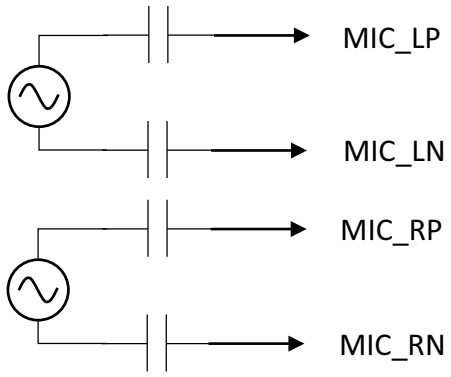

Figure 4-5: Line In differential input configuration

4.4.3 Analog Audio Output

The BC127 module's analog output circuit has the following characteristics:

- DC coupled
- Circuit comprises DAC, buffer with gain setting, low-pass filter, class AB output stage amplifier
- Differential signals—SPKR_LN/SPKR_LP (left channel), SPKR_RN/SPRK_RP (right channel)
- Load impedance—16–32 Ω
- Peak voltage output—Depends on gain setting.
  Worst-case peak-to-peak voltage—1.5 V; DC offset ~1.2 V at maximum gain

4.4.3.1 External Amplifier Support

The BC127 is designed to provide direct speaker drive and, if higher audio power is required, can drive an external amplifier.

- A PIO can be driven high when an audio link is active, and the PIO can be used to turn ON and OFF and external amplifier:
  - BC127 non-MFi builds—PIO3 is used by default.
  - BC127 MFi builds—Another PIO can be used to provide this functionality.

- Speaker outputs are DC coupled to the module's internal Bluetooth IC, and are referenced to 1.8 V.

For example, the AirPrime BC127 Series Discovery Board and the AirPrime BC127 Series Development Board both use external amplifiers for audio application demonstration purposes.

Application power supply design considerations:

- To enhance noise immunity, connect the BC127 to an external amplifier in a differential configuration, which rejects common mode noise.
- For best performance in audio applications, employ power supply filtering and layout grounding to mitigate power supply noise that can significantly degrade audio performance.

  This is especially important in USB powered applications or where a USB source is used to charge battery powered applications, since USB power supplies vary significantly with noise levels and supply stability.

  Good grounding and isolation of noise ground currents is essential for superior audio applications.
- In USB powered applications, in addition to the steady state noise levels from power supplies, plugging and unplugging of USB chargers can cause lareg supply transients that ripple through the supply chain to cause clicking and popping in the audio domain. Follow good noise immunity PCB design practices (e.g. ground isolation, short residual current return paths and the use of ferrite beads and large decoupling capacitors on USB supply connections) to mitigate these effects.

An example USB supply configuration is shown Figure 4-6:

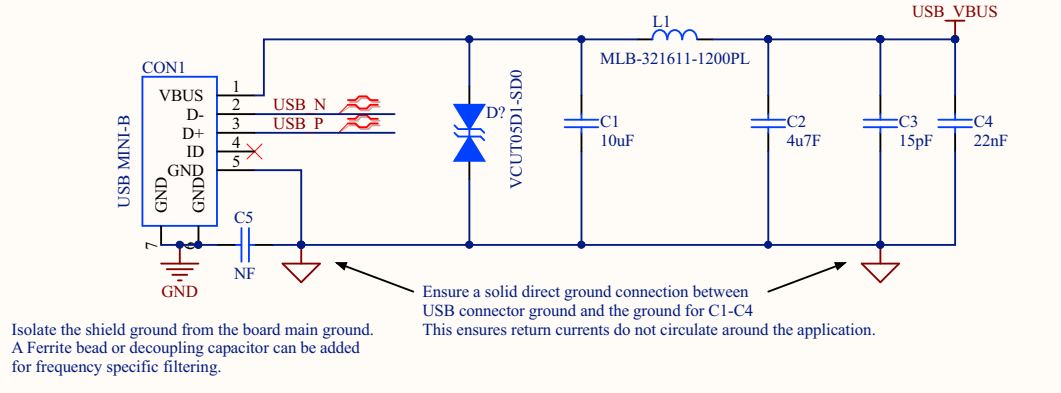

Figure 4-6: Example USB Supply Configuration

External amplifier selection and design considerations:

- For superior audio performance always follow the design and layout guidelines provided by the amplifier manufacturer.
- Always use a high quality audio amplifier that includes (ideally) built-in click and pop suppression circuits. These amplifiers use noise suppression and soft start techniques to filter supply noise and transients as well as minimizing ground loop currents and DC offsets that can cause degraded audio effects. Some amplifiers even employ ground sensing and suppression techniques to minimize and remove noise coupling to the audio path.
- Ensure the amplifier circuit is correctly grounded. For example, in the circuit in Figure 4-7 (used on the AirPrime BC127 Series Development Board), the amplifier audio ground (SGND) is connected to the main ground via a single "star" point at the

audio output jack. This is suitable for connection to headphones where noise from an external source is not expected.

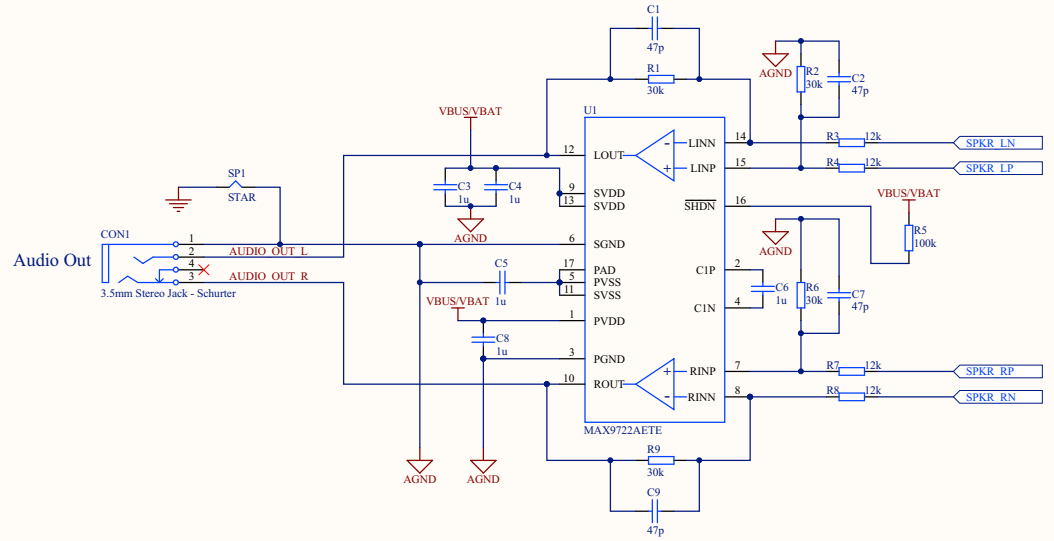

Figure 4-7: Example External Audio Amplifier Connection Suitable for Connecting to External Headphones

Important: *Because no two audio amplifiers are the same, it is important to ensure that you follow the design recommendations provided by the supplier of the amplifier.*

Audio design guidelines include:

- When connecting to external devices such as laptops in a "Line In" configuration, there is a possibility that the sleeve of the audio cable can carry noise derived from the laptop. Also external devices connected through the audio cable sleeve can have different ground potentials which causes currents to flow through the sleeve ground.

  In these cases, it is important to isolate the sleeve ground from the audio amplifier to avoid the noise coupling to the amplifier and degrading the signal source. To do this, add a filter circuit or ferrite bead connecting the sleeve ground to the ground on the application board as shown in Figure 4-8 below.

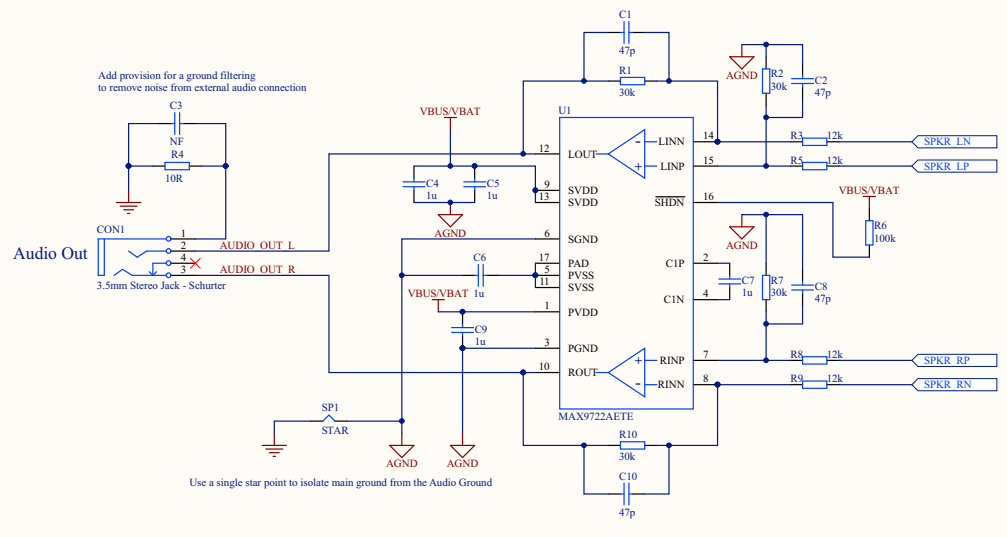

Figure 4-8: Isolating the Sleeve Ground from the Amplifier

- Some amplifiers do not support "capless" operation and require AC coupling on the amplifier's input and output. Series capacitance can introduce clicks and pops when the amplifier is turned on/off, as voltage transients occur across the capacitors causing audible spikes on the audio output.

  Choice of capacitors used in these configurations is important:
  - Avoid using ceramic capacitors as these tend to have high voltage coefficients.
  - Use low voltage coefficients capacitors such as tantalum or electrolytic capacitors to reduce low frequency distortion effects.
- In differential mode, the tolerance of the source and feedback resistors which set the gain of an amplifier is important. 1% resistors give a 40 dB CMRR whereas 0.1% resistors give a 60 dB CMRR. Use 0.1% resistor arrays for even better performance.
- The BC127 can be used to drive amplifiers in a single ended format. Simply terminate the positive differential outputs directly to the audio ground.

4.4.3.2 External Speaker Connections

The speaker lines (SPKR_LN, SPKR_LP, SPKR_RN, SPKR_RP) are internally DC blocked by 100 nF capacitors on the module to limit the low frequency response of the audio output. A version of the BC127 (V4) is available with these capacitors removed and therefore require external DC blocking capacitors on the customer's application, as shown in Figure 4-9. (If you require this hardware version, make sure you order the correct SKU.)

Select the capacitor values based on the low frequency response you wish to achieve in your application—1 uF is a typical suggested value.

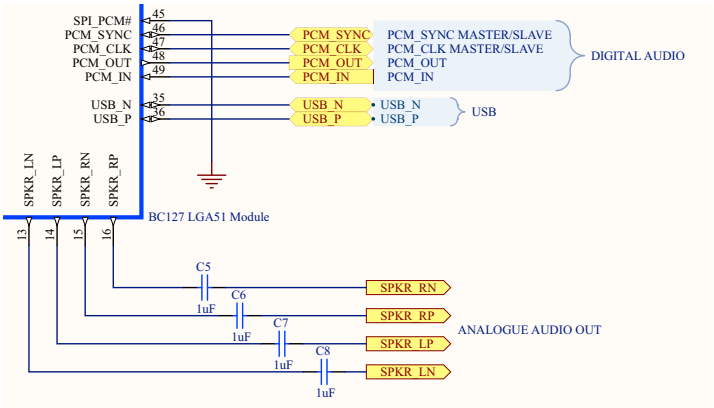

Figure 4-9: External Series Capacitance Required for Speaker Output Connects

4.5 Audio Codec

The audio interface circuit consists of:

- Stereo/dual-mono audio codec
- Dual analog audio inputs
- Dual analog audio outputs
- 2 configurable PCM/I²S interfaces
- SPDIF interface

Figure 4-10 shows the functional blocks of the interface:

- The codec supports stereo/dual-mono playback and recording of audio signals at multiple sample rates with a 24-bit resolution. The ADC and the DAC of the codec each contain 2 independent high-quality channels. Any ADC or DAC channel runs at its own independent sample rate.
- PCM interface shares the same pins as I²S interface but the audio buses are mutually exclusive in their usage.
- SPDIF interface is supported on PCM_IN and PCM_OUT pins.

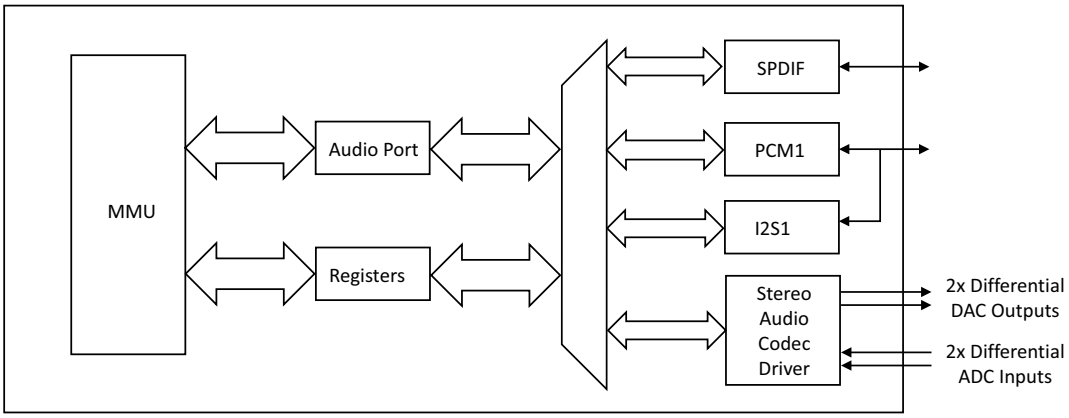

Figure 4-10: Figure 21: Audio Block Diagram

4.5.1 PCM/I²S

The AirPrime BC127 provides I²S (Inter-IC Sound) and PCM Digital Audio protocols on the same hardware interface. Features include:

- Master & Slave mode
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data
- Bidirectional digital audio interface that routes directly into the baseband layer of the firmware, without passing through the HCI protocol layer.
- Hardware for sending data to and from a SCO connection.
- Up to 3 simultaneous SCO connections on the PCM interface.
- Various clock formats including:
  - Long Frame Sync
  - Short Frame Sync
  - GCI timing environments
- 24-bit / 16-bit / 13-bit linear, 8-bit μ-law or A-law companded sample formats.
- PCM Interface Master, generates PCM_CLK and PCM_SYNC:
  - PCM_CLK—128/256/512/1536/2400 kHz
  - PCM_SYNC—8/16/32/48 kHz
- PCM Interface Slave, accepts externally generated PCM_CLK and PCM_SYNC:
  - PCM_CLK—Up to 2400 kHz
  - PCM_SYNC—8/16/32/48 kHz
- PCM Interface receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC
- PCM Interface multiplexed with debug SPI interface.
- I²S Interface:Supports left-justified or right-justified.

Important: *If the PCM interface is not used, it is strongly recommended to bring out the PCM I/O to test points.*

Pin 45 is used to place the PCM/SPI interface in PCM/I2S/SPDIF or SPI mode.

The AT configuration command **AUDIO_DIGITAL** is used to configure the Digital Audio interface parameters.

Table 4-3: PCM/I²S Interface

Pin #	Name	Description	I/O	Details
45	SPI/PCM#	SPI or PCM/I²S/SPDIF selector. Defaults to Low for PCM/I²S/SPDIF. Drive high for SPI.	Input	Supply Domain VDD_PADS
46	PCM_SYNC	PCM Sync (Master=Output, Slave=Input)	I/O	
	I2S_WS	I2S1 Word Select, (Master=Output, Slave=Input)	I/O	
47	PCM_CLK	PCM Clock (Master=Output, Slave=Input)	I/O	
	I2S_SCK	I2S1 Serial Clock (Master=Output, Slave=Input)	I/O	
48	PCM_OUT	PCM Data Output	Output	
	I2S_SD_OUT	I2S1 Serial Data Output	Output	
49	PCM1_IN	PCM Data Input	Input	
	I2S_SD_IN	I2S1 Serial Data Input	Input	

4.5.2 SPDIF

The AirPrime BC127 supports IEC-60958 standard stereo digital audio bus standards (SPDIF, AES3 (also known as AES/EBU)).

Table 4-4: SPDIF Interface

Pin #	Name	Description	I/O	Details
48	SPDIF_TX	SPDI Data Output	Output	Supply Domain VDD_PADS
49	SPDIF_RX	SPDI Data Input	Input	Supply Domain VDD_PADS

4.6 Debug SPI Slave

The AirPrime BC127 provides an SPI Slave interface for programming and debugging.

Important: *It is strongly recommended to bring out the SPI I/O and control (SPI_CS#, SPI_CLK) pins to test points on the customer application.*

Table 4-5: SPI Interface

Pin #	Name	Description	I/O	Details
45	SPI/PCM#	SPI or PCM selector. Defaults to Low for PCM/I^{2}S/SPDIF. Drive high for SPI.	Input	Supply Domain VDD_PADS
46	SPI_CS#	SPI Chip Select	Input	
47	SPI_CLK	SPI Clock	Input	
48	SPI_MISO	SPI Master Input Slave Output	Output	
49	SPI_MOSI	SPI Master Output Slave Input	Input	

4.7 Analog Voltage Measurement

The AirPrime BC127 provides one AIO (Analog Input/Output) that can be configured for analog voltage measurement or for analog voltage output signals. Auxiliary functions available on the analog interface include a 10-bit ADC and a 10-bit DAC.

When configured for analog signals, the voltage range is constrained by the analog supply voltage (1.8 V typical). When configured to drive out digital level signals generated from within the analog part of the device, the output voltage level is determined by VDD_AUX (1.35 V typical).

Table 4-6: Analog Voltage I/O

Pin #	Name	Description	I/O	Details
12	AIO_1	Analog Voltage measurement input	I/O	Supply Domain VDD_AUX (1.35 V)

4.8 I^{2}C Interface

The AirPrime BC127 provides an I^{2}C-compatible interface operating at 100 kHz and 400 kHz. This interface is used only for connection to MFi authentication co-processor revision C with Melody firmware that supports Apple™ MFi authentication.

Table 4-7: I^{2}C Interface

Pin #	Name	Description	I/O	Details
5	I2C_SCL	I^{2}C Clock	Output	Supply Domain VDD_PADS
6	I2C_SDA	I^{2}C Data	I/O	

4.9 GPIOs

The AirPrime BC127 provides multiple GPIO pins for customer use, which can be turned on or off via the AT command **PIO**.

Table 4-8: GPIO Interface

Pin #	Name	Description	I/O	Details
23	PIO_0	General Purpose IO	I/O	Supply Domain VDD_PADS
24	PIO_1	General Purpose IO	I/O	
50	PIO_2	General Purpose IO	I/O	
51	PIO_3	General Purpose IO	I/O	
26	PIO_4	General Purpose IO	I/O	
25	PIO_5	General Purpose IO	I/O	

4.10 LED

The AirPrime BC127 provides 3 open-drain LED driver pins and includes functionality for RGB with PWM flasher on sleep clock. The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

Table 4-9: LEDs

Pin #	Name	Description	I/O	Details
37	LED_0	Open drain 4.3 V tolerant	Output	LED outputs drivers for user-defined use.
38	LED_1	Open drain 4.3 V tolerant	Output	
39	LED_2	Open drain 4.3 V tolerant	Output	

5: General Layout Recommendations

In addition to specific requirements for the antenna implementation and clearance of the BC127 detailed in this document, good mixed-signal layout practices should be followed:

- Avoid tracking of high frequency signals near the RF sections of the module.
- Ensure plenty of ground vias throughout the application board.
- Tightly tie ground planes together throughout the application board.
- BC127-EXT RF tracking to application board antenna or RF connector:
  - Use 50 Ω impedance controlled tracks.
  - Do not track near sources of digital interference.
  - Provide continuous unbroken ground plane reference.
  - Avoid multiple layer changes.
- Supply decoupling should be placed as close to the supply pins as possible.
- Avoid long digital tracks on surface layers-they may support significant RF harmonic content.

6: Firmware Upgrade

The AirPrime BC127 supports firmware upgrade over the UART interface.

Sierra Wireless provides firmware files and the Melody Device Firmware Upgrade Tool on the BC127 device page at source.sierrawireless.com.

Sierra Wireless recommends upgrading to the latest version to benefit from new features and bug fixes.

7: Regulatory Compliance

Caution: *Unauthorized modifications or changes not expressly approved by Sierra Wireless could void compliance with regulatory rules, and thereby your authority to use this equipment.*

The BC127/BC127-HD/BC127-EXT/BC127-HD-EXT module is designed to meet, and upon commercial release, will meet the requirements of the following regulatory bodies and regulations, where applicable:

- Federal Communications Commission (FCC) of the United States
- The Certification and Engineering Bureau of Industry Canada (IC)
- Ministry of Internal Affairs and Communications (MIC) of Japan
- Radio Equipment and Telecommunications Terminal Equipment (R&TTE) Directive of the European Union
- The National Telecommunications Agency (ANATEL)

Upon commercial release, the following industry certification will have been obtained, where applicable:

- Bluetooth SIG

Additional certifications and details on specific country approvals may be obtained upon customer request — contact your Sierra Wireless account representative for details.

Additional testing and certification may be required for the end product with an embedded BC127/BC127-HD/BC127-EXT/BC127-HD-EXT module and are the responsibility of the OEM. Sierra Wireless offers professional services-based assistance to OEMs with the testing and certification process, if required.

7.1 United States - FCC

The BC127/BC127-HD/BC127-EXT/BC127-HD-EXT module, upon commercial release, will have been granted modular approval by the FCC. Integrators may use the BC127/BC127-HD/BC127-EXT/BC127-HD-EXT module in their end products without additional FCC certification if the following conditions are met.

- At least 20 cm separation distance between the antenna and the user's body must be maintained at all times.
- The BC127/BC127-HD/BC127-EXT/BC127-HD-EXT module must not be collocated with any other transmitter within a host device.
- The regulatory label on the end product must include the text "Contains FCC ID: SSSBC127-X" and the following compliance statement:

  This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

A user manual with the end product must clearly indicate the operating requirements and conditions to ensure compliance with current FCC RF exposure guidelines.

The end product with an embedded BC127/BC127-HD/BC127-EXT/BC127-HD-EXT module may also need to meet the FCC Part 15 unintentional emission requirements and be properly authorized per FCC Part 15 Subpart B.

7.2 Canada IC

The BC127/BC127-HD/BC127-EXT/BC127-HD-EXT module, upon commercial release, will have been granted modular approval by IC. Integrators may use the BC127/BC127-HD/BC127-EXT/BC127-HD-EXT module in their end products without additional IC certification if the following conditions are met.

- At least 20 cm separation distance between the antenna and the user's body must be maintained at all times.
- The BC127/BC127-HD/BC127-EXT/BC127-HD-EXT module must not be collocated with any other transmitter within a host device.
- The regulatory label on the end product must include the text "Contains IC : 11012A-BC127" and the following compliance statement:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

7.3 Bluetooth Qualification Program (BQP)

In case no other non-certified Bluetooth components are incorporated, the BC127/BC127-HD/BC127-EXT/BC127-HD-EXT BQP marking certification allows users to integrate the module into products without the need to obtain subsequent and separate approval.

The BC127 module family are fully approved by the Bluetooth Qualification Body (BQB) to use the Bluetooth trademark and to offer official Bluetooth functionality. The approval according to the V5.0 Bluetooth specification confirms that the module complies with the Bluetooth specification and will successfully operate with other products supporting the same profiles. This certification applies globally.

Table 7-1: BT SiG QDID

QDID	Version	Description	Melody F/W Revisions	H/W Revisions
112978	BT 5.0	Component (Tested)	7.x	• BC127 V2, V3, V4 • BC127-EXT V1 • BC127-HD V2, V3, V4
73171	BT 4.2	Host Subsystem	5.x, 6.x	• BC127 V2, V3, V4 • BC127-EXT V1 • BC127-HD V2, V3, V4
45529	BT 4.0	Controller Subsystem	4.x, 5.x, 6.x	• BC127 V2, V3 • BC128 V1, V2 *Note: BC128 model number has changed to BC127-EXT.*

7.4 Labeling

Products complying with all relevant requirements are allowed to bear the official Bluetooth logo.

For further information regarding the BQP certification requirements please review the following website:

- Bluetooth Special Interest Group—https://www.bluetooth.org/apps/content/

Note: To determine whether specific approvals have been received or to obtain the anticipated schedule for approvals, please contact your Sierra Wireless account representative.

8: Pin Out

The system interface of the AirPrime BC127 is through the LGA pattern on the bottom of the PCB.

Pins marked as "Leave open" or "Reserved" should not be used or connected.

Table 8-1: Module Pinout

Pin	Signal Name	Group	I/O[a]	Voltage	Pull Up/ Down[b]	Active[c]	Function
1	GND	Ground	0V	0V	-	-	Ground
2	GND	Ground	0V	0V	-	-	Ground
3	GND	Ground	0V	0V	-	-	Ground
4	GND	Ground	0V	0V	-	-	Ground
5	PIO_6	GPIO	I/O	VDD_PADS	NP	H	General Purpose IO
	I2C_SCL	I2C	O	VDD_PADS	NP	H	I^2C clock. External 2.2 kΩ pull-up required
6	PIO_7	GPIO	I/O	VDD_PADS	NP	H	General Purpose IO
	I2C_SDA	I2C	I/O	VDD_PADS	NP	H	I^2C data. External 2.2 kΩ pull-up required
7	No Connect	NA	NA		NP		Reserved leave open circuit
8	No Connect	NA	NA		NP		Reserved leave open circuit
9	No Connect	NA	NA		NP		Reserved leave open circuit
10	No Connect	NA	NA		NP		Reserved leave open circuit
11	GND	Ground	0V	0V	-	-	Ground
12	AIO_1	Analog	I/O	VDD_PADS	NP	H	Analog I/O, voltage sense/voltage drive
13	SPKR_LN	Augido	O		NP	H	Speaker Output Left Negative
14	SPKR_LP	Audio	O		NP	H	Speaker Output Left Positive
15	SPKR_RN	Audio	O		NP	H	Speaker Output Right Negative
16	SPKR_RP	Audio	O		NP	H	Speaker Output Right Positive
17	MIC_BIAS_A	Audio	O		NP	H	Microphone Bias
18	MIC_RN	Audio	I		NP	H	Microphone Input Right Negative
19	MIC_RP	Audio	I		NP	H	Microphone Input Right Positive
20	MIC_LN	Audio	I		NP	H	Microphone Input Left Negative
21	MIC_LP	Audio	I		NP	H	Microphone Input Left Positive
22	GND	Ground	0V	0V	-	-	Ground
23	PIO_0	GPIO	I/O	VDD_PADS	NP	H	General Purpose I/O

Table 8-1: Module Pinout (Continued)

Pin	Signal Name	Group	I/O[a]	Voltage	Pull Up/ Down[b]	Active[c]	Function
24	PIO_1	GPIO	I/O	VDD_PADS	NP	H	General Purpose I/O
25	PIO_5	GPIO	I/O	VDD_PADS	NP	H	General Purpose I/O
26	PIO_4	GPIO	I/O	VDD_PADS	NP	H	General Purpose I/O
27	GND	Ground	0V	0V	-	-	Ground
28	VREGEN	Enable	I	VBAT	PL	H	Device Enable
29	CHG_EXT	Power	O	VBAT	NP	-	External Battery Bypass Transistor Control
30	VCHG	Power	I		NP	H	Internal Charger Input Voltage
31	VBAT_SENSE	Power	I	VBAT	NP	H	Battery Sense Voltage for Charger Circuit
32	VBAT	Power	I	VBAT	NP	H	External Battery Condition
33	VDD_PADS	Power	I	VDD_PADS	NP	H	GPIO and Interfaces Reference Voltage
34	3V3_USB	Power	O	3V3_USB	NP	H	3.3V Output Voltage for external circuitry (USB only)
35	USB_N	USB	I/O	3V3_USB	NP	H	USB Differential Negative I/O
36	USB_P	USB	I/O	3V3_USB	NP	H	USB Differential Positive I/O
37	LED_0	LED	I	VDD_PADS	OD	L	Open Drain LED Driver
38	LED_1	LED	I	VDD_PADS	OD	L	Open Drain LED Driver
39	LED_2	LED	I	VDD_PADS	OD	L	Open Drain LED Driver
40	UART_CTS	UART	I	VDD_PADS	PU	L	UART Clear To Send
41	UART_TX	UART	O	VDD_PADS	PU	L	UART Transmit
42	UART_RX	UART	I	VDD_PADS	PU	L	UART Receive
43	UART_RTS	UART	O	VDD_PADS	PU	L	UART Request To Send
44	RST#	Enable	I	VDD_PADS	PU	L	Reset, drive low for 5 ms
45	SPI_PCM#	Enable	I	VDD_PADS	PL	-	PCM or SPI select. Drive High to enable SPI Debug Interface.
46	PCM_SYNC	Audio	I/O[d]	VDD_PADS	NP	H	Synchronous Audio Data Sync
	SPI_CS#	SPI	O	VDD_PADS	PU	L	Debug SPI Chip Select
	I2S_WS	I2S	I/O[d]	VDD_PADS	NP	H	I^2S Word Select
47	PCM_CLK	Audio	I/O[d]	VDD_PADS	NP	H	Synchronous Audio Data Sync
	SPI_CLK	SPI	O	VDD_PADS	PU	L	Debug SPI Clock
	I2S_CLK	I2S	I/O[d]	VDD_PADS	NP	H	I^2S Clock

Table 8-1: Module Pinout (Continued)

Pin	Signal Name	Group	I/O[a]	Voltage	Pull Up/ Down[b]	Active[c]	Function
48	PCM_OUT	Audio	O[d]	VDD_PADS	NP	H	Synchronous Audio Data Output
	SPI_MISO	SPI	O	VDD_PADS	PU	L	Debug SPI Master Input Slave Output
	I2S_SD_OUT	I2S	I/O[d]	VDD_PADS	NP	H	I^2S Data Out
	SPDIF_TX	TPDIF	O	VDD_PADS	NP	H	SPDIF Data Out
49	PCM_IN	Audio	I[d]	VDD_PADS	NP	H	Synchronous Audio Data Input
	SPI_MOSI	SPI	I	VDD_PADS	PU	L	Debug SPI Master Output Slave Input
	I2S_SD_IN	I2S	I	VDD_PADS	NP	H	I^2S Data In
	SPDIF_RX	SPDIF	I	VDD_PADS	NP	H	SPDIF Data In
50	PIO_2	GPIO	I/O	VDD_PADS	NP	H	General Purpose I/O
51	PIO_3	GPIO	I/O	VDD_PADS	NP	H	General Purpose I/O
52	GND	Ground	0V	0V	-	-	Ground (BC127-EXT Only)
53	BT RF	RF	I/O	N/A	NP	H	RF I/O (BC127-EXT Only)
54	GND	Ground	0V	0V	-	-	Ground (BC127-EXT Only)

a. Signal direction with respect to the module.
b. NP—No Pull; PD—Pull Down; PU—Pull Up; PUE—Pull Up External
c. H—High; L—Low; SW—Software defined
d. Depends on Master/Slave configuration

A: List of Abbreviations

Table 1-1: Abbreviations

Abbreviation	Definition
ADC	Analog to Digital Converter
AIO	Analog Input/Output
AUX	AUXiliary
CLK	CLocK
CPU	Central Processing Unit
CTS	Clear To Send
DAC	Digital to Analog Converter
DC	Direct Current
DCE	Data Communication Equipment
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
ESD	ElectroStatic Discharges
GND	GrouND
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
IIC (I^2C)	Inter IC Control bus
I/O	Input/Output
MFi	Made for iPhone/iPod/iPad (Apple licensing program)
MIC	MICrophone
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PWM	Pulse Width Modulation
RF	Radio Frequency
RI	Ring Indicator
RTC	Real Time Clock

Table 1-1: Abbreviations (Continued)

Abbreviation	Definition
RTS	Request To Send
RXD	Receive Data
SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface
SPK	SPeaKer
TP	Test Point
TXD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
VM	Virtual Machine