XR809 Datasheet

A Single-Chip Wi-Fi and Internet-of-Things solution for MCU Applications

Revision 1.1

Nov 22, 2018

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Revision History

Version	Data	Summary of Changes
1.0	2017-10-20	Initial Version
1.1	2018-10-22	Update power domain description

Table 1-1 Revision History

Contents

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1 Overview

1.1 General Description

XR809 is a highly integrated low-power WLAN Microcontroller System-on-Chip (SOC) solution designed for Internet of Things (IoT), Wearable equipment, Machine-to-Machine (M2M), Home automation, Cloud Connectivity and Smart Energy applications.

The XR809 application subsystem is powered by an ARM Cortex-M4F CPU that operates up to 160MHz. It supports an integrated 384KB SRAM and 2MB Flash ROM. It also includes many peripherals, including UART, TWI, SPI, PWM, IrDA (T/R), SDIO and auxiliary ADC.

The WLAN subsystem contains the 802.11b/g/n radio, baseband and MAC that designed to meet both the low power and high throughput network application.

The SoC is designed for networked low-power embedded applications. It has an integrated network processor with a large set of TCP/IP with IPv4/IPv6 based services. These services can be accessed via a serial UART/SPI link connected to an external host CPU.

1.2 Features

- Package
  - 6 x 6mm 52-pin QFN package

- Power Management and Clock Source
  - Integrate high efficiency power management unit with single 2.7-5.5V power supply input.
  - Integrated DC-DC and LDOs for internal power supply
  - Separate power switches for CPU, RAM and peripherals
  - 24MHz source crystal clock support
  - 32KHz RC clock support

- Application Microcontroller Subsystem
  - ARM Cortex-M4F, up to 160MHz
  - Embedded 384KB SRAM and 2MB Flash ROM
  - Supports Secure Boot
  - Hardware Crypto Engine for Advanced Security, Including AES, DES/3DES, SHA2/MD5, CRC
  - 4-channels General Direct Memory Access(DMA) channels
  - 2 Universal Asynchronous Receivers and Transmitters (UART)
  - 2 Serial Peripheral Interfaces
  - 2 General Timers, 2 alarm Timers, 1 RTC and 1 watch dog
  - 4 PWM and Event Capture Controllers

- 3 channels 12-bit accuracy ADC
- 1 Two Wire Interface Controllers for sensors control
- 1 IR receiver and 1 IR transmitter

- WLAN Subsystem

- 802.11b/g/n Radio, Baseband, Medium Access Control(MAC)
- Embedded TCP/IP Stack
- Station, AP Modes
- SmartConfig Technology for Autonomous and Fast WIFI Connections
- Security support for WEP, WPA/WPA2 personal, WPS2.0
- Industry-Standard BSD Socket Application Programming Interfaces (APIs)

- Miscellaneous
- Integrates 2Kbit eFuse to store device specific information and RF calibration data

1.3 Application

- Home Automation
- Home Appliances
- Access Control
- Smart Energy
- Cloud Connectivity
- Industrial Control
- Wearable Equipment
- IP Network Sensor Nodes

1.4 Block Diagram

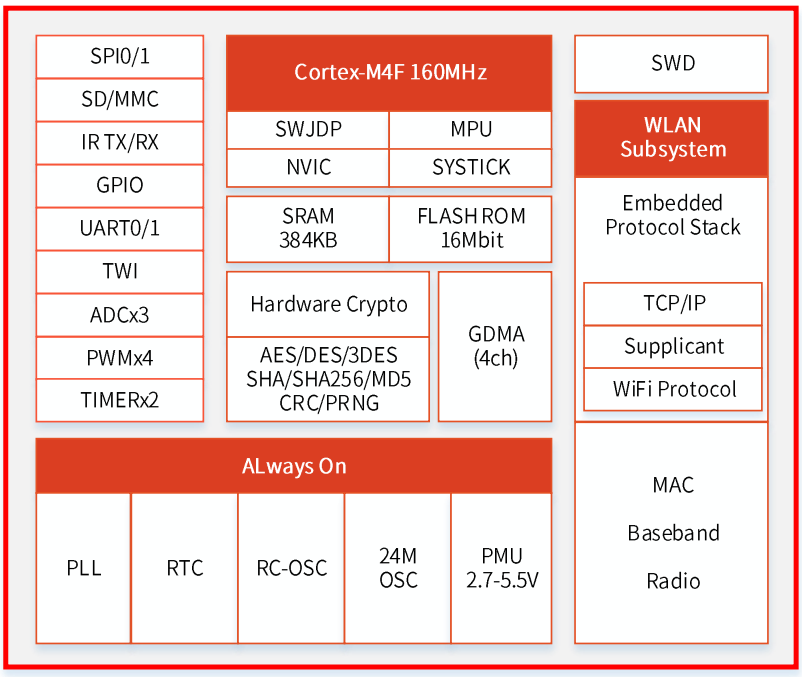


Figure 1-1 XR809 Functional Block Diagram

2 Function Description

2.1 System Overview

2.1.1 Power Management

A single 2.7 – 5.5V power supply is required for the XR809. It could be from an AC-DC converter to convert the AC voltage supply to 5V or a DC-DC converter to convert higher voltage supply to 3.3V. It could be from a battery directly too.

The Power Management Unit (PMU) contains a DC-DC, several Low Drop-out Regulators (LDOs), a highly efficient buck converter and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, efficient line/load regulation, high ripple rejection, and low output noise.

The PMU integrates several LDOs for different circuits: DLDO stands for digital core LDO and the ALDO stands for Analog and RF system LDO. PLDO stands for clock generate system LDO and RLDO stands for the RTC and SLEEP system LDO. In Deep-Sleep mode, the DLDO, PLDO, RLDO can be shut down and only the RLDO is working.

There are four power domains in the system: RTC domain, SRAM domain, Digital Core domain and WIFI domain.

2.1.2 Clock

The clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based up a module's individual requirements. The system depends on, and generates two different clocks: a high frequency clock *HFCLK* and a low frequency clock *LFCLK.*

The system integrates an internal 32.768 KHz RC oscillator. This clock is used for each subsystem to achieve lower current consumption for different running mode.

There is one clock source for HFCLK, the 24MHz crystal oscillator. The HFCLK is enabled automatically when the system is powered up and can be switched off when all subsystems won't use it anymore in some low power modes.

The HFCLK is used to generate the clock source for Digital PLL, which is used to generate the clock sources for Cortex-M4 core, WLAN and peripherals.

The following figure shows the clock control block diagram.

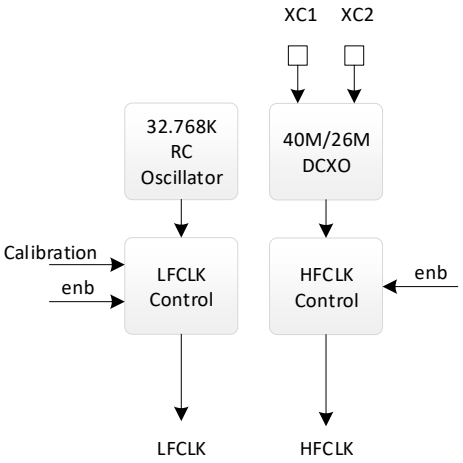


Figure 2-1 XR809 Clock Control

2.1.3 Memory Mapping

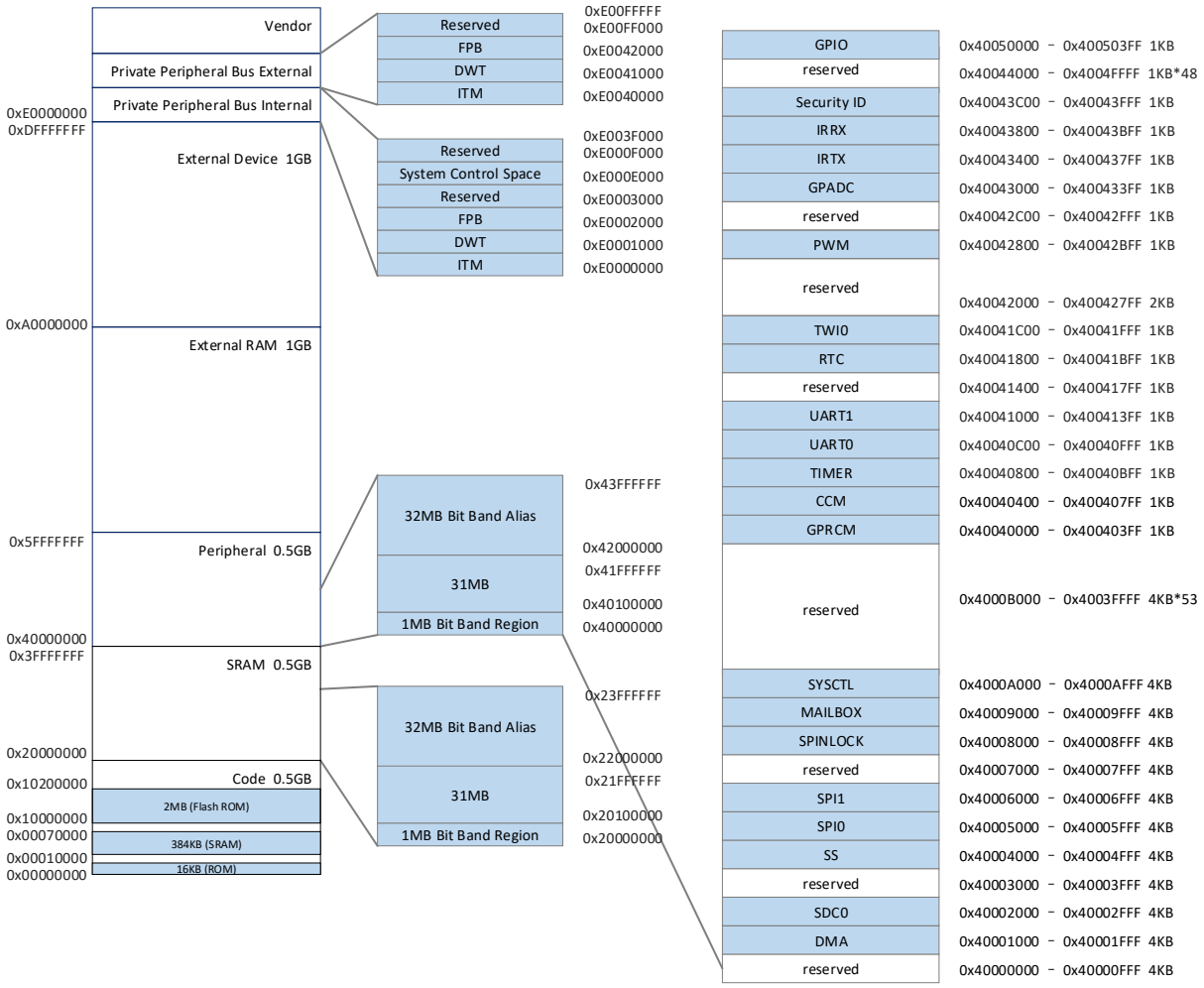


Figure 2-2 XR809 Memory Mapping

2.1.4 CPU

XR809 features an ARM Cortex-M4 processor, which is the most energy efficient ARM processor available. It supports the clock rates from 32KHz up to 160MHz. The processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption.

The ARM Cortex-M4 core has low-latency interrupt processing with the following features:

- Thump-2 instruction set for optimal performance and code size
- Handler and thread modes
- Memory Protection Unit (MPU) for memory protection features
- Floating Point Unit (FPU) to support DSP related function
- Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing
- Three Advanced High-Performance bus AHB-Lite interfaces: ICode, DCode and system bus
- Bit-band support for memory and select peripheral that include atomic bit-band write and read

operations

- Wake-up Interrupt Controller (WIC) providing ultra-low power sleep mode support

2.1.5 Crypto Engine

The Crypto Engine (CE) is one encrypt/decrypt algorithms accelerator. It is suitable for a variety of applications.

Features:

- Supports AES, DES, 3DES, SHA-1, MD5, PRNG, CRC32/16, SHA256
- Supports ECB, CBC, CTR modes for AES/DES/3DES
- Supports 128-bits, 192-bits and 256-bit key size for AES
- Supports 160-bits hardware PRNG with 192-bits seed

2.2 Peripherals

2.2.1 GPIO

The XR809 GPIO unit provides as many as 23 GPIO (General Purpose IO) pins. All ports are brought out of the device using alternate function multiplexing. The GPIO function can be multiplexed on a multi-function I/O pin by selecting the GPIO alternate function in the GPIO Controller registers.

There are two types of GPIO designs in XR809: GPIO and AGPIO. Each GPIO can be configured with the following options:

- Input / Output / Floating(Hi-Z) mode
- Input mode: Pull-up or Pull-down
- Output mode: Active driving
- Pull-up/down control: the pull-up and pull-down resistance is 90KΩ with ±30% variation over PVT condition
- External Interrupt IO with 5 trigger modes: high-level, low-level, rising edge, falling edge, double edge

The digital IO AGPIO function is equivalent to GPIO as shown above. A dedicated internal control signal is used to select between the digital and analog functions. These IOs are multiplexed with 3 channels ADC.

GPIO	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5
PA00					EINTA0
PA01					EINTA1
PA06			TWI0_SCL		EINTA6
PA07			TWI0_SDA		EINTA7
PA08	ADC_CH0				EINTA8
PA12	ADC_CH4			IR_TX	EINTA12
PA14	ADC_CH6			IR_RX	EINTA14
PA15				UART1_CTS	EINTA15
PA16	IR_TX	IR_RX		UART1_RTS	EINTA16

PA17				UART1_TX	EINTA17
PA18				UART1_RX	EINTA18
PA19			PWM0/ECT0	SPI1_MOSI	EINTA19
PA20			PWM1/ECT1	SPI1_MISO	EINTA20
PA21			PWM2/ECT2	SPI1_CLK	EINTA21
PA22			PWM3/ECT3	SPI1_CS0	EINTA22
PB00	UART0_TX				EINTB0
PB01	UART0_RX				EINTB1
PB02	SWD_TMS				EINTB2
PB03	SWD_TCK				EINTB3
PB04	SPI0_MOSI				EINTB4
PB05	SPI0_MISO				EINTB5
PB06	SPI0_CS0				EINTB6
PB07	SPI0_CLK				EINTB7

Table 2-1 GPIO Multiplexing

2.2.2 UART

The XR809 provides 2 UART controllers: one is used for debug and another with auto-flow control are used for communication with external devices. The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

Features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- Support DMA controller interface
- Support Software/ Hardware Flow Control
- Support IrDA 1.0 SIR
- Support RS-485 mode
- Support configurable Baudrate from 9600, 19200, 38400, 115200 and 921600 etc.
- Support baudrate detection

2.2.3 SPI

The XR809 features two SPI controllers. Each controller can be configured to a SPI master or a SPI slave. They are used as an extension interface to control the peripheral devices. They support two options of clock polarity (CPOL) and two options of initial clock phase (CPHA).

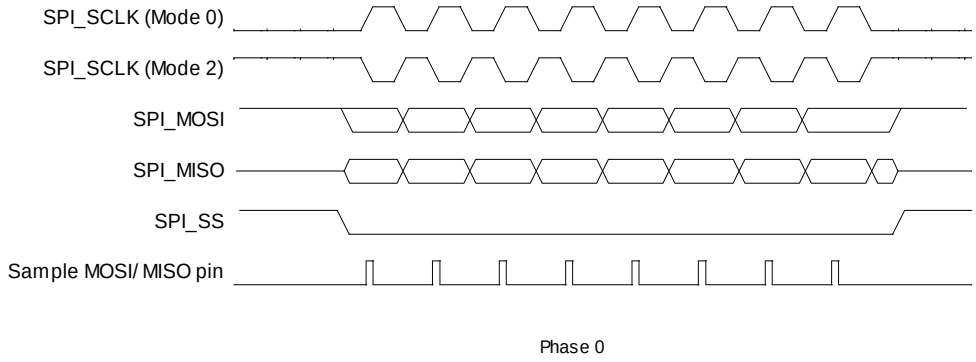


Figure 2-3 SPI Phase 0 Transfer Format

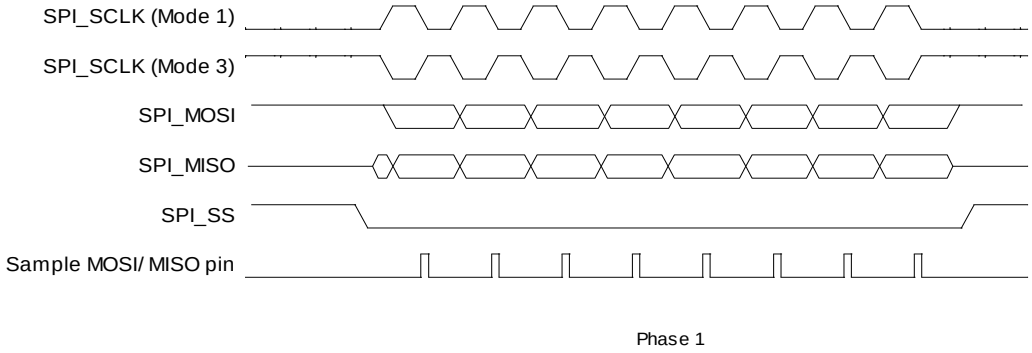


Figure 2-4 SPI Phase 1 Transfer Format

2.2.4 TWI

The XR809 features one TWI serial interface. It can be configured as master and salve mode. The TWI controllers can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

Features:

- Compatible with IIC protocol and SCCB protocol
- Software-programmable for Slave or Master
- Supports Repeated START signal
- Multi-master systems supported
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies

2.2.5 PWM

XR809 features 4 PWMs to generate pulse sequences with programmable frequency a duration for LCD, vibrators and other devices. The PWM controller provides 4 PWM channels, which are divided into two pairs of PWM pair, each is composed of three parts: a clock controller, two timer modules, a programmable dead-zone generator. The PWM channel logic can be configured as input capture function. The capturer detects the rising edge and the falling edge of the signal and calculates the high-level and the low-level duration with a 16-bit counter.

Features:

- 4 PWM channels, divided into 2 PWM pairs
- Supports pulse, period and complementary pair outputs
- Support input capture
- Programmable dead-zone generator
- Configurable output frequency, 0%-100% duty adjustable
- Supports internal DMA controller

2.2.6 IrDA

XR809 features an infrared remote transmitter and a receiver controller. Through the process control pulse waveform, the remote controller can support a variety of infrared protocol.

The IR receiver controller features:

- Full physical layer implementation
- Support IR for remote control
- 64x8 bits FIFO for data buffer

The IR transmitter controller features:

- Full physical layer implementation
- 128 bytes FIFO for data buffer
- Configurable carrier frequency
- Interrupt and DMA support

2.2.7 ADC

XR809 features one auxiliary ADC function. The ADC function contains a 4-channel analog switch, a single end input asynchronous 12-bit SAR (Successive Approximation Register) ADC. The channels 0, 4 and 6 are used to detect the voltage of the external input and the channel 8 is dedicated to detect the voltage of the VBAT.

Features:

- 12-bit Resolution and 10-bit effective SAR type A/D converter
- 4-channel multiplexer, 3 normal channel and 1 VBAT voltage detection channel
- 64 FIFO depth of data register
- Power Supply Voltage: 2.5V, Analog Input Range: 0 to 2.5V

- Maximum Sampling frequency: 1 MHz
- Support self-calibration
- Support data compare and interrupt
- Support four operation mode: Single conversion mode, Single-cycle conversion mode, Continuous conversion mode, Outbreak conversion mode

2.3 WIFI Subsystem

2.3.1 WIFI MAC

Supports MAC enhancements including:

- 802.11d - Regulatory domain operation
- 802.11e - QoS including WMM
- 802.11h - Transmit power control dynamic and frequency selection
- 802.11i - Security including WPA2 compliance
- 802.11r - Roaming

2.3.2 WIFI Baseband

Features:

- Compatible with IEEE 802.11 b/g/n standard
- MCS0-7 (BPSK, r=1/2 through 64QAM, r=5/6)
- Short Guard Interval
- Long Guard Interval

2.3.3 WIFI Radio

Features:

- Integrated 2.4GHz PA, LNA, and T/R switch
- Internal impedance matching network

2.3.4 WIFI 2.4G RF Transmitter/Receiver Specification

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range	Center channel frequency	2412		2484	MHz
RX Sensitivity (802.11b)	1Mbps DSSS		-97		dBm
	2Mbps DSSS		-94		dBm
	5.5Mbps CCK		-92		dBm

	11Mbps CCK		-89		dBm
RX Sensitivity (802.11g)	6Mbps OFDM		-93		dBm
	9Mbps OFDM		-91.5		dBm
	12Mbps OFDM		-90		dBm
	18Mbps OFDM		-87.5		dBm
	24Mbps OFDM		-84.5		dBm
	36Mbps OFDM		-81		dBm
	48Mbps OFDM		-77		dBm
	54Mbps OFDM		-75		dBm
RX Sensitivity (802.11n, 20MHz)	MCS 0		-91.5		dBm
	MCS 1		-89		dBm
	MCS 2		-86.5		dBm
	MCS 3		-84		dBm
	MCS 4		-80.5		dBm
	MCS 5		-76		dBm
	MCS 6		-74.5		dBm
	MCS 7		-72.5		dBm
TX Power/EVM	1Mbps DSSS		21.5/11%		dBm
	11Mbps CCK		21.5/11%		dBm
	6Mbps OFDM		20/-20.5		dBm
	54Mbps OFDM		18.5/-25.5		dBm
	HT20, MCS 0		18.5/-22.5		dBm
	HT20, MCS 7		17.5/-29		dBm

Table 2-2 RF Transmitter/Receiver Specification

2.3.5 Power Consumption

XR809, 25℃, VBAT=3.6V, MCU 160MHz

MCU State	WLAN State	TX/RX	Test Condition		mA	mW
Active	Active	TX	1M DSSS	19dBm	181	651.6
			11M CCK	19dBm	183	658.8
			6M OFDM	15dBm	139	500.4
			54M OFDM	15dBm	139	500.4
			HT20 MCS0	14dBm	133	478.8
			HT20 MCS7	14dBm	131	471.6
		RX	1M DSSS	-	29.7	106.92
			54M OFDM	-	29.6	106.56
	PS Mode	RX	DTIM1	-	8.446	30.4056

			DTIM3	-	8.082	29.0952
			DTIM10	-	7.9546	28.63656
	OFF	-	-	-	7.3	26.28
DEEPSLEEP	Active	TX	1M DSSS	19dBm	173.9	626.04
			11M CCK	19dBm	175.9	633.24
			6M OFDM	15dBm	131.9	474.84
			54M OFDM	15dBm	131.9	474.84
			HT20 MCS0	14dBm	125.9	453.24
			HT20 MCS7	14dBm	123.9	446.04
		RX	1M DSSS	-	22.5	81
			54M OFDM	-	22.5	81
	PS Mode	RX	DTIM1	-	0.770	2.773
			DTIM3	-	0.333	1.198
			DTIM10	-	0.18	0.648
	OFF	-	-	-	0.125	0.45
Hibernate	OFF	-	-	-	0.010	0.0360
DOWN	-	-	-	-	0.0007	0.00252

Table 2-3 Power Consumption

3 Electrical Characteristics

3.1 Absolute Maximum Rating

Symbol	Parameter	Maximum rating	Unit
I/O	In/Out current for input and output	-40 to 40	mA
VCC	2.7-5.5V Power supply	-0.3 to 5.8	V
T_{opr}	Operating Temperature	-40 to 85	℃
T_{stg}	Storage Temperature	-40 to 125	℃
VESD	HBM	±4000	V
VESD	CDM	±800	V

Table 3-1 Absolute Maximum Rating

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_{opr}	Ambient Operating Temperature	-40	-	85	℃
VCC	Power supply	2.7	3.6/5	5.5	V

Table 3-2 Recommended Operating Conditions

3.3 Digital IO Characteristics

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IL}	Input Low Voltage	VCC_IO=3.3V	-0.3	1.32	V
V_{IH}	Input High Voltage	VCC_IO=3.3V	2.06	3.6	V
V_{OL}	Output Low Voltage	|IOL| = 7.5~50 mA	-0.3	0.4	V
V_{OH}	Output High Voltage	|IOH| = 7.5~50 mA	2.9	3.3	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	40	110	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	40	110	KΩ

Table 3-3 DC Characteristics

3.4 XTAL Oscillator

Parameter	Value
Frequency	24MHz
Stability	+/-20ppm including temperature variation

Table 3-4 XTAL Oscillator Requirements

4 Package Specifications

4.1 Pin Layout

XR809 uses 6mm x 6mm QFN package of 52-pin with 0.4mm pitch.

4.1.1 XR809 Pin Layout

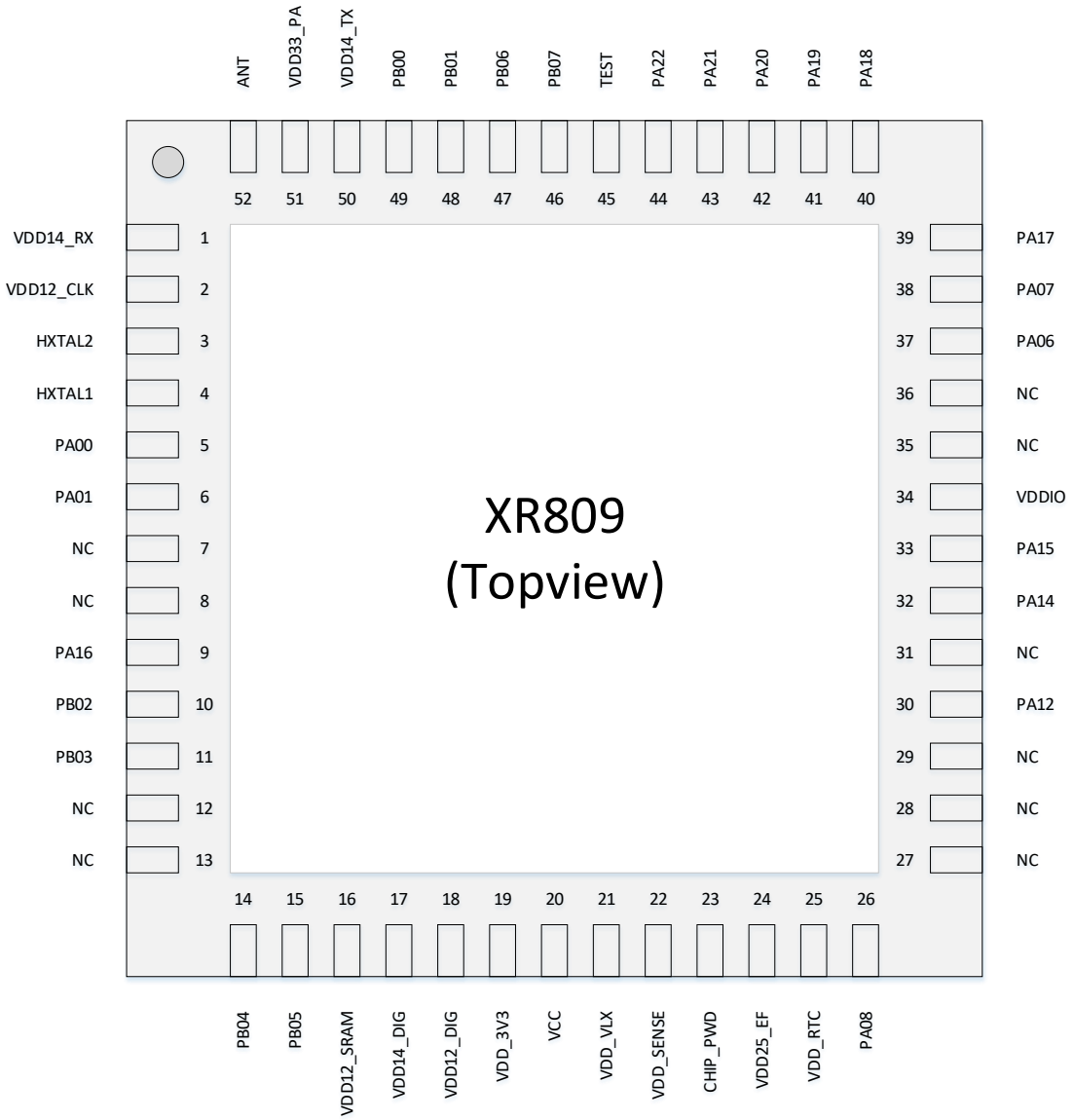


Figure 4-1 XR809 Pin Layout

4.2 Pin Description

4.2.1 XR809

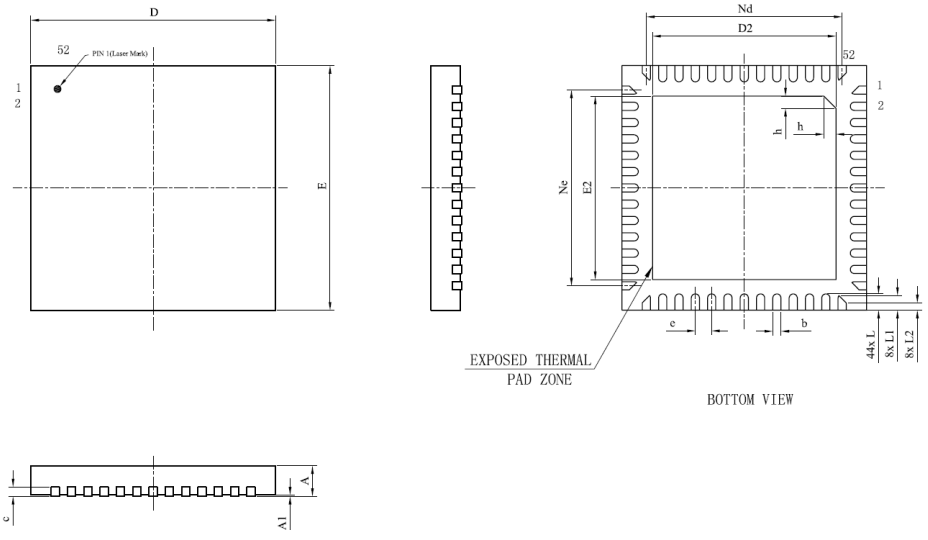
QFN NO.	Pin Name	Pin Description	I/O	Supply Domain
Power, Reset and Clocks				
25	NC			
24	NC			
4	HXTAL1	24MHz crystal	Analog	VDD_3V3
3	HXTAL2	24MHz crystal	Analog	VDD_3V3
23	CHIP_PWD/RESET	Chip Power Down/System Reset	Input	
2	VDD12_CLK	Clock 1.2V power supply	Power	
1	VDD14_RX	RF 1.4V power supply	Power	
50	VDD14_TX	RF 1.4V power supply	Power	
20	VCC	2.7-5.5V power supply	Power	
22	VDD_SENSE	BUCK power supply	Power	
21	VDD_VLX	BUCK output	Power	
17	VDD14_DIG	DLDO power supply	Power	
24	VDD25_EF	ADC and eFuse 2.5V power supply	Power	
34	VDD_IO	IO 3.3V power supply	Power	
19	VDD_3V3	3.3V power supply	Power	
16	VDD12_SRAM	SRAM 1.1V power supply	Power	
18	VDD12_DIG	Digital core 1.1V power supply	Power	
51	VDD33_PA	PA 3.3V power supply	Power	
25	VDD_RTC	RTC 1.1V power supply	Power	
Programmable I/O				
5	GPIOA0	Programmable input/output	In/Out	VDD_IO
6	GPIOA1	Programmable input/output	In/Out	VDD_IO
13	NC			
12	NC			
35	NC			
36	NC			
37	GPIOA6	Programmable input/output	In/Out	VDD_IO
38	GPIOA7	Programmable input/output	In/Out	VDD_IO
26	GPIOA8	Programmable input/output	In/Out	VDD_IO
27	NC			
28	NC			
29	NC			
30	GPIOA12	Programmable input/output	In/Out	VDD_IO
31	NC			
32	GPIOA14	Programmable input/output	In/Out	VDD_IO

33	GPIOA15	Programmable input/output	In/Out	VDD_IO
9	GPIOA16	Programmable input/output	In/Out	VDD_IO
39	GPIOA17	Programmable input/output	In/Out	VDD_IO
40	GPIOA18	Programmable input/output	In/Out	VDD_IO
41	GPIOA19	Programmable input/output	In/Out	VDD_IO
42	GPIOA20	Programmable input/output	In/Out	VDD_IO
43	GPIOA21	Programmable input/output	In/Out	VDD_IO
44	GPIOA22	Programmable input/output	In/Out	VDD_IO
49	GPIOB0	Programmable input/output	In/Out	VDD_IO
48	GPIOB1	Programmable input/output	In/Out	VDD_IO
10	GPIOB2	Programmable input/output	In/Out	VDD_IO
11	GPIOB3	Programmable input/output	In/Out	VDD_IO
14	GPIOB4	Programmable input/output	In/Out	VDD_IO
15	GPIOB5	Programmable input/output	In/Out	VDD_IO
47	GPIOB6	Programmable input/output	In/Out	VDD_IO
46	GPIOB7	Programmable input/output	In/Out	VDD_IO
WIFI Radio Interface				
52	ANT	RF Antenna	Analog	
Debug IO				
45	TEST	TEST pin	Input	

Table 4-1 XR809 Pin Description

4.3 Package Information

4.3.1 QFN52



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Figure 4-2 QFN52 Package Outline Drawing

5 Application Reference Design

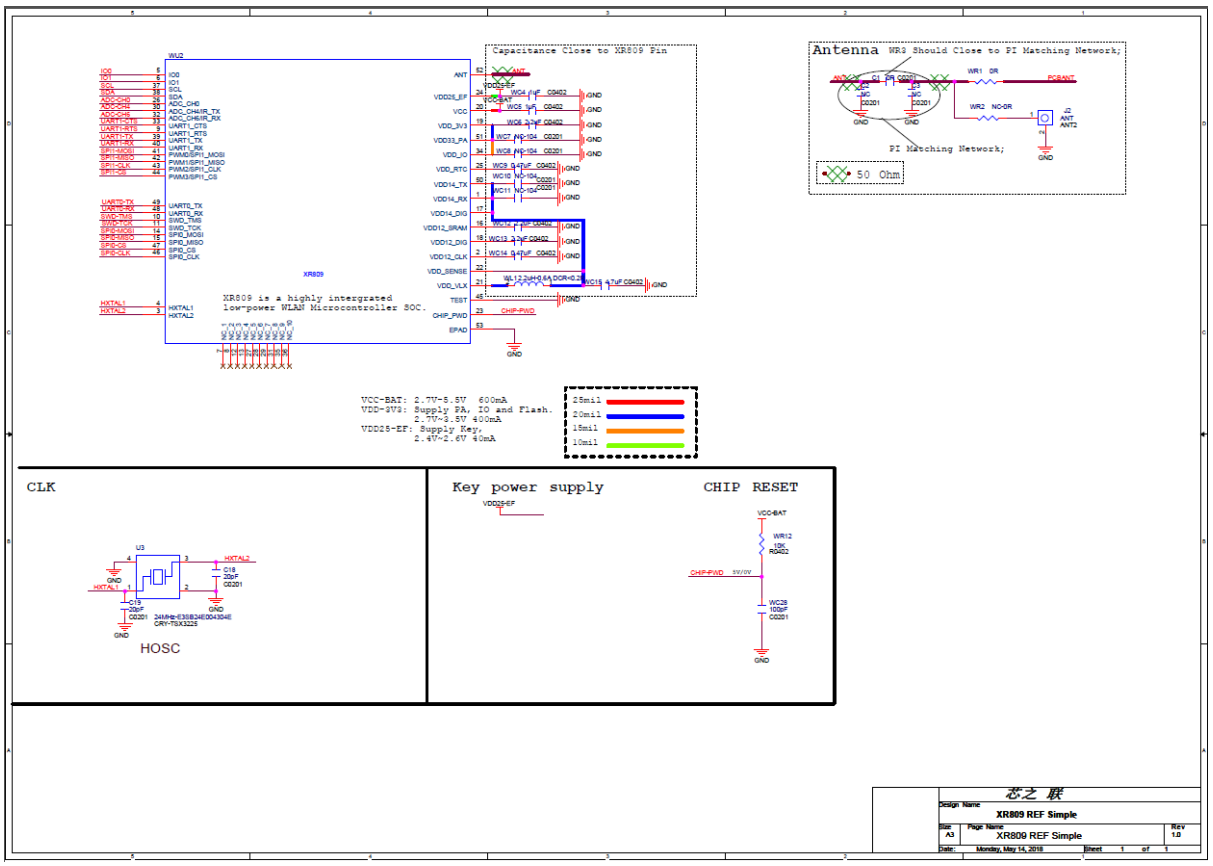


Figure 5-1 XR809 Application Reference Design

