XR872 Datasheet

High Performance Wireless MCU for Artificial Intelligence and Internet of Things (AIoT) Applications

Revision 0.1

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Revision History

Version	Data	Summary of Changes
0.1	2019-6-23	Initial Version

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1 Overview

1.1 General Description

XR872 delivers a highly integrated high performance Wi-Fi wireless System-on-Chip (SoC) solution designed for Artificial Intelligence and Internet of Things (AIOT) applications, such as smart audio, face detection and recognition, Machine-to-Machine (M2M), Smart Home, Cloud Connectivity and Smart Energy.

The XR872 application subsystem is powered by an ARM Cortex-M4F CPU that operates up to 384MHz. It supports an integrated 416KB SRAM and 160KB ROM, a QSPI interface to SIP up to 16MB Flash, a OPI interface to SIP 4MB PSRAM. Integrated I-cache enables Execute In Place (XIP) from flash and PSRAM, and integrated D-cache enables read and write from PSRAM. It also includes many peripherals, including UART, TWI, SPI, DMIC, AUDIO CODEC, PWM, CIR (T/R), CSI, SDIO and auxiliary ADC.

The Wi-Fi subsystem contains the 802.11b/g/n baseband, MAC and radio with integrated PA, LNA, Switch and harmonic filter, which is design to meet both the low power, high integration and high performance network application. A novel digital RF transmitter is design using XRADIOTECH's MPD™ technology to deliver higher output power and maintain higher efficiency, and also to keep the chip not sensitive to antenna mismatch but always have good EVM at different VSWR.

The SoC is optimized for low-power operation by using several low-power state and fast wake-up times from hardware to software. Multiple power domains and clocks can be shut down individually. The application subsystem and Wi-Fi subsystem can be put into low-power states independently, supporting a variety of application use cases. Also an optional external DC-DC regulator can provide voltage from 1.5V to 2.5V for whole VDD_ANA power domain with on chip DC-DC control signal, without sacrificing standby power consumption even using high quiescent current DC-DC.

1.2 Features

- **General System Features**

Table 1-1 XR872 Features

chip List	Description	XR872AT	XR872ET
Package	Trays and tape-in-reel	6x6mm^2	5x5mm^2
		QFN52	QFN40
Supply voltage	Power supply from system	1.8~5.5V	
PMU	LDO for external device (EXT LDO)	Yes	
External Clock	Reference High frequency clock	24/26/40	
MCU Core	Core Type	Cortex-M4F	

	Core clock maximum frequency		384MHz	240MHz
Memory	Internal ROM		160KB	
	Internal RAM		416KB	416KB
	Internal Flash		/	/
	External Flash with XIP		128Mb	
	Cache (can be configured to system ram)		40KB	40KB
	PSRAM		4MB	/
Backup register	Backup register for power save		16B	
Secure boot			Yes	
Crypto Engine	AES/DES/3DES/SHA/MD5/CRC		Yes	
TRNG	Provide random number seed		Yes	
Watchdog reset protection	Protect specified peripherals been reset by watchdog reset		Yes	
BOR	BOR Detection		Yes	
Wi-Fi	802.11 b/g/n		Yes	
Peripheral	GPIO	General Purpose	33	25
	UART		3	3
	SPI	Master and slave	2	2
	TWI	Max.400Kbps	2	2
	SDIO	Master	1	1
	GPADC	VBAT	1	1
		Normal	7	2
	DMA	8Channel	1	1
	I2S		1	0
	DMIC		1	0
	CODEC	x1 ADC	1	1
		x1 DAC	1	1

		x1 Line-in	1	0
	CSI+JPEG		1	1
	RTC		1	1
	Timer	Watchdog	1	1
		Normal	2	2
		Wakeup	1	1
	PWM	Output	8	8
		Input capture	8	8
	CIR	Receiver	1	0
		Transmitter	1	0
	32K	Internal RCOSC	1	1
		External XTAL	1	0
	WAKEUP IO	From RTC wakeup	9	9

- **Audio Subsystem**

- 1 Digital Microphone Controller with left and right channel voice input
- 1 24bit audio digital-to-analog(DAC) channel, support sample rates from 8KHz to 192KHz
- 1 24bit audio analog-to-digital(ADC) channel for microphone input, support sample rates from 8KHz to 48KHz
- 1 24bit audio-to-digital(ADC) channel for line-in, support sample rates from 8KHz to 48KHz
- DMA and interrupt support

- **Video Subsystem**

- a CMOS Sensor Interface Controller(CSIC) which is an image or video input control module to receive image or video data via digital camera(DC)interface, CCIR656 interface
- Supports JPEG base line
- Supports online encoding mode with CSI
- Supports nv12 input format in offline encoding mode
- Supports configurable picture resolutions
  - Minimum picture resolution: 32x32
  - Offline maximum picture resolution: 1920x1088

- Online maximum picture resolution: 1920x1088

- Supports online 640x480@60fps or online 1280x720@40fps
- Supports offline 640x480@30fps or offline 1280x720@20fps
- Supports bitrate control through quantization table

- **Wi-Fi Subsystem**

- IEEE 802.11b/g/n, 1x1 SISO 2.4GHz
- Integrated MAC, BB, RF and Embedded TCP/IP Stack
- Integrated T/R switch, harmonic filter, PA and LNA
- Antenna diversity
- Station, AP Modes
- Smart-Config Technology for Autonomous and Fast Wi-Fi Connections
- Security support for WEP, WPA/WPA2 personal, WPS2.0
- Industry-Standard BSD Socket Application Programming Interfaces (APIs)

- **Power Management**

- Integrate highly flexibility power management unit by several LDOs and external DC-DC controller
- Wide range power supply: 1.8-5.5V

- **Miscellaneous**

- Integrates 1Kbit eFuse to store device specific information and RF calibration data

1.3Application

- Smart Audio
- Smart Video
- Security Systems
- Smart Energy
- Internet Gateway
- Smart Home
- Access Control
- Cloud Connectivity
- Industrial Control
- IP Network Sensor Nodes

1.4Block Diagram

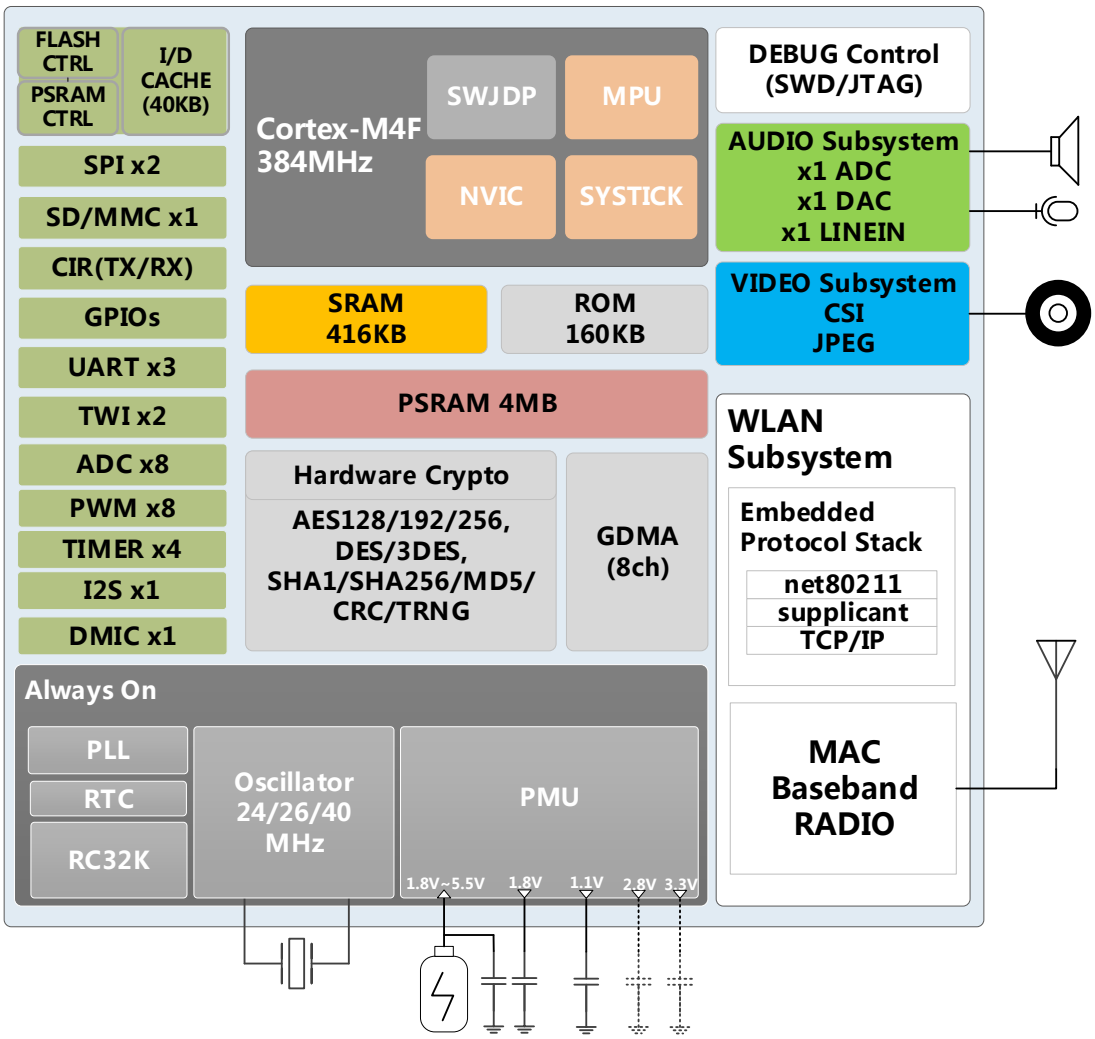


Figure 1-1 XR872 Functional Block Diagram

2 Function Description

2.1System Overview

2.1.1 Power Management

A single 1.8~5.5V power supply is required for the XR872. It could be from an AC-DC converter, USB to supply to 5V or a DC-DC converter to convert higher voltage supply to 3.3V or even lower. It could be from a battery directly too, no matter it is lithium, single 3V button or 2 serial NI-MH battery.

The Power Management Unit (PMU) contains a DC-DC control interface, several Low Drop-out Regulators (LDOs), and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, load regulation, high ripple rejection, and low output noise. The PMU integrates several LDOs for different circuits: TOP LDO, RTC LDO, SoC LDO, EXT LDO, as shown in Figure 2-1. They have different operating conditions and features:

- **TOP LDO** provide programmable voltage from 1.4V to 3.6V with maximum 350mA load current, for Analog and PSRAM, also SoC LDO input. Normally, make sure VBAT voltage is higher than this programmable output voltage setting.
- **RTC LDO** is the main supply only for RTC domain to optimize power consumption at HIBERNATION state.
- **SoC LDO** is the main supply for whole chip digital circuit with programmable voltage from 0.6V to 1.35V to let DVFS operate effectively.
- **EXT LDO** is main power supply for external device in application, and also can be provide to VDDIO, GPADC and internal CODEC. It has maximum 200mA load current. The output voltage is limited to 3.3⁄3.1V (by register configure setting), when VBAT is lower than the value, it will automatically switch to bypass mode to let output voltage follow VBAT.

When using external DC-DC to further reduce power consumption, the connection can be set as figure 2-1. PA23 GPIO pin is specified for external DC-DC pup, the detail software setting and flow is integrated in our SDK. When external DC-DC is used, the output voltage on VDD18 should be at least 0.1V step higher than TOP LDO setting voltage to have DC-DC be operating normally.

There are four power domains in the system: RTC domain, OA domain, Digital Core domain and Wi-Fi domain. They mainly used for different scenario to maintain ultra-low power application. We define XR872 into **ACTIVE, STANDBY, HIBERNATION** and **SHUTDOWN** power management states, is shown in table 2-1.

Table 2-1 Power Management States

POWER MODE	CM4F	Wi-Fi	EXT LDO	RTC LDO	TOP LDO	SoC LDO	DCXO /DPLL	Description
ACTIVE	ACTIVE	ACTIVE	ON	ON	ON	ON	ON	All CPU active

	ACTIVE	OFF	ON	ON	ON	ON	ON/OFF	APP CPU active
STANDBY	SLEEP	ACTIVE	ON	ON	ON	ON	ON	APP CPU goes to sleep, Wi-Fi DTIMx state
	SLEEP	SLEEP	ON	ON	LP	LP	OFF	
	SLEEP	OFF	ON	ON	LP	LP	OFF	APP CPU goes to sleep, Wi-Fi power off
HIBERNATE	OFF	OFF	ON/OFF	ON	OFF/LP	OFF	OFF	Only RTC on, waiting for timer or wakeup IO to interrupt
SHUTDOWN	OFF	OFF	OFF	OFF	OFF	OFF	OFF	CHIP_PWD pin keep low level

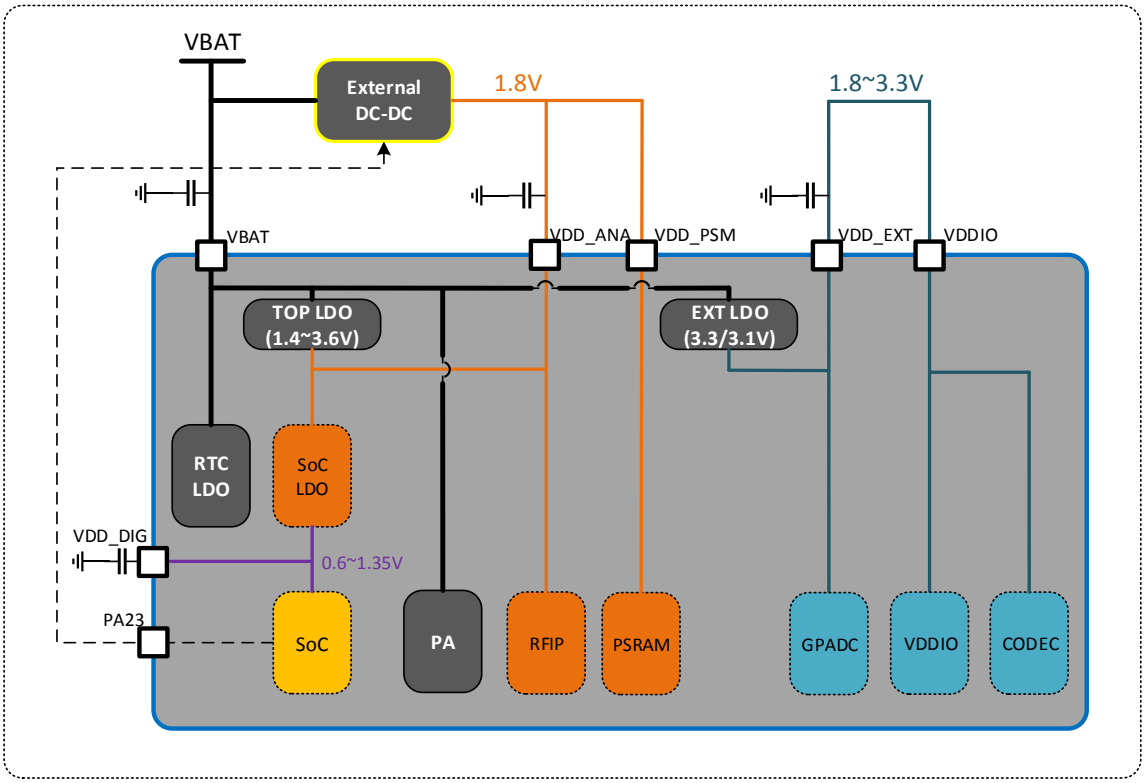


Figure 2-1 Power Architecture

2.1.2 Clock and Reset

2.1.2.1 Clock

The clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon module's individual requirements. The system generates two different clocks: a high frequency clock HFCLK and a low frequency clock LFCLK.

The system supports two LFCLK clock sources, the 32.768 KHz crystal oscillator and the 32.768 KHz RC oscillator.

The 32.768 KHz crystal oscillator requires an external AT-cut quartz crystal to be connected to the LXTAL1 and LXTAL2 pins. The LFCLK clock and all of the available LFCLK sources are switched off by default when the system is powered up. The LFCLK clock can be started by selecting the preferred clock source in PRCM register. It is used for each subsystem to achieve lower current consumption for different running mode. In addition, the LFCLK is also used in RTC circuit to achieve accuracy timing.

There is only one clock source for HFCLK, generated by the 24MHz, 26MHz, or 40MHz crystal oscillator. The HFCLK is enabled automatically when the system is powered up and can be switched off when all subsystems won't use it anymore in some low power modes.

The HFCLK is used to generate the clock source for Digital PLL, which is used to generate the clock sources for Cortex-M4F core, Wi-Fi and peripherals. There is also an Audio PLL used to generate the clock source for Audio Subsystem.

The following figure shows the clock control block diagram.

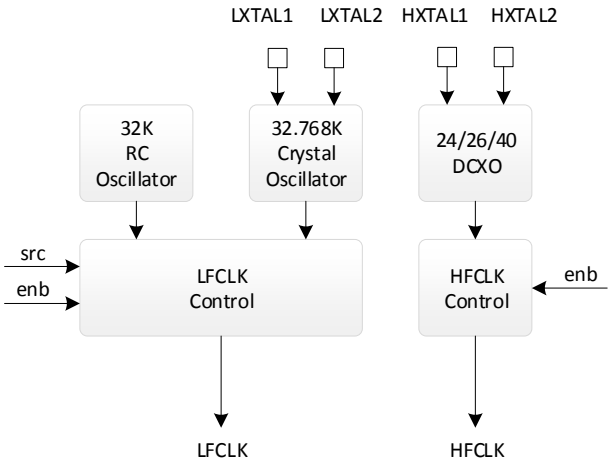


Figure 2-2 Clock Control

2.1.2.2 Reset

TBD

2.1.3 Power State and Power Sequence

2.1.3.1 Power-on Sequences

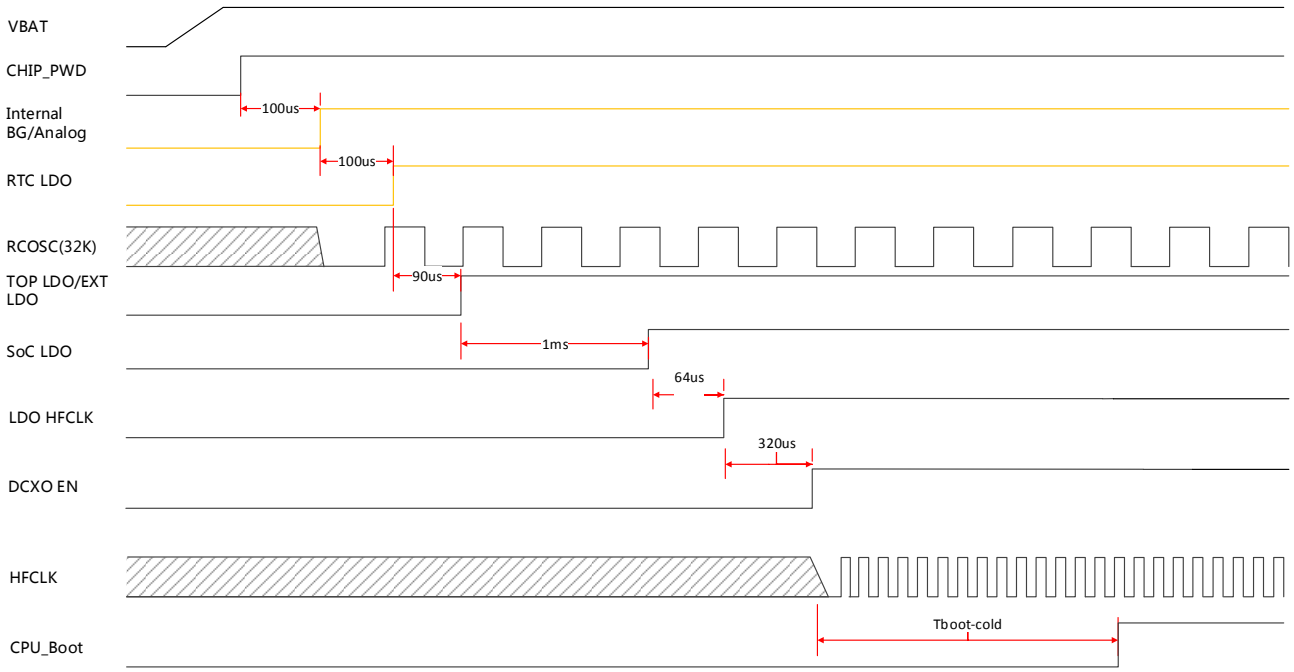
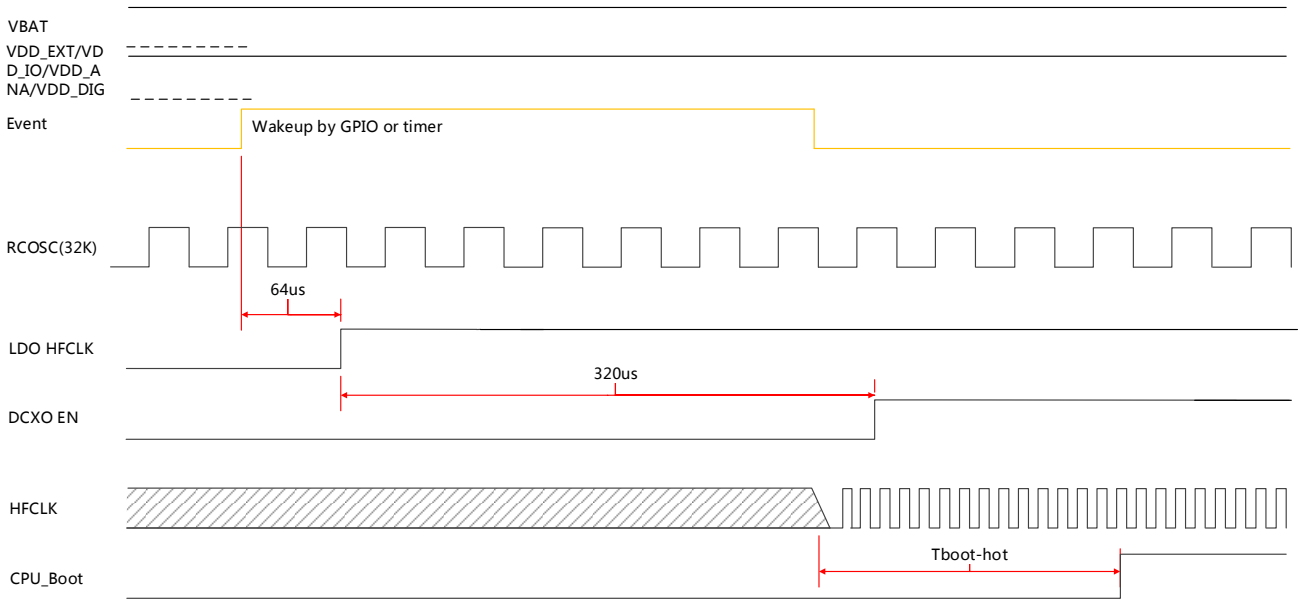
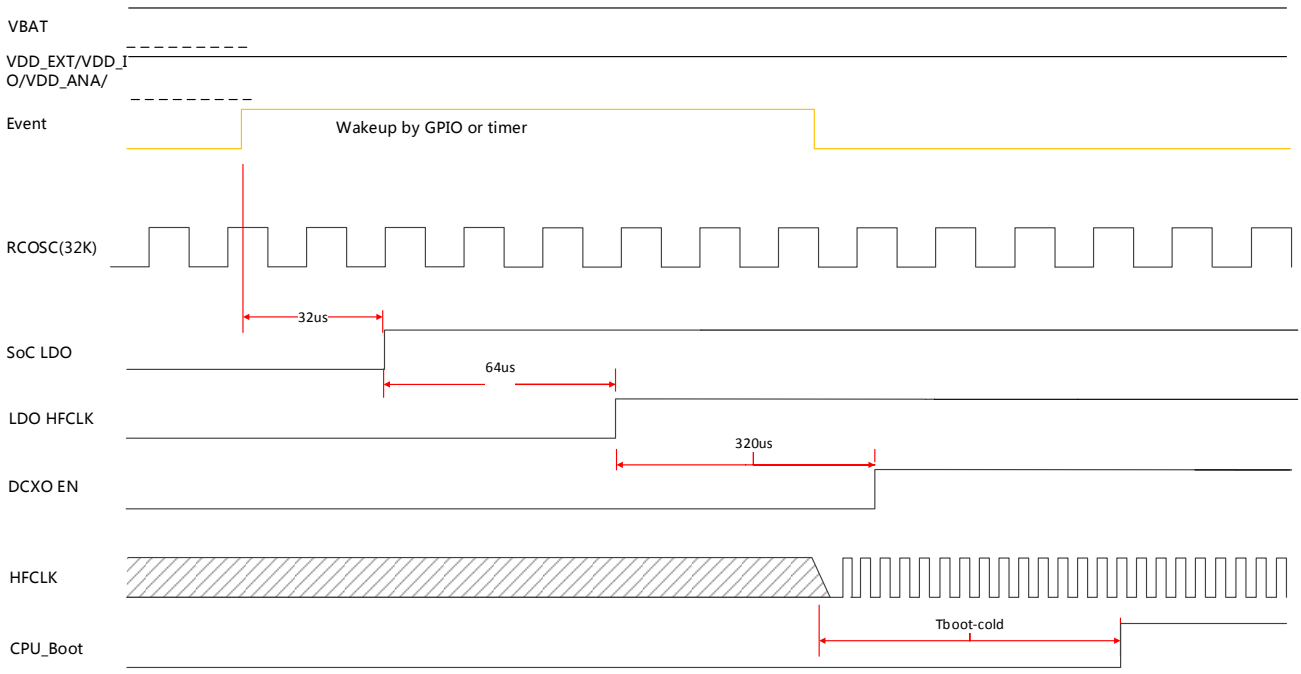


Figure 2-3 Power-on Sequence

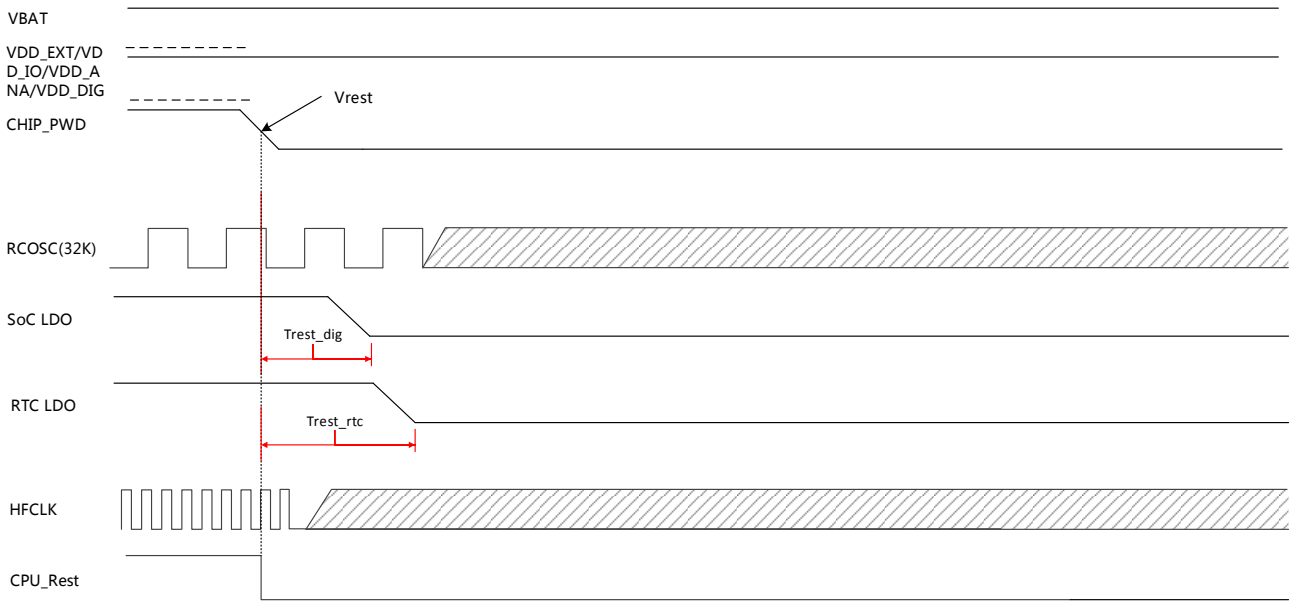
2.1.3.2 Wakeup from Standby



2.1.3.3 Wakeup from Hibernation



2.1.3.4 Shutdown Sequence



2.1.4 Memory Mapping

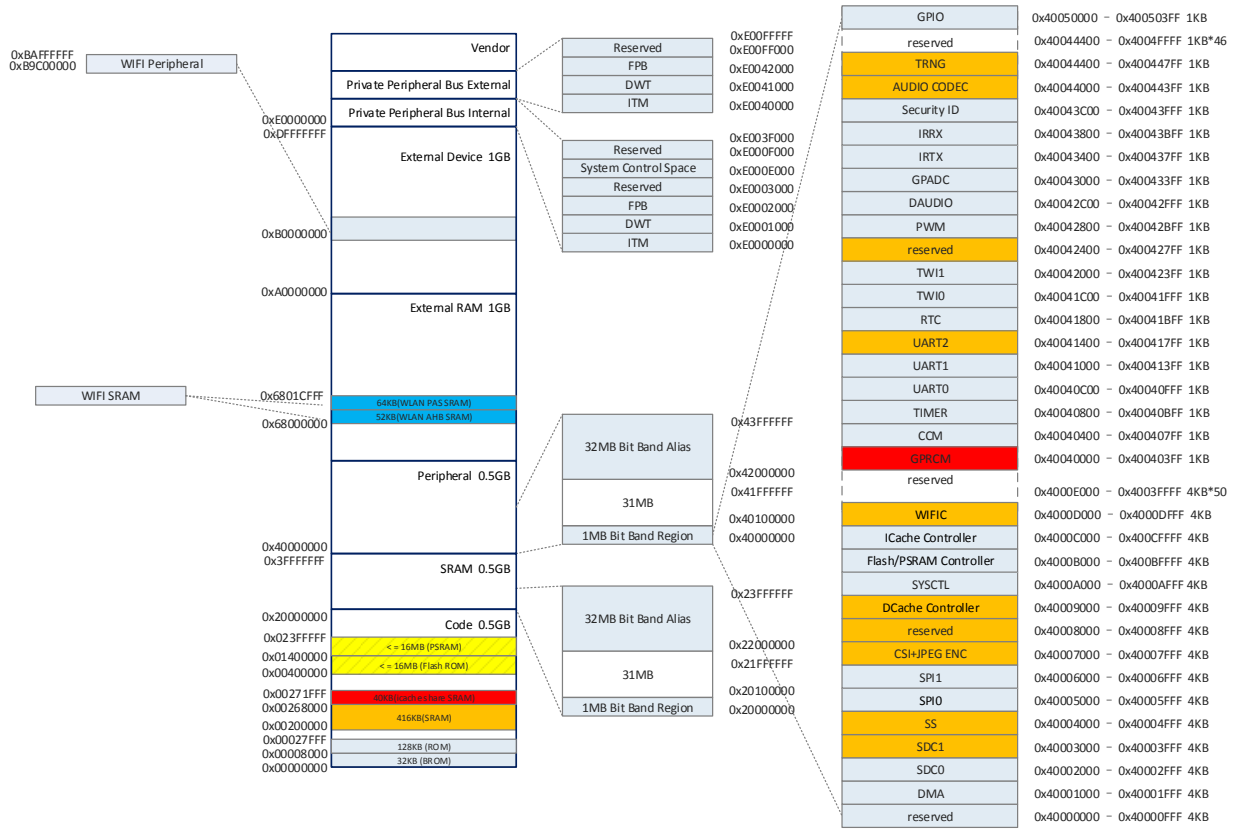


Figure 2-4 Memory Mapping

Table 2-2 SRAM Memory Mapping

RAM Region	SIZE	AR400A Address	WIFI MCU Address
BROM	32KB	0x00000000 – 0x00007FFF	invisible
ROM	128KB	0x00008000 – 0x00027FFF	invisible
SRAMA0	288KB	0x00200000 – 0x00247FFF	invisible
SRAMA1	128KB	0x00248000 – 0x00267FFF	Shared by WIFI and CSI+JPE, CSI+JPE has high priority, APP has lowest priority. WIFI MCU address range is:0x08080000 – 0x0809FFFF CSI+JPE use parts of this SRAM for work SRAM. Only one master access the SRAM at the same time. CSI_JPE_SHARE_SRAM=1, CSI+JPE access 32K bytes (0x00260000 – 0x00267FFF)

			CSI_JPE_SHARE_SRAM=2, CSI+JPE access 64K bytes (0x00258000 – 0x00267FFF) WIFI_SEL_SSRAM=1, WIFI access 32K bytes (0x00260000 – 0x00267FFF) WIFI_SEL_SSRAM=2, WIFI access 64K bytes (0x00258000 – 0x00267FFF) WIFI_SEL_SSRAM=3, WIFI access 96K bytes (0x00250000 – 0x00267FFF) WIFI_SEL_SSRAM=4, WIFI access 128K bytes (0x00248000 – 0x00267FFF) WIFI_SEL_SSRAM=0 & CSI_JPE_SHARE_SRAM=0, AR400A access;
SRAMA2	40KB	0x00268000 – 0x00271FFF	invisible
FLASH ROM	16MB	0x00400000 – 0x013FFFFF	invisible
WIFI Peripheral		0xB9C00000 – 0xXXXXXXXX	0xXXXXXXX- 0xXXXXXXXX
SRAMC	52KB	0x68000000 – 0x6800CFFF	0x08000000 – 0x0800CFFF (AHB RAM)
SRAMD	64KB	0x6800D000 – 0x6801CFFF	0x09000000 – 0x0900FFFF（PAS RAM）
ROM	128KB	invisible	0x00000000 – 0x0001FFFF （ITCM）

2.1.5 CPU

XR872 features an ARM Cortex-M4F processor, which is the most energy efficient ARM processor available. It supports the clock rates from 32KHz up to 384MHz. The processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption.

The ARM Cortex-M4 core has low-latency interrupt processing with the following features:

- Thump-2 instruction set for optimal performance and code size
- Handler and thread modes
- Memory Protection Unit (MPU) for memory protection features
- Floating Point Unit (FPU) to support DSP related function
- Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing
- Three Advanced High-Performance bus AHB-Lite interfaces: ICode, DCode and system bus

- Bit-band support for memory and select peripheral that include atomic bit-band write and read operations
- Wake-up Interrupt Controller (WIC) providing ultra-low power sleep mode support

2.1.6 DMA

There are 8 AHB DMA channels for this DMA controller. Only one channel can be active and the sequence is according to the priority level.

The DMA controller can support 8-bit/16-bit/32-bit data width. The data width of Source and Destination can be different, but the address should be aligned. Although the increase mode of NDMA should be address aligned, but its byte counter should not be multiple. The DMA Source Address, Destination Address, Byte Counter Registers can be modified even if the DMA is started.

2.1.7 Cache

A configurable 40KB cache is implemented to improve the code fetch performance when CPU accesses a non-zero wait-state memory such as external flash or PSRAM.

The core cache is a small block of memory containing a copy of a small portion of cached data in the external memory. If CPU reads a cached data, the data will be copied to the core cache. Once CPU requests the same data again, it can be obtained directly from the core cache (called cache hit) instead of fetching it again from the external memory to achieve zero wait-state latency.

The cache can be disabled and this block of memory can be turned into high speed system memory. The sizes of SRAM and cache can be set to one of the following configurations:

- 40KB cache, 416KB SRAM
- 32KB cache, 424KB SRAM
- 24KB cache, 432KB SRAM
- 16KB cache, 440KB SRAM
- 8KB cache, 448KB SRAM
- 0KB cache, 456KB SRAM

Here, the total cache size with each 8KB block can be set to either I-cache or D-cache. I-cache is only used for external flash or PSRAM read, while D-cache has both read and write functions. I-cache and D-cache can work simultaneous to maximum the performance. The cache system has following features:

- Configurable 1/2/4-way set associate (8KB/16KB/32KB)
- Each way has 512 cache lines with 4-word link size
- 20-bit tag memory: 19-bit high address and 1-bit valid bit

Both I-cache and D-cache can be configured to 1/2/4-way, how to use it depends on system application requirement. The detail configures of I-cache and D-cache please refer to user manual.

2.1.8 Crypto Engine

The Crypto Engine (CE) is one encrypt/decrypt algorithms accelerator. It is suitable for a variety of applications.

Features:

- Supports AES, DES, 3DES, SHA-1, MD5, CRC32/16, SHA256, TRNG
- Supports ECB, CBC, CTR modes for AES/DES/3DES
- Supports 128-bits, 192-bits and 256-bit key size for AES
- Supports 160-bits hardware PRNG with 192-bits seed

The TRNG generates random numbers from the 8 free-run ring oscillators (RCO). IRQ will be issued once the random data is successfully generated.

2.1.9 Timer

Timer 0 and 1 can take their inputs from internal RC oscillator, external 32768Hz crystal or OSC. They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 24-bit programmable overflow counter and work in auto-reload mode or no-reload mode.

The watch-dog is used to resume the controller operation when it had been disturbed by malfunctions such as noise and system errors. It features a down counter that allows a watchdog period of up to 16 seconds. It can generate a general reset or an interrupt request.

2.1.10 RTC

The real time clock (RTC) is for calendar usage. It is built around a 30-bit counter and used to count elapsed time in YY-MM-DD and HH-MM-SS. The unit can be operated by the backup battery while the system power is off. It has a built-in leap year generator.

The alarm generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, both the alarm interrupt and the power management wakeup are activated. In power-off mode, the power management wakeup signal is activated. In this section, there are two kinds of alarm. Alarm 0 is a general alarm; its counter is based on second. Alarm 1 is a weekly alarm; its counter is based on the real time.

2.2Peripherals

2.2.1 GPIO

The XR872 GPIO unit provides as many as 33 GPIO (General Purpose IO) pins. All ports are brought out of the device using alternate function multiplexing. The GPIO function can be multiplexed on a multi-function I/O pin by selecting the GPIO alternate function in the GPIO Controller registers.

There are two types of GPIO designs in XR872: GPIO and AGPIO. Each GPIO can be configured with the following options:

- Input / Output / Floating(Hi-Z) mode
- Input mode: Pull-up or Pull-down
- Output mode: Active driving
- Pull-up/down control: the pull-up and pull-down resistance is 90KΩ with ±30% variation over PVT condition
- External Interrupt IO with 5 trigger modes: high-level, low-level, rising edge, falling edge, double edge
- 9 WAKEUP IOs can be set to wake system by external interrupt at HIBERNATION mode (RTC on only)
- All IOs can be set to wake system by external interrupt in STANDBY mode (RTC and OA domain on)

The digital IO AGPIO function is equivalent to GPIO as shown above. A dedicated internal control signal is used to select between the digital and analog functions. These IOs are multiplexed with 8 channels ADC (1 is internal connected to measure VBAT voltage).

GPIO PA23 has a special function which is used to enter test mode when it is high on first power-up. So we need to keep it from pulling high (floating or tie low) to have whole chip power up correctly.

Table 2-3 XR872AT GPIO Multiplexing

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
PA00	SPI1_MOSI	SD_CMD	TWI1_SCL	CSI_D0	EINTA0
PA01	SPI1_MISO	SD_DATA0	TWI1_SDA	CSI_D1	EINTA1
PA02	SPI1_CLK	SD_CLK	UART0_TX	CSI_D2	EINTA2
PA03	SPI1_CS0	SD_DATA1	UART0_RX	CSI_D3	EINTA3
PA04/WUPIO0	UART1_RTS	SD_DATA2	TWI0_SCL	CSI_D4	EINTA4
PA05/WUPIO1	UART1_CTS	SD_DATA3	TWI0_SDA	CSI_D5	EINTA5
PA06/WUPIO2	UART1_RX	SPI1_CS1	TWI0_SCL	CSI_D6	EINTA6
PA07/WUPIO3	UART1_TX	SPI1_CS2	TWI0_SDA	CSI_D7	EINTA7
PA08	FEM_CTRL1	PWM0/ECT0	TWI1_SCL	CSI_PCLK	EINTA8
PA09	FEM_CTRL2	PWM1/ECT1	TWI1_SDA	CSI_MCLK	EINTA9
PA10	ADC_CH0	PWM2/ECT2	DMIC_CLK	CSI_HSYNC	EINTA10
PA11	ADC_CH1	PWM3/ECT3	DMIC_DATA	CSI_VSYNC	EINTA11
PA12	ADC_CH2	PWM4/ECT4	I2S_MCLK	IR_TX	EINTA12
PA13	ADC_CH3	PWM5/ECT5	I2S_BCLK	UART1_TX	EINTA13
PA14	ADC_CH4	PWM6/ECT6	I2S_DI	UART1_RX	EINTA14
PA15	ADC_CH5	PWM7/ECT7	I2S_DO	UART1_CTS	EINTA15
PA16	ADC_CH6	IR_RX	I2S_LRCLK	UART1_RTS	EINTA16
PA19/WUPIO5	UART2_RTS	TWI0_SCL	PWM0/ECT0	SPI1_MOSI	EINTA19
PA20/WUPIO6	UART2_CTS	TWI0_SDA	PWM1/ECT1	SPI1_MISO	EINTA20
PA21/WUPIO7	UART2_RX	DMIC_CLK	PWM2/ECT2	SPI1_CLK	EINTA21
PA22/WUPIO8	UART2_TX	DMIC_DATA	PWM3/ECT3	SPI1_CS0	EINTA22
PA23/WUPIO9/TEST	EXT_DCDC_PUP	/	FEM_CTRL1	FEM_CTRL2	EINTA23
PB00	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	EINTB0
PB01	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	EINTB1
PB02	SWD_TMS	JTAG_TD0	PWM6/ECT6	FLASH_WP/IO2	EINTB2
PB03	SWD_TCK	JTAG_TDI	PWM7/ECT7	FLASH_HOLD/IO	EINTB3
PB04	SPI0_MOSI	SD_CMD	UART1_TX	FLASH_MOSI/IO0	EINTB4
PB05	SPI0_MISO	SD_DATA0	UART1_RX	FLASH_MISO/IO1	EINTB5
PB06	SPI0_CS0	FEM_CTRL2	UART1_CTS	FLASH_CS	EINTB6
PB07	SPI0_CLK	SD_CLK	UART1_RTS	FLASH_CLK	EINTB7
PB16	/	SD_CMD	/	/	EINTB16
PB17	/	SD_DATA0	/	/	EINTB17
PB18	/	SD_CLK	/	/	EINTB18

Table 2-4 XR872ET GPIO Multiplexing

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
PA00	SPI1_MOSI	SD_CMD	TWI1_SCL	CSI_D0	EINTA0
PA01	SPI1_MISO	SD_DATA0	TWI1_SDA	CSI_D1	EINTA1
PA02	SPI1_CLK	SD_CLK	UART0_TX	CSI_D2	EINTA2
PA03	SPI1_CS0	SD_DATA1	UART0_RX	CSI_D3	EINTA3
PA04/WUPIO0	UART1_RTS	SD_DATA2	TWI0_SCL	CSI_D4	EINTA4
PA05/WUPIO1	UART1_CTS	SD_DATA3	TWI0_SDA	CSI_D5	EINTA5
PA06/WUPIO2	UART1_RX	SPI1_CS1	TWI0_SCL	CSI_D6	EINTA6
PA07/WUPIO3	UART1_TX	SPI1_CS2	TWI0_SDA	CSI_D7	EINTA7
PA08	FEM_CTRL1	PWM0/ECT0	TWI1_SCL	CSI_PCLK	EINTA8
PA09	FEM_CTRL2	PWM1/ECT1	TWI1_SDA	CSI_MCLK	EINTA9
PA10	ADC_CH0	PWM2/ECT2	DMIC_CLK	CSI_HSYNC	EINTA10
PA11	ADC_CH1	PWM3/ECT3	DMIC_DATA	CSI_VSYNC	EINTA11
PA19/WUPIO5	UART2_RTS	TWI0_SCL	PWM0/ECT0	SPI1_MOSI	EINTA19
PA20/WUPIO6	UART2_CTS	TWI0_SDA	PWM1/ECT1	SPI1_MISO	EINTA20
PA21/WUPIO7	UART2_RX	DMIC_CLK	PWM2/ECT2	SPI1_CLK	EINTA21
PA22/WUPIO8	UART2_TX	DMIC_DATA	PWM3/ECT3	SPI1_CS0	EINTA22
PA23/WUPIO9/T	EXT_DCDC_PUP	/	FEM_CTRL1	FEM_CTRL2	EINTA23
PB00	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	EINTB0
PB01	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	EINTB1
PB02	SWD_TMS	JTAG_TD0	PWM6/ECT6	FLASH_WP/IO2	EINTB2
PB03	SWD_TCK	JTAG_TDI	PWM7/ECT7	FLASH_HOLD/IO	EINTB3
PB04	SPI0_MOSI	SD_CMD	UART1_TX	FLASH_MOSI/IO	EINTB4
PB05	SPI0_MISO	SD_DATA0	UART1_RX	FLASH_MISO/IO	EINTB5
PB06	SPI0_CS0	FEM_CTRL2	UART1_CTS	FLASH_CS	EINTB6
PB07	SPI0_CLK	SD_CLK	UART1_RTS	FLASH_CLK	EINTB7

2.2.2 UART

The XR872 provides 3 UART controllers: one is used for debug and two with auto-flow control are used for communication with external devices. The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

Features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- Support DMA controller interface
- Support Software/ Hardware Flow Control
- Support IrDA 1.0 SIR
- Support RS-485 mode
- Support configurable baud rate from 9600, 19200, 38400, 115200 and 921600 etc.
- Support baud rate detection

2.2.3 SPI

The XR872 features two SPI controllers. Each controller can be configured to a SPI master or a SPI slave. They are used as an extension interface to control the peripheral devices. They support two options of clock polarity (CPOL) and two options of initial clock phase (CPHA).

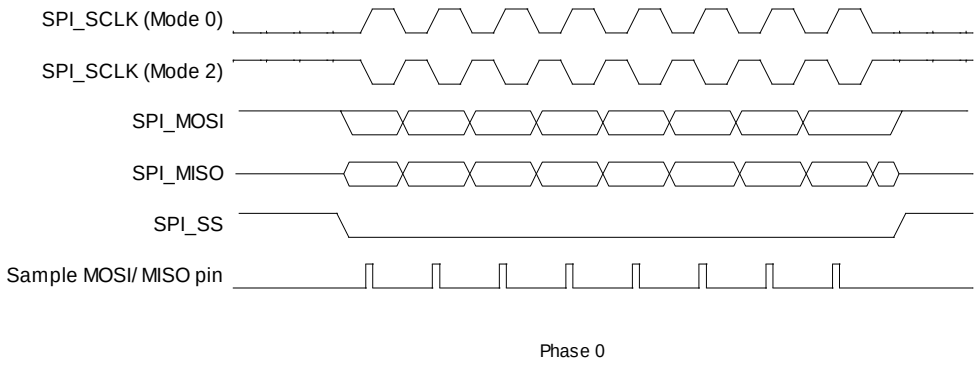


Figure 2-5 SPI Phase 0 Transfer Format

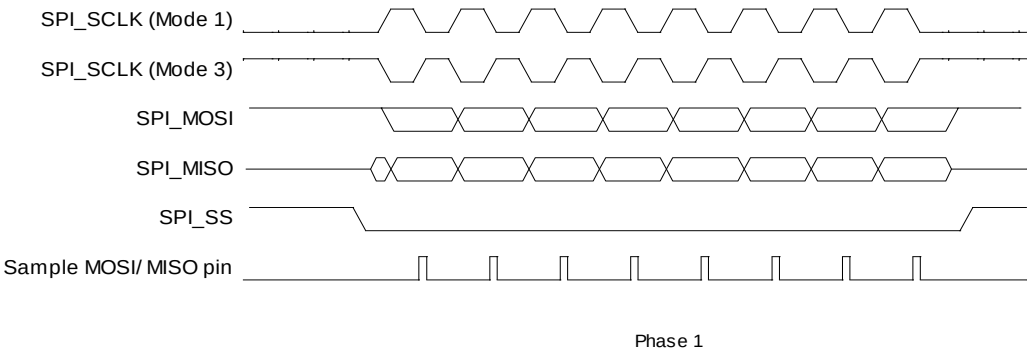


Figure 2-6 SPI Phase 1 Transfer Format

2.2.4 TWI

The XR872 features two TWI serial interfaces. They can be configured as master and salve mode. Each TWI controller supports three IO mapping. The TWI controllers can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

Features:

- Compatible with IIC protocol and SCCB protocol
- Software-programmable for Slave or Master
- Supports Repeated START signal
- Multi-master systems supported
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies

2.2.5 PWM

XR872 features 8 PWMs to generate pulse sequences with programmable frequency a duration for LCD, vibrators and other devices. The PWM controller provides 8 PWM channels, which are divided into four pairs of PWM pair, each is composed of three parts: a clock controller, two timer modules, a programmable dead-zone generator. The PWM channel logic can be configured as input capture function. The capturer detects the rising edge and the

falling edge of the signal and calculates the high-level and the low-level duration with a 16-bit counter.

Features:

- 8 PWM channels, divided into 4 PWM pairs
- Supports pulse, period and complementary pair outputs
- Support input capture
- Programmable dead-zone generator
- Configurable output frequency, 0%-100% duty adjustable

2.2.6 SD/MMC/SDIO

XR872 features a SD/MMC controller can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memo), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card and Consumer Electronics Advanced Transport Architecture (CE-ATA).

Features:

- Supports Secure Digital memory protocol commands (compatible with SD3.0)
- Supports Secure Digital I/O protocol commands
- Supports Multimedia Card protocol commands
- Supports CE-ATA digital protocol commands
- Supports one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 4.41) or CE-ATA device
- Supports hardware CRC generation and error detection
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports block size of 1 to 65535 bytes
- Supports internal DMA controller

2.2.7 CIR

XR872 features an infrared remote transmitter and a receiver controller. Through the process control pulse waveform, the remote controller can support a variety of infrared protocol.

The IR receiver controller features:

- Full physical layer implementation
- Support IR for remote control
- 64x8 bits FIFO for data buffer

The IR transmitter controller features:

- Full physical layer implementation
- 128 bytes FIFO for data buffer
- Configurable carrier frequency
- Interrupt and DMA support

2.2.8 GPADC

XR872 features one GPADC function. The ADC function contains a 8-channel analog switch, a single end input asynchronous 12-bit SAR (Successive Approximation Register) ADC. The channels 0 to 6 are used to detect the voltage of the external input and the channel 8 is dedicated to detect the voltage of the VBAT. The channel 7 is NC.

Features:

- 12-bit Resolution and 10-bit effective SAR type A/D converter
- 8-channel multiplexer, 7 normal channel and 1 VBAT voltage detection channel
- 64 FIFO depth of data register
- DMA support
- Power supply 1.62~3.6V，internal Capless LDO provide 1.4V/2.5V/0.4*VDD-EXT to Vref
- Maximum Sampling frequency: 1 MHz
- Support self-calibration
- Support data compare and interrupt
- Support four operation mode: Single conversion mode, Single-cycle conversion mode, Continuous conversion mode, Outbreak conversion mode

2.2.9 I2S

XR872 features one DAI(Digital Audio Interface) Controller function. The controller supports standard I2S format, Left-justified Mode format, Right-justified Mode format, PCM Mode format and TDM Mode format.

Features:

- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Support different sample period width in each interface when using LRCK and LRCKR at the same time
- Support full-duplex synchronous work mode
- Support Master / Slave mode

- Support adjustable interface voltage
- Support clock up to 100MHz
- Support adjustable audio sample resolution from 8-bit to 32-bit.
- Support up to 8 slots which has adjustable width from 8-bit to 32-bit.
- Support sample rate from 8KHz to 192KHz
- Support up to 4 data output pin
- Support 8-bits u-law and 8-bits A-law companded sample
- One 128 depth x 32-bit width FIFO for data transmit, one 64 depth x 32-bit width FIFO for data receive
- Support programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)

2.3Video Subsystem

2.3.1 CSI

The Camera Serial Interface (CSI) is a parallel image input interface. It includes the following features:

- 8 bits input data
- Support digital camera(DC) interface and CCIR656 interface
- Pass raw data direct to memory
- Pass jpeg data direct to memory
- Pass YUV420 data to JPEG
- Convert YUV422 data to YUV420
- support X/Y scale 1/2 and cropwin

2.3.2 JPEG

- Supports JPEG base line;
- Supports online encoding mode with CSI;
- Supports nv12 input format in offline encoding mode
- Supports configurable picture resolutions
- Minimum picture resolution: 32x32
- Offline maximum picture resolution: 1920x1088

- Online maximum picture resolution: 1920x1088
- Supports online 640x480@60fps and online 1280x720@40fps
- Supports offline 640x480@60fps and offline 1280x720@20fps
- Supports bitrate control through quantization table

2.4AUDIO Subsystem

2.4.1 DMIC

XR872 features one DMIC Controller which supports a 2-channels digital microphone interface, the DMIC controller can output 128fs (fs= ADC sample rate).

Features:

- Support up to 2 channels
- Support sample rate from 8KHz to 24KHz

2.4.2 AUDIO CODEC

XR872 Integrated one ADC and one DAC for audio microphone in and playback, another ADC in line-in channel used for smart audio AEC feature which record audio signal from power amplifier output.

ADC (Microphone Input)

- Mono ADC with 94dB SNR typically(A-weight)
- –90 dB THD+N @ 0 dB boost and 3.0Vpp differential input
- Mono Fully-differential analog microphone input with 0dB~33dB boost amplifier gain
- ADC sample rates supported: 8k, 11.025k, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz

Line-in (AEC Input)

- Mono ADC with 94dB SNR typically (A-weight)
- –90 dB THD+N @ 0 dB boost and 3.0Vpp differential input
- Mono Fully-differential analog microphone input with -3dB~24dB boost amplifier gain
- ADC sample rates supported: 8k, 11.025k, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz

DAC

- Mono DAC with 100dB SNR typically (A-weight)
- –90 dB THD+N @ -3dBFS

- Mono Fully-differential Line Output with 1.0Vrms maximum output voltage
- DAC sample rates supported: 8k, 11.025k, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 96kHz, 192kHz

Power Supply

Integrated one low noise LDO for Codec with features as bellow:

- LDO input from 1.8~3.6V
- LDO output is programmable from 1.6~3.025V
- The default output voltage of LDO is set to 2.8V to maintain maximum voltage range. When VBAT is higher than 2.3V, it maintains good PSRR for Codec. While VBAT is lower than 2.3V, it will have some performance degradation because of power noise to ADC and DAC.

2.5Wi-Fi Subsystem

2.5.1 Wi-Fi MAC

Supports MAC enhancements including:

- 802.11d - Regulatory domain operation
- 802.11e - QoS including WMM
- 802.11h - Transmit power control dynamic and frequency selection
- 802.11i - Security including WPA2 compliance
- 802.11r - Roaming

2.5.2 Wi-Fi Baseband

Features:

- Compatible with IEEE 802.11 b/g/n standard
- 802.11n MCS0-7 with data rate up to 72.2Mbps (BPSK, r=1⁄2 through 64QAM, r=5⁄6)
- 6M~54M data rate for 802.11g
- DSSS, CCK modulation with long and short preamble
- Short Guard Interval
- Long Guard Interval
- RX antenna Diversity

2.5.3 Wi-Fi Radio

Features:

- Integrated 2.4GHz PA, LNA, and T/R switch
- Internal impedance matching network and harmonic filter allow chip to connect to antenna directly
- High Power Amplifier with 1.8~5.5V full range directly support XRADIOTECH's MPD™ technology ensure linearity tracking automatically to always keep EVM and mask within specifications
- Special Architecture and Device design to keep the reliability of PA up to 5.5V high voltage and also deliver high output power (>25dBm)

2.5.4 Front End Module Control

For applications that use external front-end components, the XR872 provides the ability to control them with two antenna switch control outputs named:

- FEM_CTRL1: TX_EN
- FEM_CTRL2: RX_EN

FEM_CTRL1 and FEM_CTRL2 are used to control TX and RX signal path separately. It is very useful when customer want to use XR872 to extend range coverage by add addition high output power RF PA. The typical extend application is below:

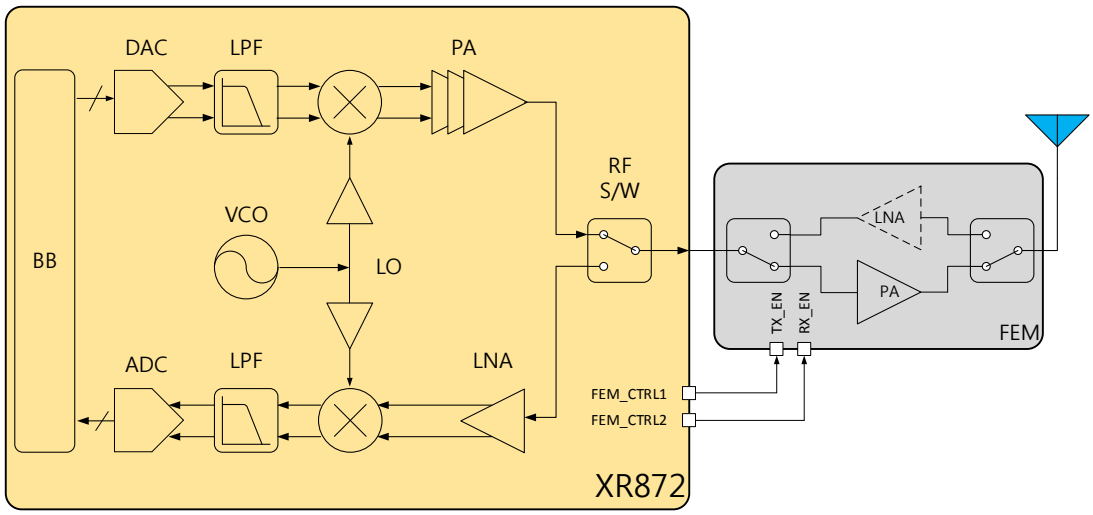


Figure 2-7 FEM Control Application Diagram

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol	Parameter	Maximum rating	Unit
I/O	In/Out current for input and output	-35 to 35	mA
VBAT	1.8-5.5V Power supply	-0.3 to 6	V
CHIP_PWD	RESET pin for chip	-0.3 to 6	V
VDD_ANA	Power supply	-0.3 to 3	V
VDD_DIG	Power supply	-0.3 to 1.5	V
VDD_EXT	Power supply	-0.3 to 4	V
VDD_PSM	Power supply	-0.2 to 2.45	V
VDD_IO	Power supply	-0.3 to 4	V
AVDD	Power supply	-0.3 to 4	V
T_{opr}	Operating Temperature	-40 to 85	^{o}C
$T_{junction}$	Junction Temperature	125	^{o}C
T_{stg}	Storage Temperature	-65 to 150	^{o}C
VESD	HBM	±2000	V
VESD	CDM	±500	V

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{opr}	Ambient Operating Temperature	-40	-	85	°C
VBAT	Power supply of chip input	1.8	5/3.6/1.8	5.5	V
CHIP_PWD	RESET	1.8	-	5.5	V
VDD_ANA	Power supply of analog/RF input	1.4	1.8	2.5	V
VDD_DIG	Power supply of digital input	0.6	1.1	1.35	V
VDD_EXT	Power supply of external device output	1.62	3.3	3.5	V
VDD_PSM	Power supply of PSRAM input	1.62	1.8	1.98	V
VDD_IO	Power supply of GPIO input	1.62	3.3/1.8	3.6	V
AVDD	Power supply of Codec output	1.62	2.8/1.8	2.95	V

3.3 Digital IO Characteristics

Table 3-3 DC Characteristics of VDD_IO=3.3V

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage	VDD_IO=3.3V	-0.3	1.32	V
V_{IH}	Input High Voltage	VDD_IO=3.3V	2.06	3.6	V
V_{OL}	Output Low Voltage	|IOL| = 7.5~50 mA	-0.3	0.4	V
V_{OH}	Output High Voltage	|IOH| = 7.5~50 mA	2.9	3.6	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	35	95	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	35	95	KΩ

Table 3-4 DC Characteristics of VDD_IO=1.8V

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage	VDD_IO=1.8V	-0.3	0.65	V
V_{IH}	Input High Voltage	VDD_IO=1.8V	1.18	1.98	V

V_{OL}	Output Low Voltage	|IOL| = 2.25~15 mA	-0.3	0.4	V
V_{OH}	Output High Voltage	|IOH| = 2.25~15 mA	1.44	2	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	63	190	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	63	190	KΩ

3.4 Bootstrap Modes and Pins

Table 3-5 Bootstrap pins

Symbol	Bootstrap Function Name	Value	Description
PA23	Test Mode	0	Normal operation mode
		1	Enter into test/debug mode when releasing CHIP_PWD
PB02, PB03	Boot Mode	00	when releasing CHIP_PWD will cause the system going to firmware update mode.
		01	Internal normal boot
		10	
		11	

3.5 High Frequency Reference Clock

External XTAL and Built-in Oscillator

Table 3-6 External High Frequency Crystal Characteristics Requirements

Parameter	Conditions	Min.	Typ.	Max.	Unit
Frequency Range			24, 26, 40,		MHz
ESR		-	-	60	Ohm
C_{in_xtal}(1)	Single-ended	0	-	25.4	pF
C_{shunt}(1)		-	2	-	pF
Load Capacitance(1)		-	0	27	pF
Crystal Frequency Accuracy at Nominal Temp.	25 °C	-10	-	+10	ppm
Crystal Drift Due to Temperature	-20 to +85 °C	-10	-	+10	ppm
Crystal Pull Ability		10	-	150	ppm/pF

(1) The load capacitance value (C_{load}) and shunt capacitance value(C_{shunt}) depends on XTAL model, XTAL1 and XTAL2 pin have inside capacitance (C_{in_xtal}), so external added load capacitance value (PCB Welding Capacitance) C_{load_ext} = C_{load} * 2 - C_{in_xtal} - C_{pcb} - C_{shunt} * 2, C_{pcb} is PCB parasitic capacitance(single-ended). C_{in_xtal} has tuning range about 25.4pF, which is controlled by software, for details please go to software user manual.

3.6 Low Frequency Reference Clock

External XTAL and Built-in Oscillator

Table 3-7 External Low Frequency Crystal Characteristics Requirements

Parameter	Conditions	Min.	Typ.	Max.	Unit
Frequency Range			32.768		KHz
ESR		-	-	60	Ohm
C_{in_xtal}(1)	Single-ended	0	3.5	15	pF
Load Capacitance(1)		-	16	27	pF
Oscillator Tuning Range(2)		+/-20	+/-50	+/-70	ppm

Crystal Frequency Accuracy at Nominal Temp.	25 °C	-150	-	+150	ppm
Crystal Drift Due to Temperature	-20 to +85 °C	-100	-	+100	ppm
Crystal Pull Ability		10	-	150	ppm/pF

3.7 Audio Codec Specifications

Table 3-8 ADC Specifications

Condition: VBAT=3.6V, AVDD=2.0V, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Full-Scale Input Level	PGA Gain=0dB@THD<-40dB		TBD		Vrms
SNR (A-weighted)	PGA Gain=0dB		TBD		dB
THD+N (-3dBFS 1KHz input)			TBD		dB
SNR (A-weighted)	PGA Gain=18dB		TBD		dB
THD+N (-3dBFS 1KHz input)			TBD		dB
SNR (A-weighted)	PGA Gain=30dB		TBD		dB
THD+N (-3dBFS 1KHz input)			TBD		dB

Table 3-9 Line-in Specifications

Condition: VBAT=3.6V, AVDD=2.0V, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Full-Scale Input Level	PGA Gain=0dB@THD<-40dB		TBD		Vrms
SNR (A-weighted)	PGA Gain=0dB		TBD		dB
THD+N (-3dBFS 1KHz input)			TBD		dB
SNR (A-weighted)	PGA Gain=24dB		TBD		dB
THD+N (-3dBFS 1KHz input)			TBD		dB

Table 3-10 DAC Specifications

Condition: VBAT=3.6V, AVDD=2.0V, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Full-Scale Output Level	R_{Load}=100K		TBD		Vrms
SNR (A-weighted)			TBD		dB
THD+N(-3dBFS 1KHz output)			TBD		dB

3.8 Wi-Fi 2.4G RF Receiver Specifications

Table 3-11 RF Receiver Specifications

Condition: VBAT=3.6V, VDD_ANA=1.8V, XTAL=40MHz, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412		2484	MHz
RX Sensitivity (802.11b)	1Mbps DSSS		TBD		dBm
	2Mbps DSSS		TBD		dBm
	5.5Mbps CCK		TBD		dBm
	11Mbps CCK		TBD		dBm
RX Sensitivity (802.11g)	6Mbps OFDM		TBD		dBm
	9Mbps OFDM		TBD		dBm
	12Mbps OFDM		TBD		dBm
	18Mbps OFDM		TBD		dBm
	24Mbps OFDM		TBD		dBm
	36Mbps OFDM		TBD		dBm
	48Mbps OFDM		TBD		dBm
	54Mbps OFDM		TBD		dBm
RX Sensitivity (802.11n, 20MHz)	MCS 0		TBD		dBm
	MCS 1		TBD		dBm
	MCS 2		TBD		dBm
	MCS 3		TBD		dBm
	MCS 4		TBD		dBm
	MCS 5		TBD		dBm
	MCS 6		TBD		dBm
	MCS 7		TBD		dBm
Maximum Receive Level	6 Mbps OFDM		TBD		dBm
	54 Mbps OFDM		TBD		dBm

	MCS0		TBD		dBm
	MCS7		TBD		dBm
Receive Adjacent Channel Rejection	1 Mbps CCK		TBD		dBc
	11 Mbps CCK		TBD		dBc
	BPSK rate 1⁄2, 6 Mbps OFDM		TBD		dBc
	64QAM rate 3⁄4, 54 Mbps OFDM		TBD		dBc
	HT20, MCS 0, BPSK rate 1⁄2		TBD		dBc
	HT20, MCS 7, 64QAM rate 5⁄6		TBD		dBc

3.9 Wi-Fi 2.4G RF Transmitter Specifications

Table 3-12 RF Transmitter Specifications 1

Condition1: VBAT=3.6V, VDD_ANA=1.8V, XTAL=40MHz, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412		2484	MHz
TX Power[1]	1Mbps DSSS mask compliant		TBD		dBm
	11Mbps CCK mask compliant		TBD		dBm
	6Mbps OFDM mask compliant		TBD		dBm
	54Mbps OFDM EVM compliant		TBD		dBm
	HT20, MCS 0 mask compliant		TBD		dBm
	HT20, MCS 7 EVM compliant		TBD		dBm
EVM	1Mbps DSSS 16dBm		TBD		dB
	11Mbps CCK 16dBm		TBD		dB
	6Mbps OFDM 15dBm		TBD		dB
	54Mbps OFDM EVM 15dBm		TBD		dB
	HT20, MCS 0 mask 15dBm		TBD		dB
	HT20, MCS 7 EVM 14dBm		TBD		dB
Carrier Suppression				-30	dBc

Accuracy of Power Control	Closed-loop control across all temperature ranges and channels	-1.5		1.5	dB
Harmonic Output Power	2nd Harmonic			-40	dBm/MHz
	3rd Harmonic			-45	dBm/MHz

1. Refer to IEEE 802.11 specification for Tx spectrum limits:

- 802.11b mask (18.4.7.3)

- 802.11g mask (19.5.4)

- 802.11g EVM (17.3.9.6.3)

- 802.11n HT20 mask (20.3.21.1)

- 802.11n HT20 EVM (20.3.21.7.3)

Table 3-13 RF Transmitter Specifications 2

Condition2: VBAT=5.0V, VDD_ANA=1.8V, XTAL=40MHz, Temperature=25°C

Parameter	**Description**	**Performance**			
		Min.	**Typ.**	**Max.**	**Unit**
Frequency Range	Center channel frequency	2412		2484	MHz
TX Power[1]	1Mbps DSSS mask compliant		TBD		dBm
	11Mbps CCK mask compliant		TBD		dBm
	6Mbps OFDM mask compliant		TBD		dBm
	54Mbps OFDM EVM compliant		TBD		dBm
	HT20, MCS 0 mask compliant		TBD		dBm
	HT20, MCS 7 EVM compliant		TBD		dBm
EVM	1Mbps DSSS 16dBm		TBD		dBm
	11Mbps CCK 16dBm		TBD		dBm
	6Mbps OFDM 15dBm		TBD		dBm
	54Mbps OFDM EVM 15dBm		TBD		dBm
	HT20, MCS 0 mask 15dBm		TBD		dBm
	HT20, MCS 7 EVM 14dBm		TBD		dBm
Carrier Suppression				-30	dBc

Accuracy of Power Control	Closed-loop control across all temperature ranges and channels	-1.5		1.5	dB
Harmonic Output Power	2nd Harmonic			-40	dBm/MHz
	3rd Harmonic			-45	dBm/MHz

Table 3-14 RF Transmitter Specifications 3

Condition3: VBAT=1.8V, VDD_ANA=1.5V, XTAL=40MHz, Temperature=25°C

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412		2484	MHz
TX Power[1]	1Mbps DSSS mask compliant		TBD		dBm
	11Mbps CCK mask compliant		TBD		dBm
	6Mbps OFDM mask compliant		TBD		dBm
	54Mbps OFDM EVM compliant		TBD		dBm
	HT20, MCS 0 mask compliant		TBD		dBm
	HT20, MCS 7 EVM compliant		TBD		dBm
EVM	1Mbps DSSS 16dBm		TBD		dBm
	11Mbps CCK 16dBm		TBD		dBm
	6Mbps OFDM 15dBm		TBD		dBm
	54Mbps OFDM EVM 15dBm		TBD		dBm
	HT20, MCS 0 mask 15dBm		TBD		dBm
	HT20, MCS 7 EVM 14dBm		TBD		dBm
Carrier Suppression				-30	dBc
Accuracy of Power Control	Closed-loop control across all temperature ranges and channels	-1.5		1.5	dB
Harmonic Output Power	2nd Harmonic			-40	dBm/MHz
	3rd Harmonic			-45	dBm/MHz

3.10 Power Consumption

Table 3-15 Power Consumption 1

Temp=25°C, VBAT=3.6V, VDD_ANA=1.8V, external DC-DC 90% efficiency, MCU 240MHz

Power Mode	MCU State	Wi-Fi State	TX/RX	Test Condition		Current Consumption			Unit
						Min.	Typ.	Max.	
ACTIVE	ACTIVE	Active	TX[1]	1M DSSS	19dBm		TBD		mA
				11M CCK	19dBm		TBD		mA
				6M OFDM	15dBm		TBD		mA
				54M OFDM	15dBm		TBD		mA
				HT20, MCS0	15dBm		TBD		mA
				HT20, MCS7	14dBm		TBD		mA
			RX	1M DSSS	-		TBD		mA
				11M CCK	-		TBD		mA
				54M OFDM	-		TBD		mA
				HT20, MCS0	-		TBD		mA
				HT20, MCS7	-		TBD		mA
STANDBY	SLEEP	Active	TX[1]	1M DSSS, null frame	19dBm		TBD		mA
			RX	RX listen	-		TBD		mA
				1M DSSS	-		TBD		mA
		PS Mode[2]	RX	DTIM1	-		TBD		uA
				DTIM3	-		TBD		uA
				DTIM8	-		TBD		uA
				DTIM10	-		TBD		uA
		OFF	-	-	-		TBD		uA
HIBERNATION[3]	OFF	OFF	-	-	-		TBD		uA
SHUTDOWN[4]	OFF	OFF	-	-	-		TBD		uA

1. Data is captured at TX continues mode on the duration of transmitting;

2. Use XR872 by external 32K XTAL, Beacon length 1ms；

3. RTC and wake up timer on only;

4. CHIP_PWD keeps at low level;

Table 3-16 Power Consumption 2

Temp=25°C, VBAT=3.6V, VDD_ANA=1.8V, Internal TOP LDO supply, MCU 240MHz

Power Mode	MCU State	Wi-Fi State	TX/RX	Test Condition		Current Consumption			Unit
						Min.	Typ.	Max.	
ACTIVE	ACTIVE	Active	TX[1]	1M DSSS	19dBm		TBD		mA
				11M CCK	19dBm		TBD		mA
				6M OFDM	15dBm		TBD		mA
				54M OFDM	15dBm		TBD		mA
				HT20, MCS0	15dBm		TBD		mA
				HT20, MCS7	14dBm		TBD		mA
			RX	1M DSSS	-		TBD		mA
				11M CCK	-		TBD		mA
				54M OFDM	-		TBD		mA
				HT20, MCS0	-		TBD		mA
				HT20, MCS7	-		TBD		mA
STANDBY	SLEEP	Active	TX[1]	1M DSSS, null frame	19dBm		TBD		mA
			RX	RX listen	-		TBD		mA
				1M DSSS	-		TBD		mA
		PS Mode[2]	RX	DTIM1	-		TBD		uA
				DTIM3	-		TBD		uA
				DTIM8	-		TBD		uA
				DTIM10	-		TBD		uA
		OFF	-	-	-		TBD		uA
HIBERNATION[3]	OFF	OFF	-	-	-		TBD		uA

SHUTDOWN[4]	OFF	OFF	-	-	-		TBD		uA

1. Data is captured at TX continues mode on the duration of transmitting;

2. Use XR872 by external 32K XTAL, Beacon length 1ms；

3. RTC and wake up timer on only;

4. CHIP_PWD keeps at low level;

4 Package Specifications

4.1 Pin Layout

XR872 use 6mm x 6mm QFN and 5mm x 5mm packages for different feature list.

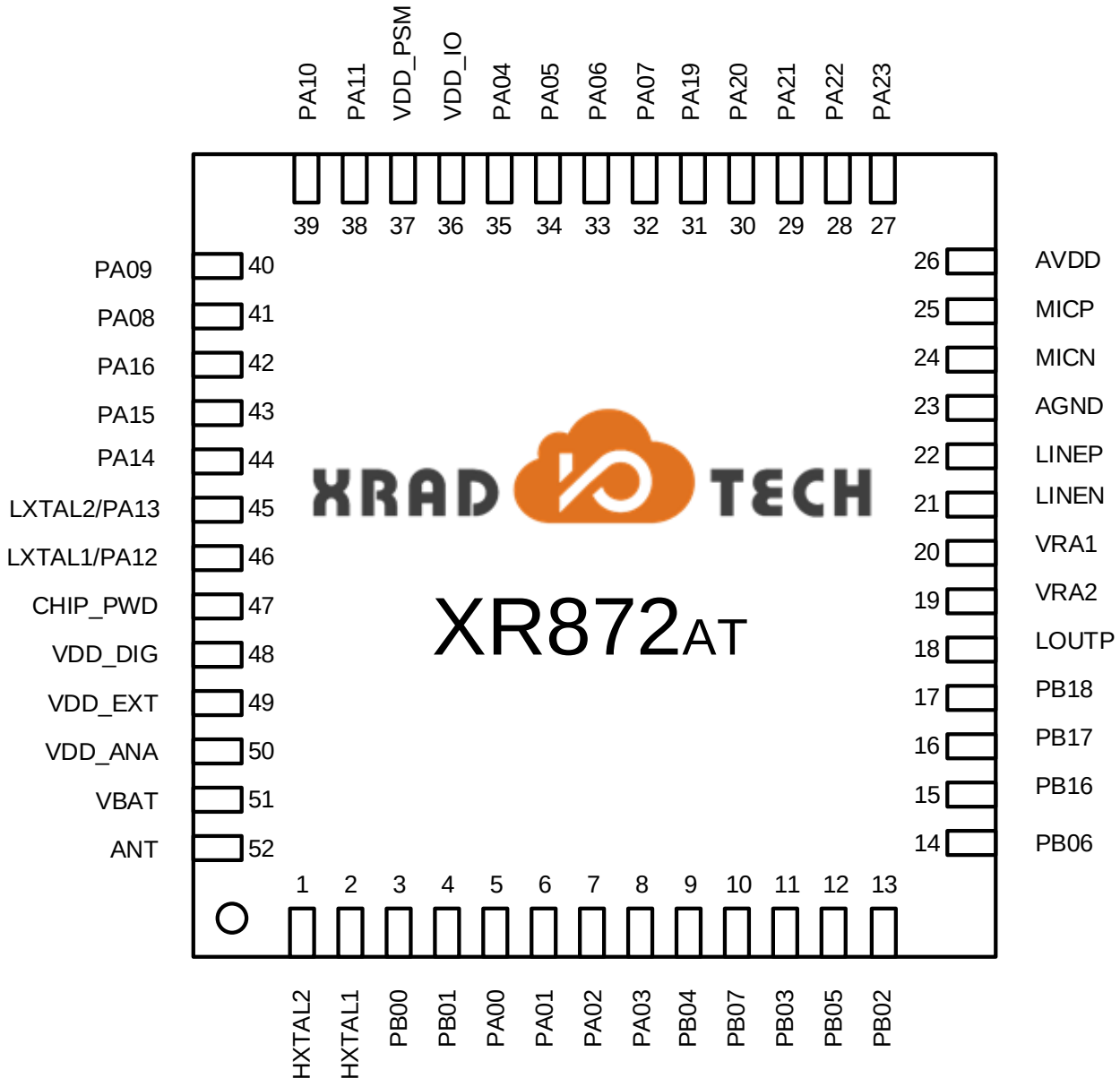


Figure 4-1 XR872AT Pin Layout

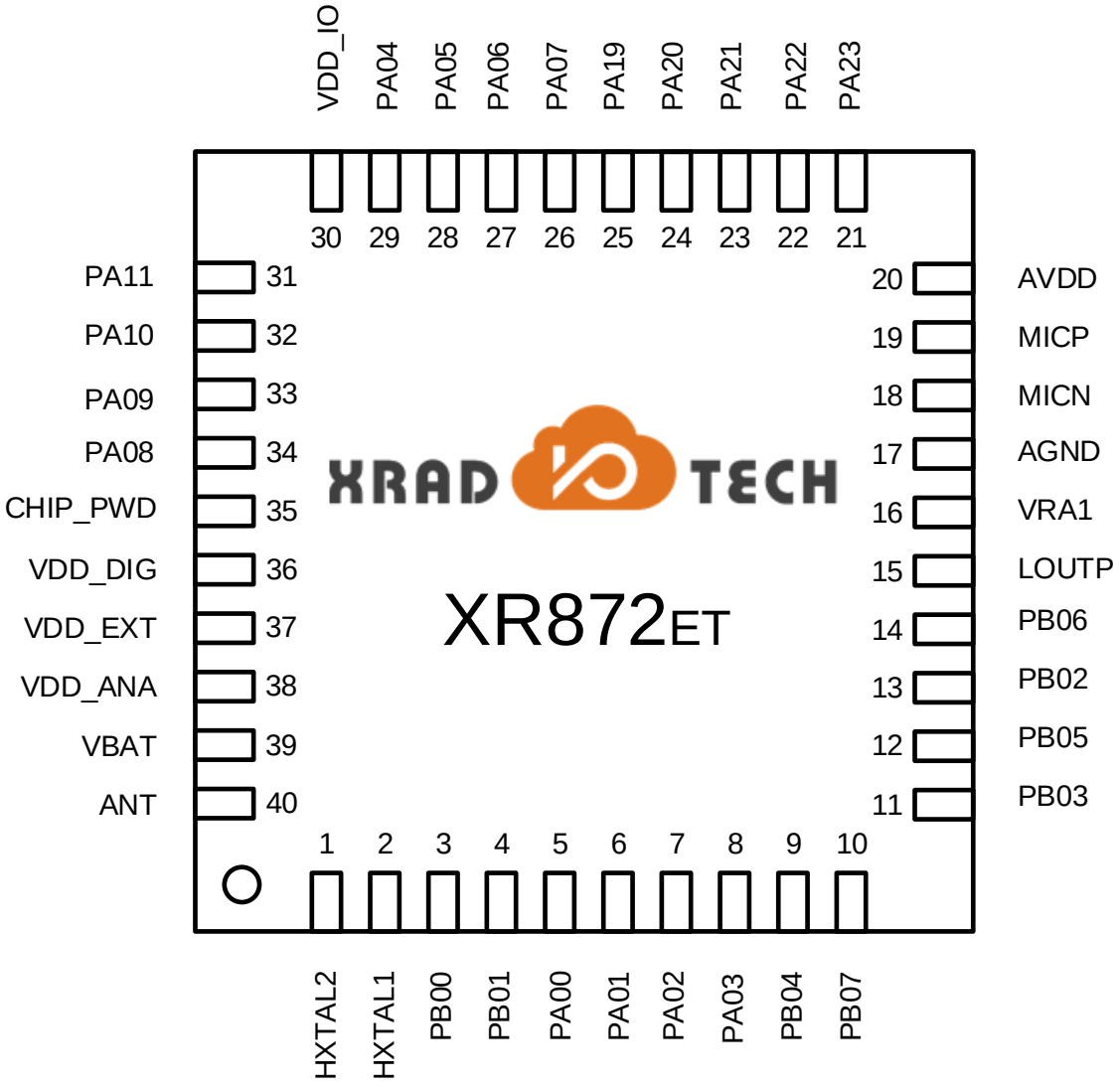


Figure 4-2 XR872ET Pin Layout

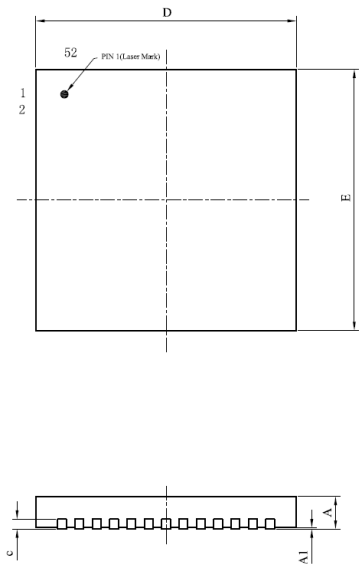
4.2 Pin Descriptions

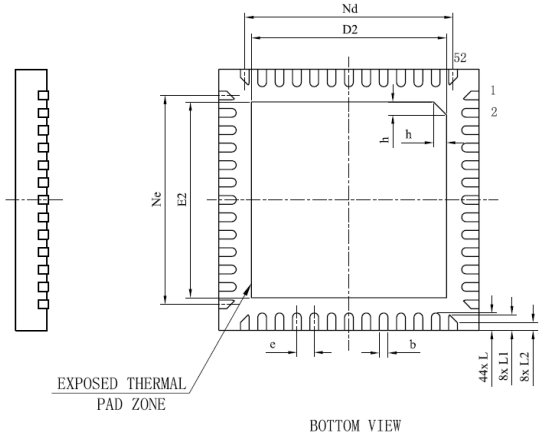
Table 4-1 Pin Description

Pin Name	I/O	XR872AT	XR872ET	Pin Description
HXTAL1	Analog	2	2	40MHz crystal
HXTAL2	Analog	1	1	40MHz crystal
LXTAL1	Analog	46	/	32.768KHz crystal
LXTAL2	Analog	45	/	32.768KHz crystal
CHIP_PWD	Input	47	35	Chip Power Down/System Reset
VDD_ANA	Power	50	38	Analog power supply
VDD_DIG	Power	48	36	1.1V digital power supply
VBAT	Power	51	39	1.8-5.5V power supply
VDD_EXT	Power	49	37	external device power supply
VDD_IO	Power	36	30	GPIO power supply
VDD_PSM	Power	37	/	PSRAM power supply
AVDD	Power	26	20	Codec ldo output
VRA1	Analog	20	16	Codec analog decap output1
VRA2	Analog	19	/	Codec analog decap output2
AGND	Ground	23	17	Codec analog gnd
PA00	In/Out	5	5	Programmable input/output
PA01	In/Out	6	6	Programmable input/output
PA02	In/Out	7	7	Programmable input/output
PA03	In/Out	8	8	Programmable input/output
PA04	In/Out	35	29	Programmable input/output, wakeup io
PA05	In/Out	34	28	Programmable input/output, wakeup io
PA06	In/Out	33	27	Programmable input/output, wakeup io
PA07	In/Out	32	26	Programmable input/output, wakeup io
PA08	In/Out	41	34	Programmable input/output, gpadc in
PA09	In/Out	40	33	Programmable input/output, gpadc in

PA10	In/Out	39	32	Programmable input/output, gpadc in
PA11	In/Out	38	31	Programmable input/output, gpadc in
PA12	In/Out	46	34	Programmable input/output, gpadc in
PA13	In/Out	45	/	Programmable input/output, gpadc in
PA14	In/Out	44	/	Programmable input/output, gpadc in
PA15	In/Out	43	/	Programmable input/output, gpadc in
PA16	In/Out	42	/	Programmable input/output, gpadc in
PA19	In/Out	31	25	Programmable input/output, wakeup io
PA20	In/Out	30	24	Programmable input/output, wakeup io
PA21	In/Out	29	23	Programmable input/output, wakeup io
PA22	In/Out	28	22	Programmable input/output, wakeup io
PA23	In/Out	27	21	Programmable input/output, test strap pin/wakeup .
PB00	In/Out	3	3	Programmable input/output
PB01	In/Out	4	4	Programmable input/output
PB02	In/Out	13	13	Programmable input/output
PB03	In/Out	11	11	Programmable input/output
PB04	In/Out	9	9	Programmable input/output
PB05	In/Out	12	12	Programmable input/output
PB06	In/Out	14	14	Programmable input/output
PB07	In/Out	10	10	Programmable input/output
PB16	In/Out	15	/	Programmable input/output
PB17	In/Out	16	/	Programmable input/output
PB18	In/Out	17	/	Programmable input/output
ANT	Analog	52	40	RF Antenna
LOUTP	Output	18	15	Codec DAC output p
MICP	Input	25	19	Codec ADC input p
MICN	Input	24	18	Codec ADC input n
LINEP	Input	22	/	Codec line-in input p
LINEN	Input	21	/	Codec line-in input n

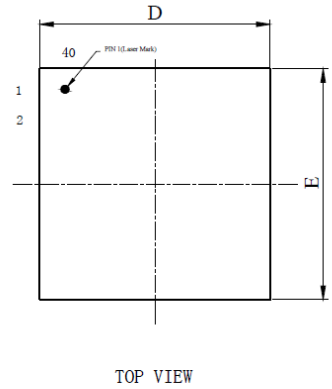
4.3 Package Information

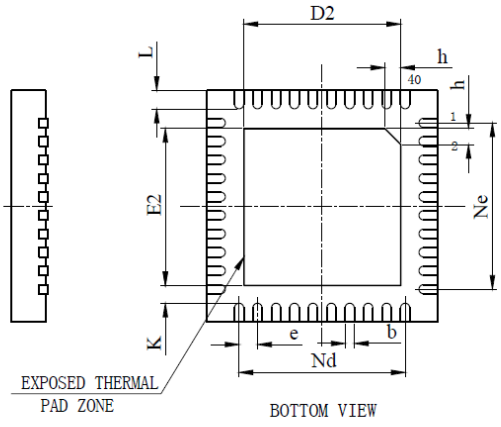




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Figure 4-3 QFN52 Package Outline Drawing





SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.80	0.85	0.90	3
	0.85	0.90	0.95	4
A1	—	0.02	0.05	
b	0.15	0.20	0.25	
c	0.18	0.20	0.25	
D	4.90	5.00	5.10	
D2	3.30	3.40	3.50	
e	0.40BSC			
Nd	3.60BSC			
E	4.90	5.00	5.10	
E2	3.30	3.40	3.50	
Ne	3.60BSC			
L	0.35	0.40	0.45	
K	0.20	--	--	
h	0.30	0.35	0.40	
L/F载体尺寸 (mil)	150*150			

Figure 4-4 QFN40 Package Outline Drawing

4.4 Package Thermal Characteristics

Table 4-2 QFN52 Package Thermal Characteristics

Symbol	Parameter	Conditions	Typ.	Unit
Θ_{JA}	Junction-to-Ambient	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	TBD	°C /W
Θ_{JB}	Junction-to-Board	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	TBD	°C /W
Θ_{JC}	Junction-to-Case	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	TBD	°C /W

Table 4-3 QFN40 Package Thermal Characteristics

Symbol	Parameter	Conditions	Typ.	Unit
Θ_{JA}	Junction-to-Ambient	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	28	°C /W
Θ_{JB}	Junction-to-Board	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	8.5	°C /W
Θ_{JC}	Junction-to-Case	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	9.2	°C /W

5 Carrier Information

TBD

6 Application Circuit

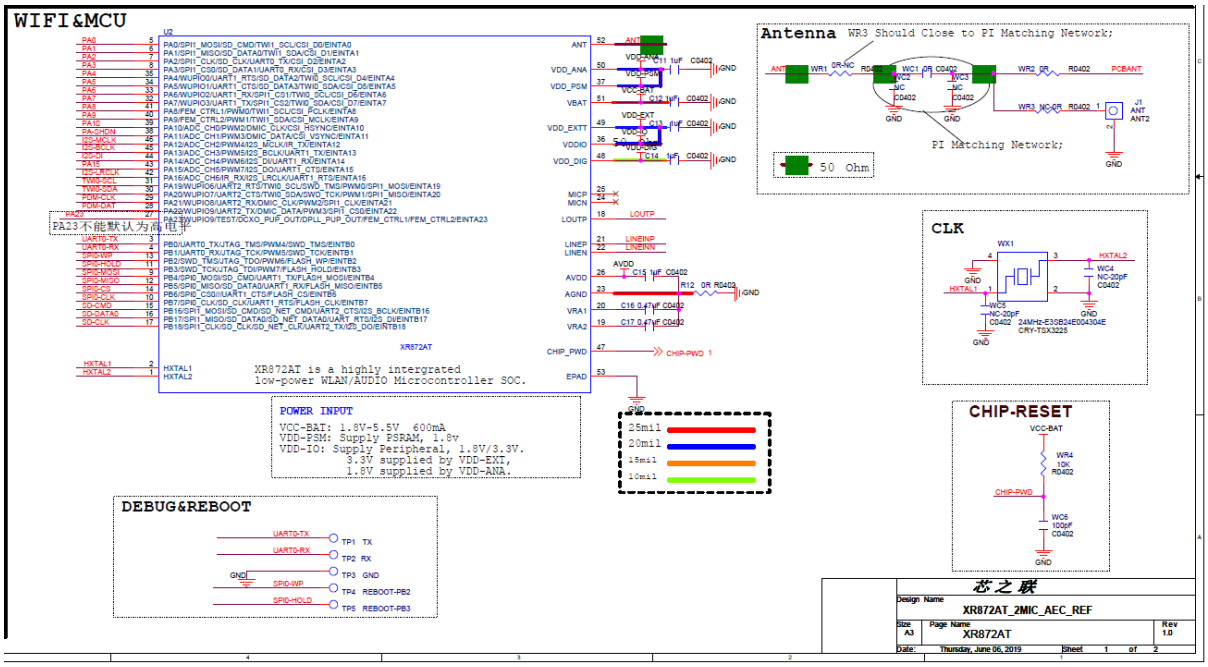


Figure 6-1 Reference Design of XR872AT