

Features

- 16 constant-current output channels
- Constant output current range :
0.5 ~ 35mA@VDD=5V
0.5 ~ 25mA@VDD=3.3V
- Excellent output current accuracy:
Between channels : $\pm 2.0\%$ (max.)
Between ICs : $\pm 3.0\%$ (max.)
- Fast response of output current,OE(min.):40ns
- I/O: Schmitt trigger input
- Data transfer frequency: $f_{MAX}=30\text{MHz}$ (Max)
- 3.3V-5V supply voltage
- Operating Temperature: -40°C to $+85^{\circ}\text{C}$
- Adjustable Pre-Charge for Ghosting Reduction
- LED Protection Circuit
- Enhanced Circuit for Caterpillar Cancelling
- Low-Gray Scale Enhancement
- Integrated Dual Latches for higher refresh rate
- Dim line at the first scan line

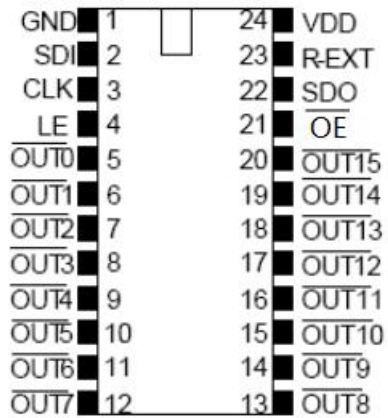
Description

The RUL6024V6 is a 16-channel constant current sink output LED driver. All 16-channels constant current can be set by a single external resistor, which provides users flexibility in controlling the light intensity of LEDs.

The RUL6024V6 exploits current precision controlling technology, which makes error between ICs less than $\pm 2.0\%$, and error between channels less than $\pm 2.0\%$. At RUL6024V6 output stage, 16-regulated output ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of forward voltage(VF) variations.

RUL6024V6 contains two 16-bit shift registers and latches which convert serial input data into parallel output format. For integrated dual latches,RUL6024V6 could get higher refresh rate.

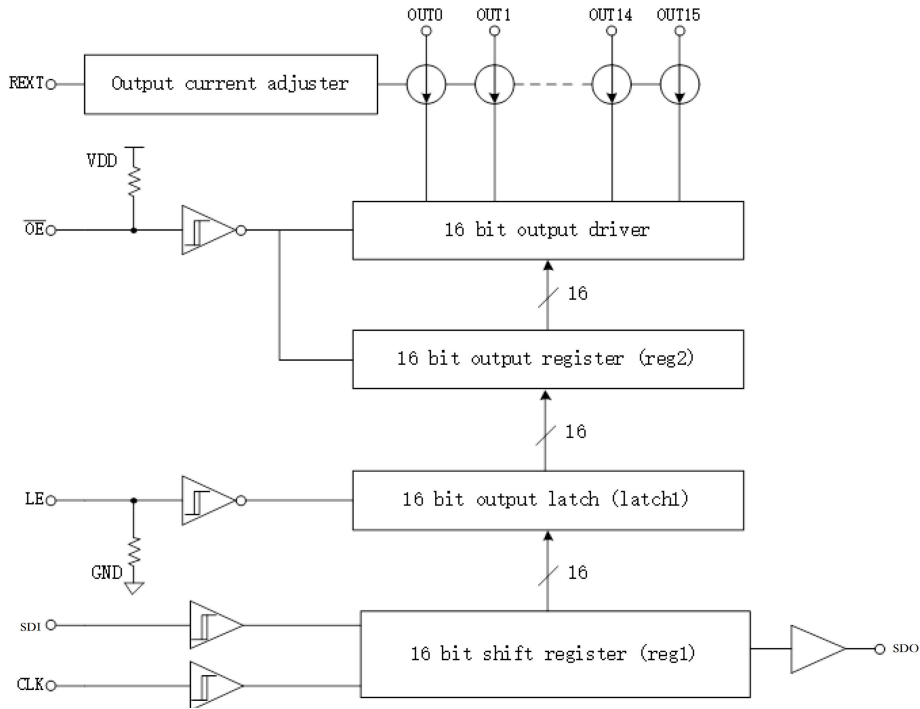
Pin Configuration



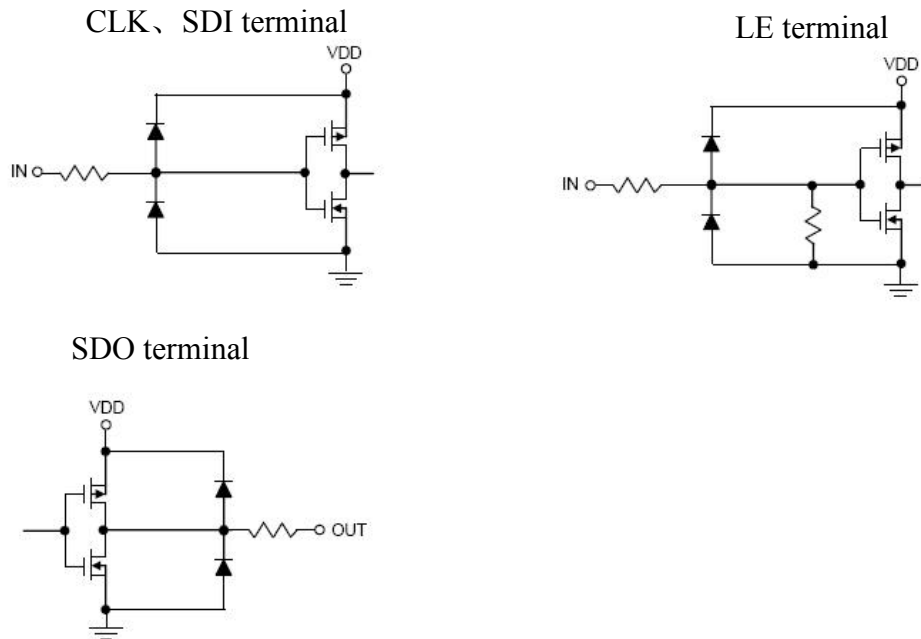
SSOP24

SSOP24	管脚名称	管脚描述
1	GND	Power Ground
2	SDI	Serial data or command input for driver control
3	CLK	Clock input terminal for data shift on rising edge
4	LE	The command parser is a counter of LE length: A different length of LE indicates a different command.
5-20	OUT0 ~ OUT15	Constant current output
21	OE	Output enable terminal, OE high level, all output drivers are enabled; OE low level, all output drivers are turned OFF
22	SDO	Serial-data or command output to the following IC.
23	R-EXT	Constant-current value setting .Connection to an external resistor to GND.
24	VDD	Power-supply voltage

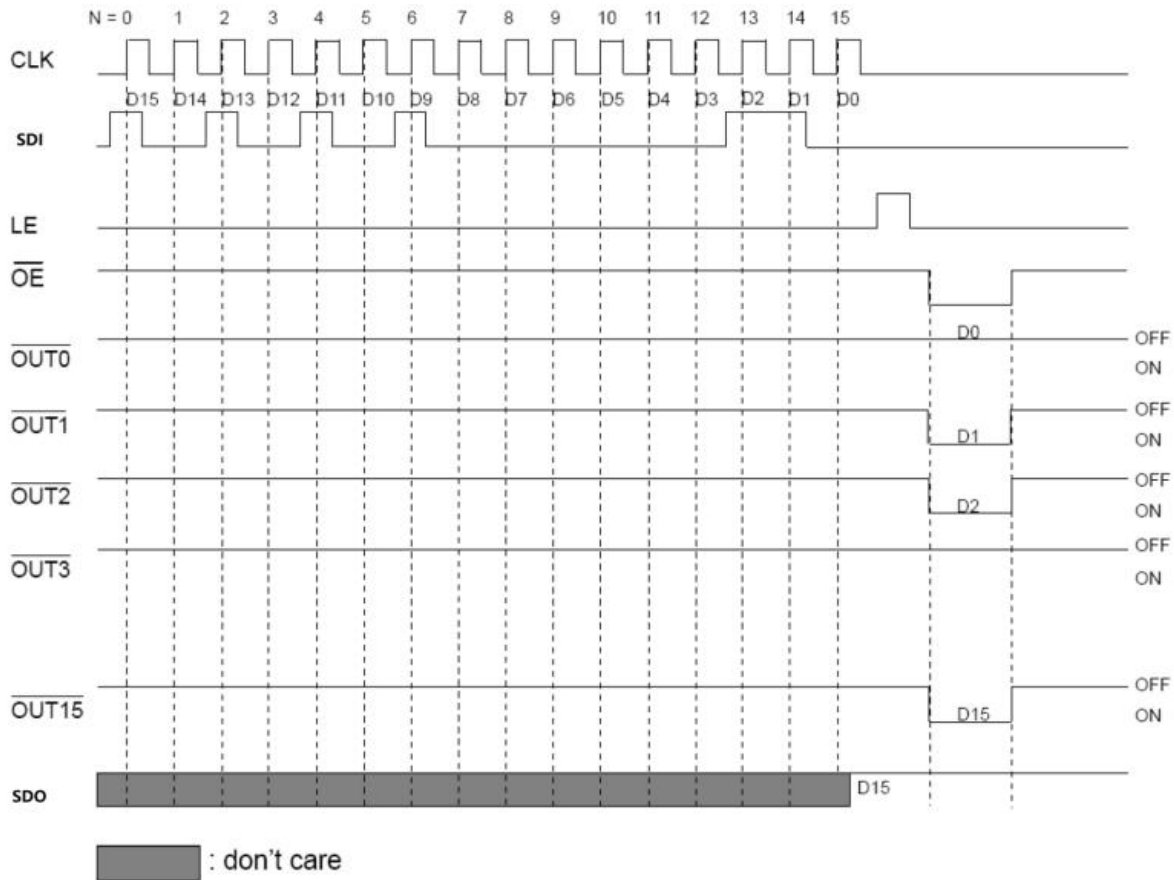
Block Diagram



I/O Equivalent Circuits

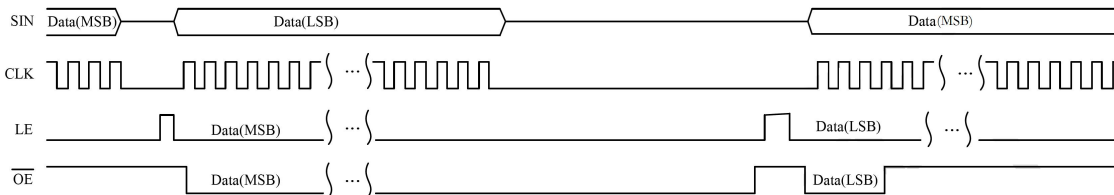


Timing Diagram



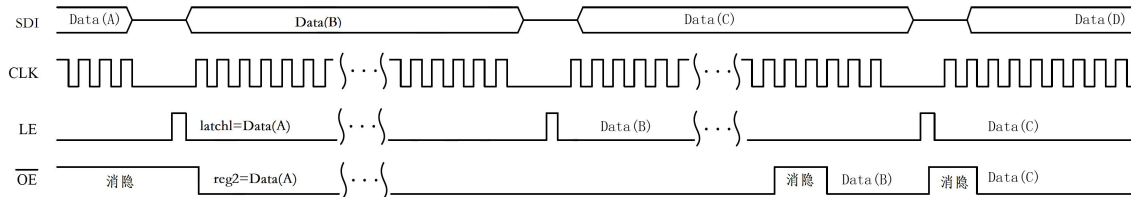
Dual Latch for higher refresh rate

Usual constant current LED sink driver timing diagrams



1. When display a high bit data, display time may far longer than data transfer time, next data transfer should wait display over.
2. When display a low bit data, display time may far shorter than data transfer time, next display should wait data transfer over.

RUL6024V6 dual latch timing diagrams



RUL6024V6 dual latch timing diagrams, data (A) and data (C) are high bit data, data (B) and data (D) are high bit data. Use the free time of display to transfer date could get higher refresh rate.

1. After data(A) transfer over, LE provide a latch signal, latch data(A)
2. After data(A) latched, OE from 1 to 0, display data(A)
3. When display data(A), transfer data(B)
4. After data(B) transfer over, LE provide a latch signal, latch data(B), then transfer data(C)
5. After data(A) displayed, latch data(B) and display data(B)
6. After data(A) transfer over, finish display data(B)
7. Latch data(C) and transfer data(D)

Truth Table

CLK	LE	OE	SDI	OUT0 ... OUT7 ... OUT15	SDO
	H	L	Dn	Dn ... Dn -7 ... Dn -15	Dn-15
	L	L	Dn+1	No Change	Dn-14
	H	L	Dn+2	Dn + 2 ... Dn -5 ... Dn -13	Dn-13
	X	L	Dn+3	Dn + 2 ... Dn -5 ... Dn -13	Dn-13
	X	H	Dn+3	Off	Dn-13

Maximum Ratings (T_a=25°C)

Characteristics		Symbol	Rating	Unit
Supply Voltage		V _{DD}	0 -7.0	V
Input Voltage (SDI,CLK,LE,GCLK)		V _{IN}	-0.4-V _{DD} +0.4	V
Output Current		I _{OUT}	+22	mA
Output voltage		V _{DS}	-0.5 ~ +5.0	V
Clock Frequency		F _{CLK}	30	MHz
GND Terminal Current		I _{GND}	360	mA
Power Dissipation (On PCB, 25°C)	QFN	P _D	2.1	W
	SSOP		1.7	
Thermal Resistance (On PCB, 25°C)	QFN	R _{th(j-a)}	60	°C/W
	SSOP		72	
Operating Temperature		T _{opr}	-40~+85	°C
Storage Temperature		T _{stg}	-55~+150	°C

DC Items (Unless otherwise specified, T_a=-40°C~85°C)

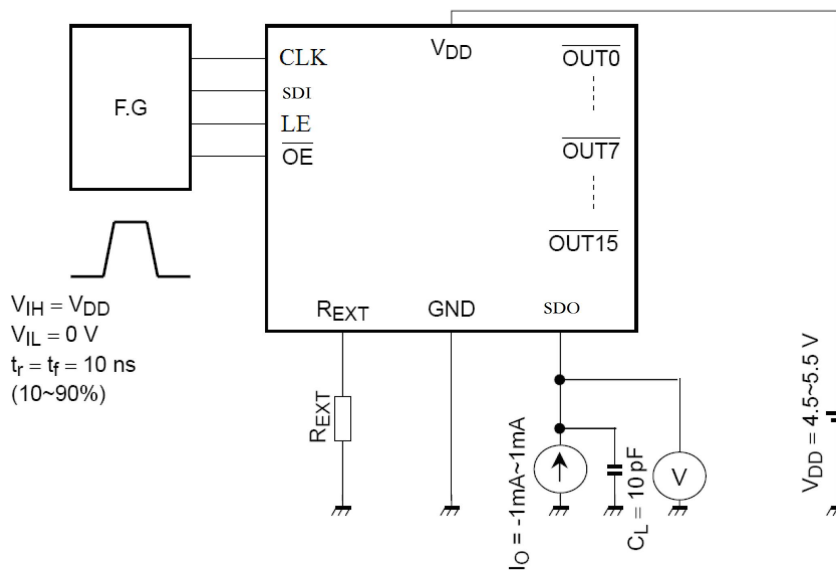
Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit	
Power Supply Voltage	V _{DD}	-	3.0	5.0	6.0	V	
Output Voltage when ON	V _{DS}	OUT0 - OUT15	-	-	5.0	V	
Constant current output	I _{OUT}	OUTn	1	-	45	mA	
SOUT high level output Current	I _{OH}	SDO	-	-	-1.0	mA	
SOUT low level output Current	I _{OL}	SDO	-	-	1.0	mA	
High level logic input voltage	V _{IH}	T _a = -40-85°C	0.7×V _{DD}	-	V _{DD}	V	
Low level logic input voltage	V _{IL}	T _a = -40-85°C	GND	-	0.3×V _{DD}	V	
Low level logic output voltage	V _{OL}	I _{OL} = +1.0mA	-	-	0.3	V	
High level logic output voltage	V _{OH}	I _{OH} = -1.0mA	4.7	-	-	V	
Pull-up resistor	R _{IN(up)}	OE	250	300	350	KΩ	
Pull-down resistor	R _{IN(down)}	LE	250	300	350	KΩ	
Power supply current	"OFF"	I _{DD(off) 1}	Set =NC , OUT0 - OUT15 = Off	-	0.7	0.9	mA
		I _{DD(off) 2}	Set =750Ω , OUT0 - OUT15 =off	-	4	5	
		I _{DD(off) 3}	Set =390Ω , OUT0 - OUT15 =off	-	6.8	8.5	
	"ON"	I _{DD(on) 1}	Set =750Ω , OUT0 - OUT15 =0n	-	4.3	5.4	
		I _{DD(on) 2}	Set =390Ω , OUT0 - OUT15 =0n	-	7.3	9.1	

Electrical Characteristics

Characteristics		Symbol	Test Conditions	Min	Typ	Max	Unit		
Delay Time (Low to High)	CLK - OUTn	t_{pLH1}	VDD=5.0 V VDS=0.8 V VIH=VDD VIL=GND Set =910 Ω VL=4.0 V RL=150 Ω CL=10 pF	-	120	150	ns		
	LE - OUTn	t_{pLH2}		-	120	150	ns		
	OE - OUTn	t_{pLH3}		-	120	150	ns		
	CLK - SDO	t_{pLH}		15	20	-	ns		
Delay Time (High to Low)	CLK - OUTn	t_{pHL1}		VDD=5.0 V VDS=0.8 V VIH=VDD VIL=GND Set =910 Ω VL=4.0 V RL=150 Ω CL=10 pF	-	90	110	ns	
	LE - OUTn	t_{pHL2}			-	90	110	ns	
	OE - OUTn	t_{pHL3}			-	90	110	ns	
	CLK - SDO	t_{pHL}			15	20	-	ns	
Pulse Width	CLK	$t_{w(CLK)}$			VDD=5.0 V VDS=0.8 V VIH=VDD VIL=GND Set =910 Ω VL=4.0 V RL=150 Ω CL=10 pF	20	-	-	ns
	LE	$t_{w(L)}$				20	-	-	ns
	OE	$t_{w(OE)}$				300	-	-	ns
Latch Hold Time	$t_{h(L)}$					VDD=5.0 V VDS=0.8 V VIH=VDD VIL=GND Set =910 Ω VL=4.0 V RL=150 Ω CL=10 pF	5	-	-
Latch Setup Time	$t_{su(L)}$		5				-	-	ns
Maximum clock rise time	t_r^{**}		-				-	500	ns
Maximum clock fall time	t_f^{**}		-				-	500	ns

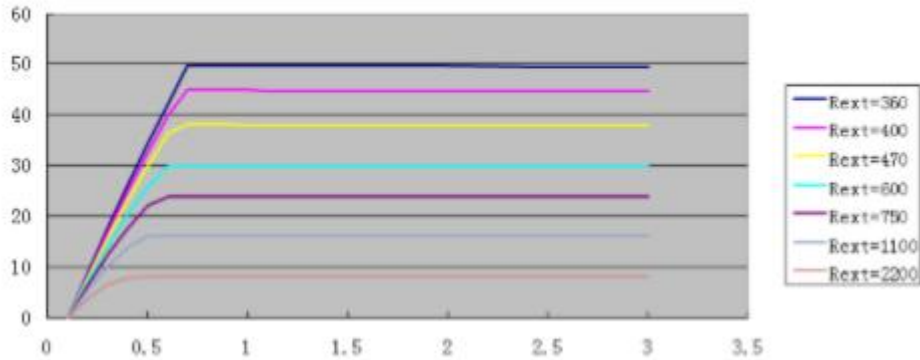
Test Circuit

Test Circuit1: High level logic input voltage/Low level logic input voltage



Application Information

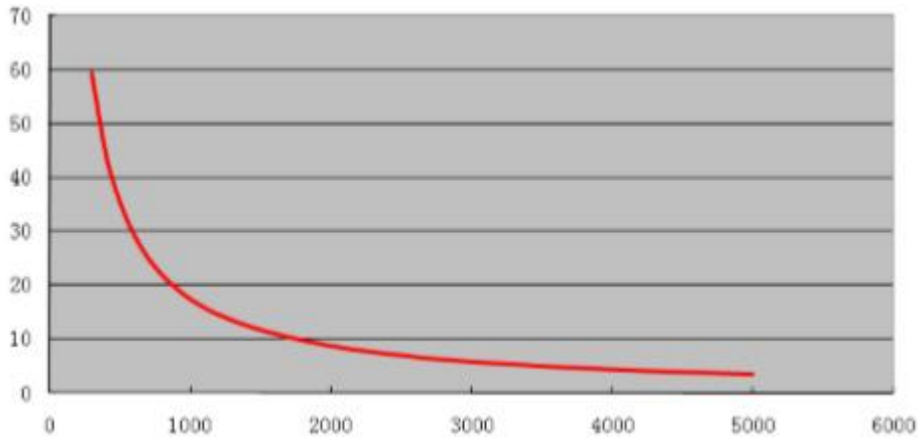
RUL6024V6 exploits current precision controlling technology, and provides nearly no current variations from channel to channel and from IC to IC. 1) The maximum current variation between channels is less than $\pm 2.0\%$, and that between ICs $< \pm 2.0\%$. 2) The current characteristic of output stage is flat, and can be kept constant regardless of the variations of LED forward voltage.



Setting Output Current

The output current (Iout) of RUL6024V6 is set by an external resistor, Rext. The relationship between Iout and Rext is

$$I_{out} = (V_{R-EXT} / R_{ext}) * 15 \quad (\text{Gain}=100\%) \quad V_{R-EXT} = 1.24V;$$

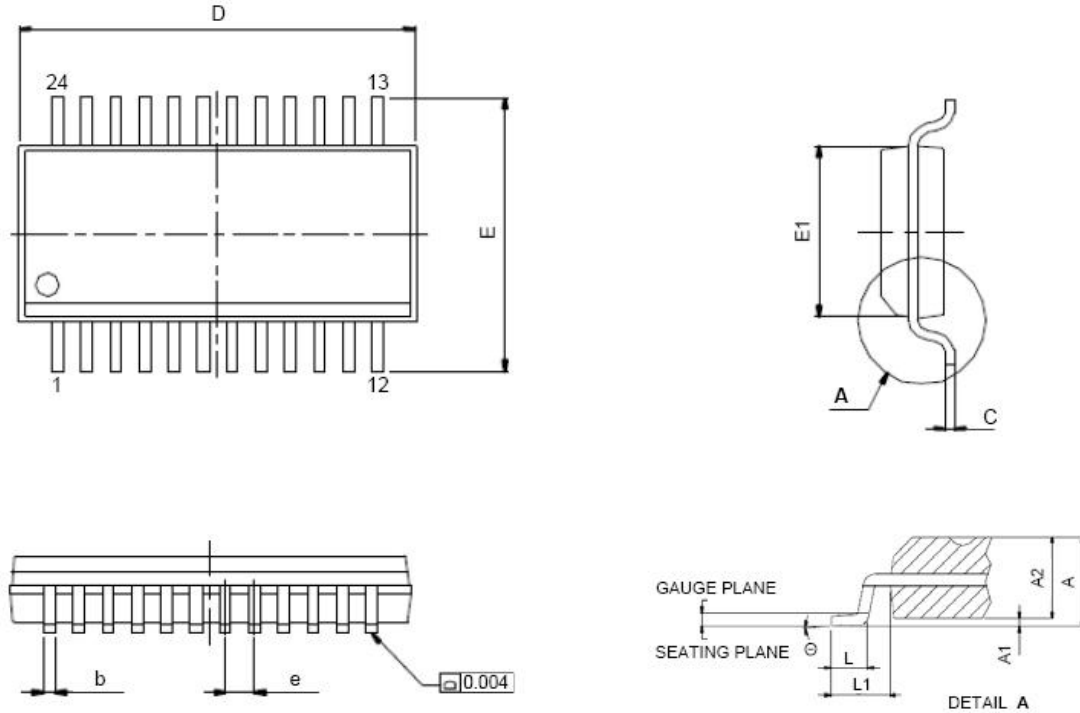


Ordering and Marking InformationNOTE:

Device	Marking	Package	Packaging	Quantity	Reel Size	Tape Width
RUL6024	RUL6024V6	SSOP24	Tape&Reel	4000	13"	12mm

Package Outline

RUL6024V6-SSOP24-0.635mm



Symbol	Dimensions In Inches		Dimensions In millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.346	1.753
A1	0.004	0.010	0.102	0.254
A2	-	0.059	-	1.499
b	0.008	0.012	0.203	0.305
C	0.007	0.010	0.178	0.254
D	0.337	0.344	8.560	8.738
E	0.228	0.244	5.791	6.198
E1	0.150	0.157	3.810	3.988
e	0.025TYP.		0.635TYP.	
L	0.016	0.050	0.406	1.270
L1	0.041TYP.		1.041TYP.	
θ	0°	8°	0°	8°

NOTE:

1: ALL UNITS ARE IN MILLIMETER.

2: EJECTOR PIN MARK POSITION MAY VARY FROM DIFFERENT MOLD.

3: ALL DIMENSIONS REFER TO JEDEC.DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

