**Laurel Electronics Co., Ltd.**

# LCD Module Specification

## Model No.: LG192962-FFDWH6V-V33

Table of Contents



**RECORD OF REVISION**

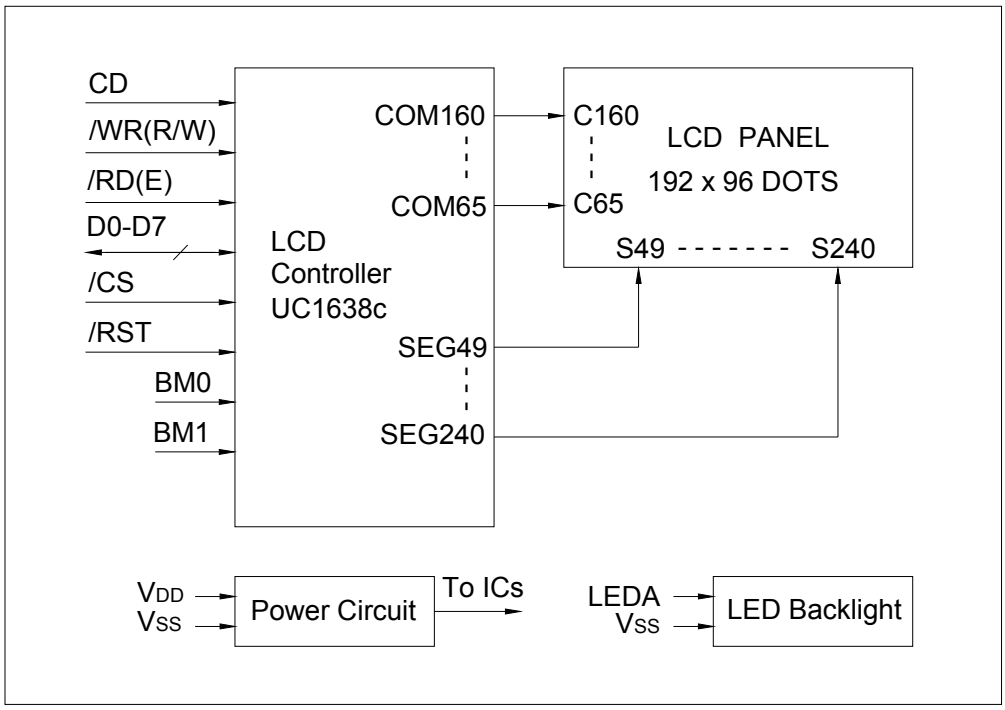
| Rev. | Date | Page | Item | Description |
|---|---|---|---|---|
| 0.1 | 2016/08/05 | - | - | New release |
| | | | | |

# *1. BASIC SPECIFICATIONS*

## 1.1 Features

| Item | Specifications | Unit |
|---|---|---|
| Display Format | 192 x 96 | dot |
| LCD Type | FSTN - Positive - Transflective<br>Black characters on white background | - |
| Driving Method | 1/96 Duty, 1/11 Bias | - |
| Viewing Direction | 6 | O'clock |
| Backlight & Color | LED, white color | - |
| Outline Dimension (WxHxT) | 87.0 x 57.0 x 9.5 | mm |
| Viewing Area (WxH) | 70.0 x 37.0 | mm |
| Active Area (WxH) | 65.26 x 32.62 | mm |
| Dot Pitch (WxH) | 0.34 x 0.34 | mm |
| Dot Size (WxH) | 0.32 x 0.32 | mm |
| Weight | 42 | g |
| Controller | UC1638c (COG) | - |
| Interface | 8080/6800 8-bit parallel, 4/3-wire SPI and $I^2C$ | - |
| Power Supply ($V_{DD}$) | 3.0 to 3.6 | V |

## 1.2 Block Diagram



## 1.3 Terminal Functions (CN1: Thru-holes; CN2: FFC)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Level</th><th>Function</th></tr>
<tr><td>1</td><td>VSS</td><td>0V</td><td>Ground</td></tr>
<tr><td>2</td><td>VDD</td><td>3V to 3.6V</td><td>Power supply for logic</td></tr>
<tr><td>3</td><td>LEDA</td><td>3.3V</td><td>Power supply for LED backlight.<br>LEDK is connected to Vss on PCB.<br>Refer to section 3.8 to 3.9</td></tr>
<tr><td>4</td><td>CD</td><td>H/L</td><td>Data or instruction selection<br>“L”: D0 to D7 are Instruction code “H”: D0 to D7 are display data<br>In S9 or I$^2$C mode, CD is not used, connect it to VSS.</td></tr>
<tr><td>5</td><td>/CS</td><td>L</td><td>Chip selection signal. Active “L”.</td></tr>
<tr><td>6</td><td>/RST</td><td>L</td><td>Reset signal. Active “L”.</td></tr>
<tr><td>7</td><td>D0</td><td rowspan="8">H/L</td><td rowspan="8">Bi-directional bus for both serial and parallel host interfaces.<br>In serial modes, connect D0 to SCK, D3 to SDAI for write and D[5:4] to SDAO for read. SDI and SDO may be connected together if necessary.
<table>
<tr><td></td><td>BM[1:0]=1x<br>8-bit parallel</td><td>BM[1:0]=00<br>S8</td><td>BM[1:0]=01<br>S9</td><td>BM[1:0]=00<br>I$^2$C</td></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td><td>SCK</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>D2</td><td>D2</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D3</td><td>D3</td><td>SDAI</td><td>SDAI</td><td>SDAI</td></tr>
<tr><td>D4</td><td>D4</td><td>SDAO</td><td>SDAO</td><td>SDAO</td></tr>
<tr><td>D5</td><td>D5</td><td>SDAO</td><td>SDAO</td><td>SDAO</td></tr>
<tr><td>D6</td><td>D6</td><td>ACK*</td><td>ACK*</td><td>–</td></tr>
<tr><td>D7</td><td>D7</td><td>ACK*</td><td>ACK*</td><td>–</td></tr>
</table>
Connect unused pins to VSS.<br>*Acknowledgement, leave it open if not used</td></tr>
<tr><td>8</td><td>D1</td></tr>
<tr><td>9</td><td>D2</td></tr>
<tr><td>10</td><td>D3</td></tr>
<tr><td>11</td><td>D4</td></tr>
<tr><td>12</td><td>D5</td></tr>
<tr><td>13</td><td>D6</td></tr>
<tr><td>14</td><td>D7</td></tr>
<tr><td>15</td><td>/WR<br>(R/W)</td><td>H/L</td><td>/WR signal for 8080 series MPU. Write data at rising edge of /WR.<br>R/W signal for 6800 series MPU. R/W=“H”: Read; R/W=“L”: Write.<br>In serial modes, /WR(R/W) is not used, connect it to VSS or keep it open.</td></tr>
<tr><td>16</td><td>/RD<br>(E)</td><td>H/L</td><td>/RD signal for 8080 series MPU. Read data when /RD is “L”.<br>Enable signal for 6800 series MPU. Read data when E is “H”, write data at falling edge of E.<br>In serial modes, /RD(E) is not used, connect it to VSS or keep it open.</td></tr>
<tr><td>17-20</td><td>NC</td><td>-</td><td>No connection</td></tr>
</table>

Note: /WR(R/W) and /RD(E) signals are pulled to VSS by on-board 100KΩ resistors. These terminals can be kept open in serial interface mode.

### 1.4 Set Bus Mode by on Board Jumpers and D1

The interface bus mode is determined by BM[1:0] and D1 levels. The relationship between jumper status, BM[1:0] level, D1 level and interface bus mode is below.

| Jumper Status (C=Close; O=Open) | | | | | | | BM[1:0] Level | D1 Level | Interface Bus Mode |
|---|---|---|---|---|---|---|---|---|---|
| J2 | J3 | J4 | J5 | J6 | J7 | J8 | | | |
| O | O | O | O | C | C | O | 10 | - | 8080 8-bit **<Default>** |
| O | O | O | C | O | C | O | 11 | - | 6800 8-bit |
| O | O | O | O | C | O | C | 00 | 0 | 4-wire SPI (S8) |
| O | O | O | C | O | O | C | 01 | 1 | 3-wire SPI (S9) |
| O | O | O | O | C | O | C | 00 | 1 | 2-wire SPI ($I^2C$) |

## *2. ABSOLUTE MAXIMUM RATINGS*

| Item | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply Voltage (Logic) | VDD | -0.3 | 4.0 | V |
| LCD Generated Voltage | VLCD | -0.3 | 19.8 | V |
| Input Voltage | VIN | -0.4 | VDD+0.5 | V |
| Operating Temperature | Topr | -20 | +70 | °C |
| Storage Temperature | Tstg | -30 | +80 | °C |

Cautions: Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## *3. ELECTRICAL CHARACTERISTICS*

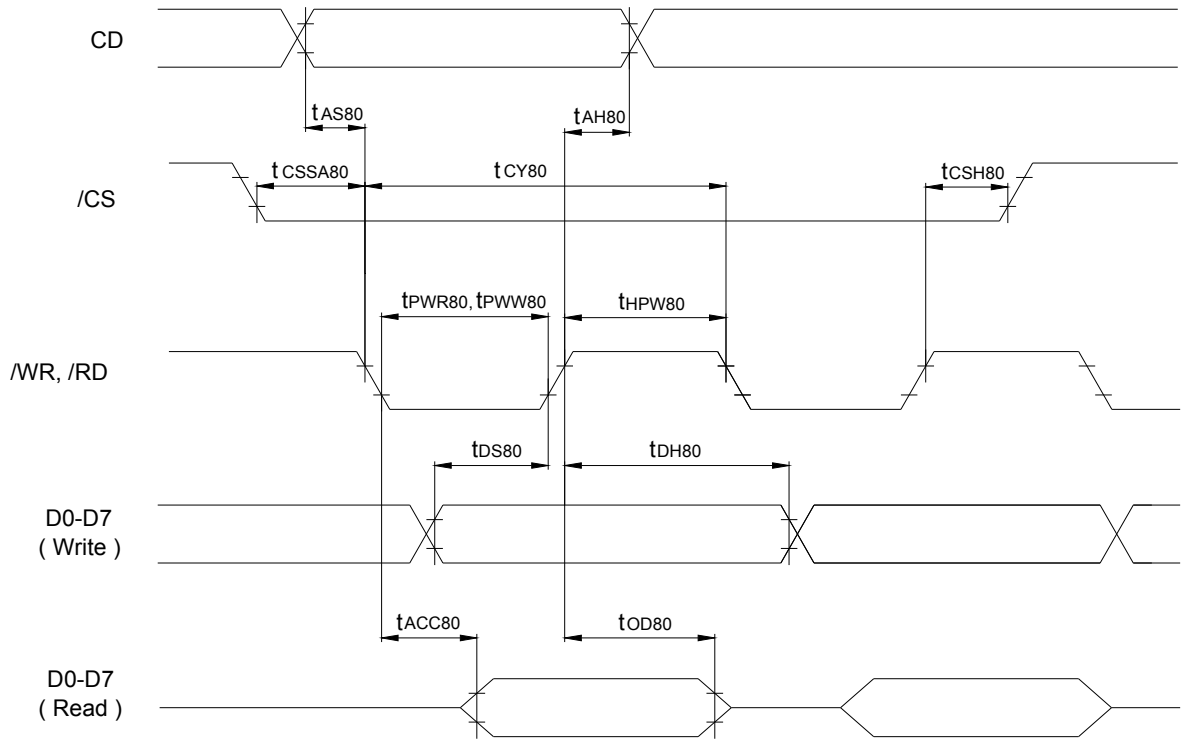
### 3.1 DC Characteristics (Ta=25°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage (Logic) | VDD | | 3.0 | 3.3 | 3.6 | V |
| Charge Pump Output Voltage | VLCD | | - | 13.5 | - | V |
| Input Low Voltage | VIL | | 0 | - | 0.2VDD | V |
| Input High Voltage | VIH | | 0.8VDD | - | VDD | V |
| Output Low Voltage | VOL | | 0 | - | 0.2VDD | V |
| Output High Voltage | VOH | | 0.8VDD | - | VDD | V |
| Supply Current (B/W mode) | IDD | VDD=3.3V VLCD=13.5V | - | 0.9 | 1.4 | mA |

## 3.2 Parallel Bus Timing Characteristics (8080 Series MPU, VDD=3.0V to 3.6V, Ta=25°C)

| Description | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Address setup time<br>Address hold time | CD | $t_{AS80}$<br>$t_{AH80}$ | | 15<br>20 | - | ns |
| Chip select setup time<br>Chip select hold time | /CS | $t_{CSSA80}$<br>$t_{CSH80}$ | | 5<br>5 | - | |
| System cycle time (read)<br>(write) | /WR<br>/RD | $t_{CY80}$ | | 430<br>280 | - | |
| Low pulse width (read)<br>(write) | | $t_{PWR80}$<br>$t_{PWW80}$ | | 200<br>125 | - | |
| High pulse width (read)<br>(write) | | $t_{HPW80}$ | | 200<br>125 | - | |
| Data setup time<br>Data hold time | D0 to D7 | $t_{DS80}$<br>$t_{DH80}$ | | 45<br>10 | - | |
| Read access time<br>Output disable time | | $t_{ACC80}$<br>$t_{OD80}$ | CL=100pF | -<br>100 | 200<br>- | |

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

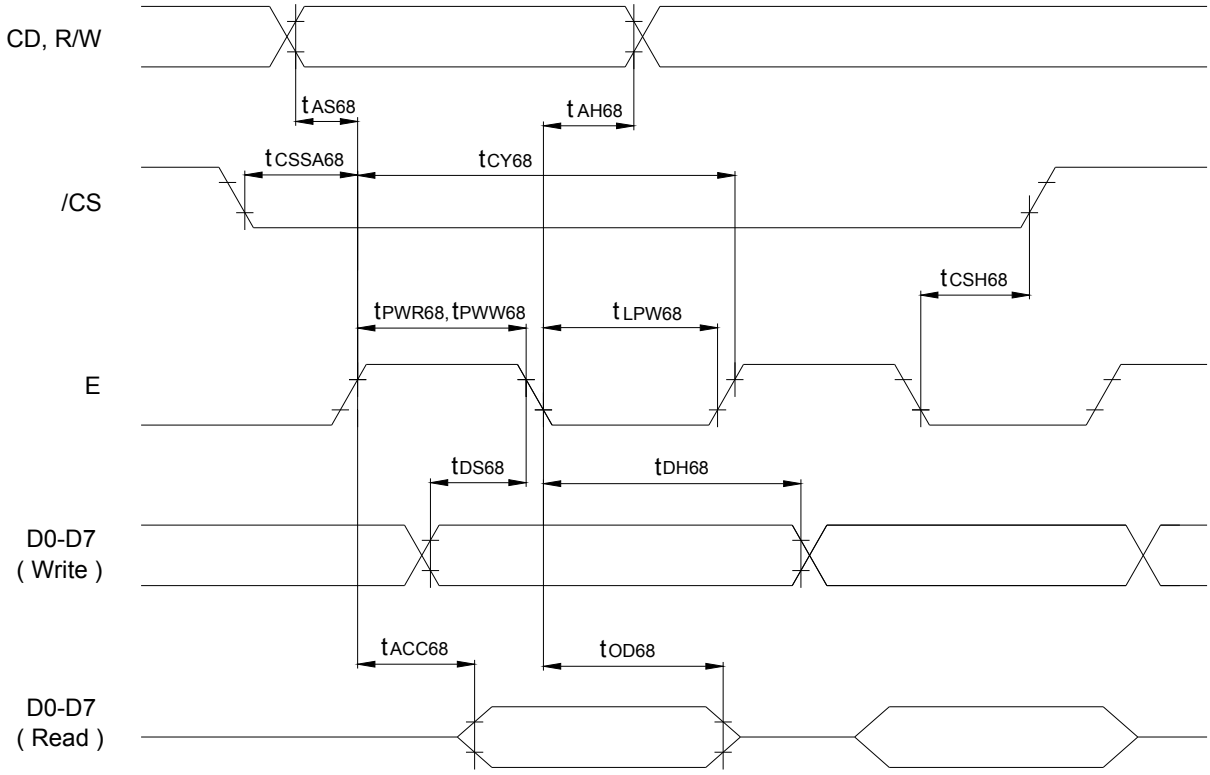



Parallel Bus Timing Characteristics (for 8080 MPU)

## 3.3 Parallel Bus Timing Characteristics (6800 Series MPU, VDD=3.0V to 3.6V, Ta=25°C)

| Description | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Address setup time<br>Address hold time | CD<br>R/W | $t_{AS68}$<br>$t_{AH68}$ | | 15<br>20 | - | ns |
| Chip select setup time<br>Chip select hold time | /CS | $t_{CSSA68}$<br>$t_{CSH68}$ | | 5<br>5 | - | |
| System cycle time (read)<br>(write) | E | $t_{CY68}$ | | 430<br>280 | - | |
| Pulse width (read) | | $t_{PWR68}$ | | 200 | - | |
| Pulse width (write) | | $t_{PWW68}$ | | 125 | - | |
| Low pulse width (read)<br>(write) | | $t_{LPW68}$ | | 200<br>125 | - | |
| Data setup time<br>Data hold time | D0 to D7 | $t_{DS68}$<br>$t_{DH68}$ | | 45<br>10 | - | |
| Read access time<br>Output disable time | | $t_{ACC68}$<br>$t_{OD68}$ | CL=100pF | -<br>100 | 200<br>- | |

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

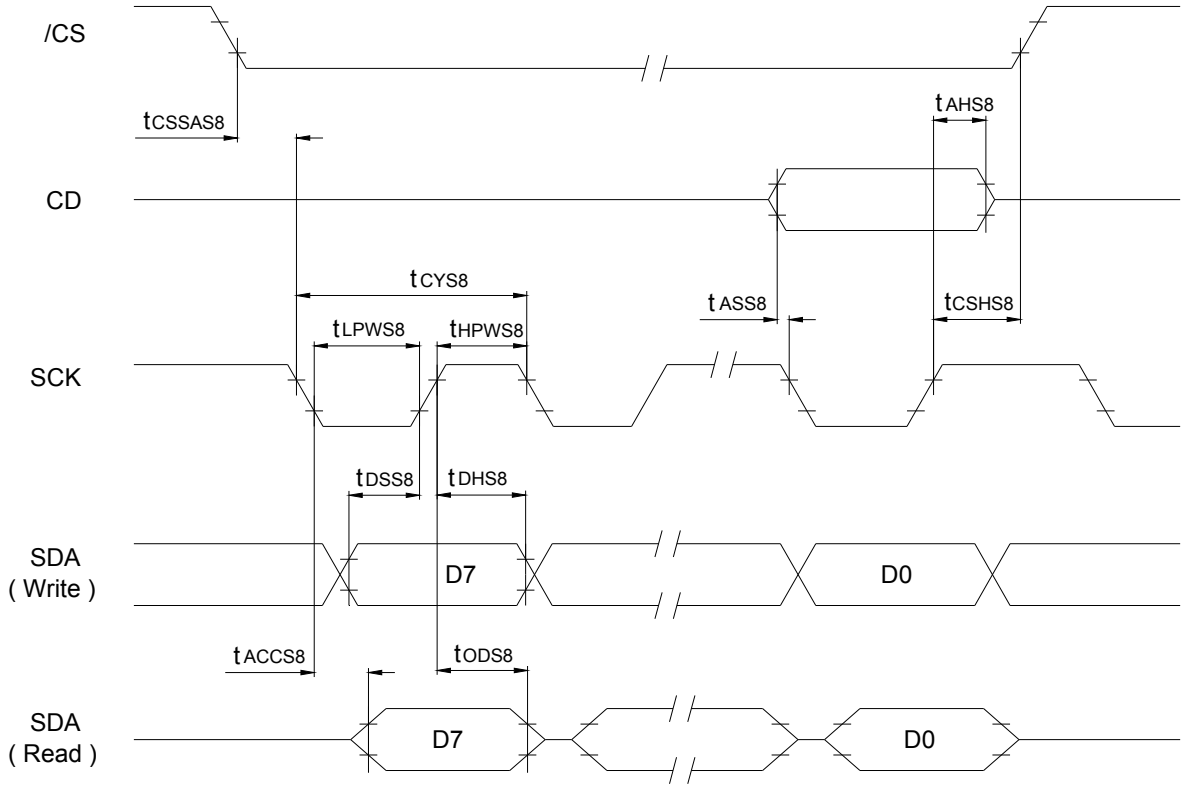



Parallel Bus Timing Characteristics (for 6800 MPU)

## 3.4 Serial Bus Timing Characteristics (S8 Mode, VDD=3.0V to 3.6V, Ta=25°C)

| Description | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Address setup time | CD | $t_{ASS8}$ | | 0 | - | ns |
| Address hold time | | $t_{AHS8}$ | | 15 | - | |
| Chip select setup time<br>Chip select hold time | /CS | $t_{CSSAS8}$<br>$t_{CSHS8}$ | | 5<br>15 | - | |
| System cycle time (read)<br>(write) | SCK | $t_{CYS8}$ | | 430<br>220 | - | |
| Low pulse width (read)<br>(write) | | $t_{LPWS8}$ | | 200<br>95 | - | |
| High pulse width (read)<br>(write) | | $t_{HPWS8}$ | | 200<br>95 | - | |
| Data setup time<br>Data hold time | SDA | $t_{DSS8}$<br>$t_{DHS8}$ | | 25<br>15 | - | |
| Read access time<br>Output disable time | | $t_{ACCS8}$<br>$t_{ODS8}$ | CL=100pF | -<br>30 | 200<br>- | |

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

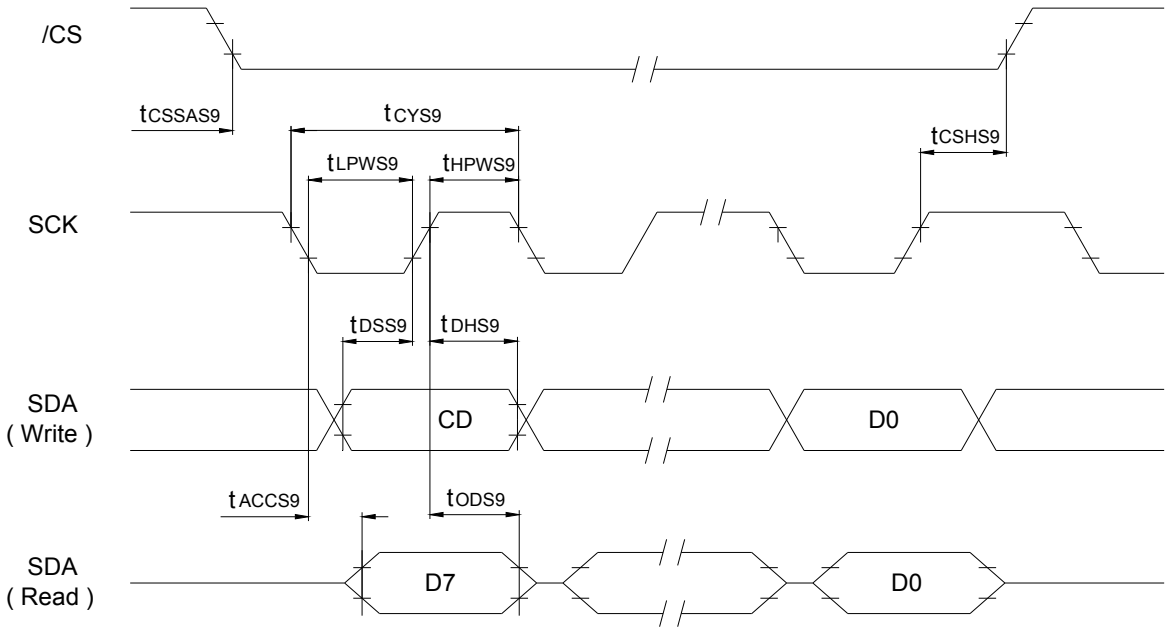



Serial Bus Timing Characteristics (for S8)

## 3.5 Serial Bus Timing Characteristics (S9 Mode, VDD=3.0V to 3.6V, Ta=25°C)

| Description | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Chip select setup time<br>Chip select hold time | /CS | $t_{CSSAS9}$<br>$t_{CSHS9}$ | | 5<br>15 | - | ns |
| System cycle time (read)<br>(write) | SCK | $t_{CYS9}$ | | 430<br>220 | - | |
| Low pulse width (read)<br>(write) | | $t_{LPWS9}$ | | 200<br>95 | - | |
| High pulse width (read)<br>(write) | | $t_{HPWS9}$ | | 200<br>95 | - | |
| Data setup time<br>Data hold time | SDA | $t_{DSS9}$<br>$t_{DHS9}$ | | 25<br>15 | - | |
| Read access time<br>Output disable time | | $t_{ACCS9}$<br>$t_{ODS9}$ | | -<br>30 | 200<br>- | |

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

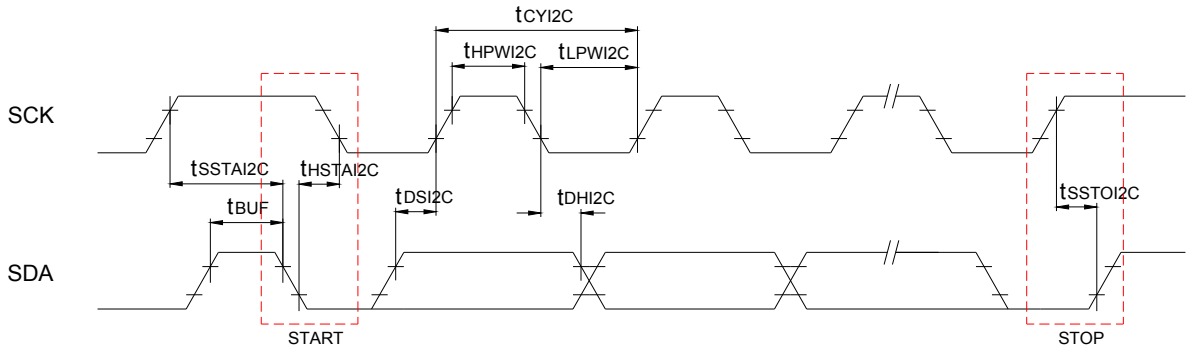



Serial Bus Timing Characteristics (for S9)

## 3.6 Serial Bus Timing Characteristics ($I^2C$ Mode, $V_{DD}$=3.0V to 3.6V, Ta=25°C)

| Description | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCK cycle time (read)<br>(write) | SCK | $t_{CYI2C}$ | | 530<br>230 | - | ns |
| Low pulse width (read)<br>(write) | | $t_{LPWI2C}$ | | 250<br>100 | - | |
| High pulse width (read)<br>(write) | | $t_{HPWI2C}$ | | 250<br>100 | - | |
| Data setup time<br>Data hold time | SCK<br>SDA | $t_{DSI2C}$<br>$t_{DHI2C}$ | | 55<br>10 | - | |
| START setup time<br>START hold time | | $t_{SSTAI2C}$<br>$t_{HSTAI2C}$ | | 10<br>55 | - | |
| STOP setup time | | $t_{SSTOI2C}$ | | 10 | - | |
| Bus free time between STOP and START condition | | $t_{BUF}$ | | 75 | - | |

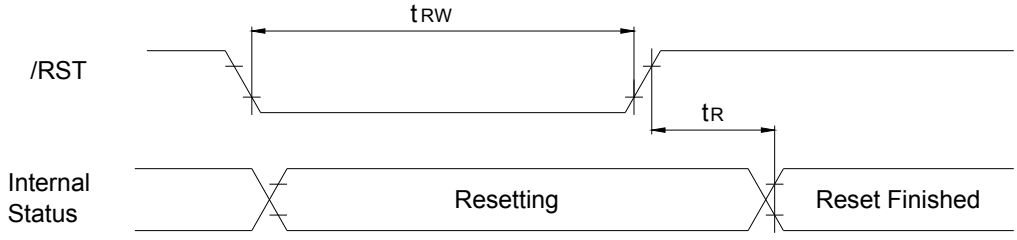
Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.




Serial Bus Timing Characteristics (for $I^2C$)

## 3.7 Reset Characteristics ($V_{DD}$=3.0V to 3.6V, Ta=25°C)

| Description | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Reset low pulse width | /RST | $t_{RW}$ | | 5 | - | ms |
| Reset to internal status pulse delay | /RST | $t_R$ | | 10 | - | us |
| Wait before power down | /RST | | | 1 | - | ms |

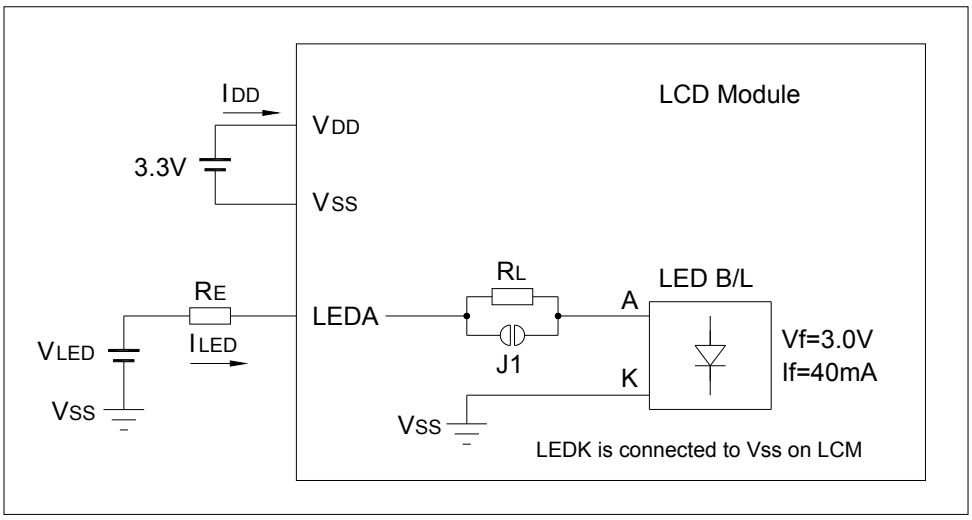



Reset Characteristics

## 3.8 LED Backlight Characteristics (Ta=25°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Forward Voltage | Vf | | 2.9 | 3.0 | 3.2 | V |
| Forward Current | If | Vf=3.0V | - | 40 | - | mA |
| Color | White | | | | | |

## 3.9 Power Supply for Logic and LED Backlight




RL (internal) and RE (external) are the current limiting resistors for LED backlight

| VLED | Jumper Status | RE Value | Remark |
|---|---|---|---|
| 3.3V | J1 open | 0Ω | Default |
| 5V | J1 open | (5V – 3.3V)/40mA=43Ω | - |
| Other voltage | J1 open | (VLED – 3.3V)/40mA | |

# *4. DISPLAY CONTROL COMMANDS*

The following is a list of host commands supported by UC1638c.

C/D=0: Control, C/D=1: Data; W/R=0: Write Cycle, W/R=1: Read Cycle
D7-D0=#: Useful Data Bits, D7-D0=-: Don't Care

| | Command | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Action | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Write Data Byte (multiple-byte command) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write byte by byte | N/A |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| | | : | : | : | : | : | : | : | : | : | : | | |
| 2 | Read Data Byte (multiple-byte command) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Read byte by byte | N/A |
| | | 1 | 1 | # | # | # | # | # | # | # | # | | |
| | | : | : | : | : | : | : | : | : | : | : | | |
| 3 | Get Status (triple-byte command) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Get Status | N/A |
| | | 1 | 1 | POR | MX | MY | PID | DE | WS | MD | MS | | |
| | | 1 | 1 | Ver[1:0] | | PMO[5:0] | | | | | | | |
| 4 | Set Column Address (double-byte command) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Set CA[7:0] | 00H |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 5 | Set Temperature Compensation | 0 | 0 | 0 | 0 | 1 | 0 | 0 | # | # | # | Set TC[2:0] | 100b |
| 6 | Set Pump Control | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | # | Set PC[0] | 1b |
| 7 | Set Adv. Program Control (double-byte command) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | R | R | R | R=0 to 5<br>Set APC[R][7:0] | N/A |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 8 | Set Scroll Line LSB | 0 | 0 | 0 | 1 | 0 | 0 | # | # | # | # | Set SL[3:0] | 0H |
| | Set Scroll Line MSB | 0 | 0 | 0 | 1 | 0 | 1 | # | # | # | # | Set SL[7:4] | 0H |
| 9 | Set Page Address LSB | 0 | 0 | 0 | 1 | 1 | 0 | # | # | # | # | Set PA[3:0] | 0H |
| | Set Page Address MSB | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | # | # | Set PA[5:4] | 0H |
| 10 | Set $V_{BIAS}$ Potentiometer (double-byte command) | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Set PM[7:0] | 54H |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 11 | Set Partial Display Control | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | # | Set LC[8] | 0:Disable |
| 12 | Set COM Scan Function | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | # | Set CSF[0] | 0b |
| 13 | Set RAM Address Control | 0 | 0 | 1 | 0 | 0 | 0 | 1 | # | # | # | Set AC[2:0] | 001b |
| 14 | Set Display mode | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | # | # | Set DC[5:4] | 00b |
| 15 | Set Line Rate | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | # | # | Set LC[3:2] | 10b |
| 16 | Set All-Pixel-ON | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | # | Set DC[1] | 0b |
| 17 | Set Inverse Display | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | # | Set DC[0] | 0b |
| 18 | Set LCD Mapping Control | 0 | 0 | 1 | 1 | 0 | 0 | 0 | # | # | 0 | Set LC[1:0] | 00b |
| 19 | Set N-Line Inversion (double-byte command) | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Set NIV[6:0] | 00H |
| | | 1 | 0 | 0 | # | # | # | # | # | # | # | | |
| 20 | Set Display Enable (double-byte command) | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | Set DC[3:2] | 10b |
| | | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | # | # | | |
| 21 | Set LCD Gray Shade 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | # | # | Set LC[5:4] | 01b |
| 22 | Set LCD Gray Shade 2 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | # | # | Set LC[7:6] | 10b |

## *DISPLAY CONTROL COMMANDS …continued*

| | Command | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Action | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 23 | System Reset (double-byte command) | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | System Reset | N/A |
| | | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | | |
| 24 | NOP | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | No operation | N/A |
| 25 | Set Test Control (double-byte command) | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | TT | | For testing only. Do not use. | N/A |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 26 | Set LCD Bias Ratio | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | # | # | Set BR[1:0] | 11b:12 |
| 27 | Reset Cursor Update Mode | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | AC[4]=0,CA=CR | N/A |
| 28 | Set Cursor Update Mode | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | AC[4]=1.CR=CA | N/A |
| 29 | Set COM End (double-byte command) | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | Set CEN[7:0] | 159 |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 30 | Set Partial Display Start (double-byte command) | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | Set DST[7:0] | 0 |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 31 | Set Partial Display End (double-byte command) | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | Set DEN[7:0] | 159 |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 32 | Set Window Programming Starting Column Address | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | Set WPC0[7:0] | 0 |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 33 | Set Window Programming Starting Page Address | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | Set WPP0[5:0] | 0 |
| | | 1 | 0 | 0 | 0 | # | # | # | # | # | # | | |
| 34 | Set Window Programming Ending Column Address | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | Set WPC1[7:0] | 239 |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 35 | Set Window Programming Ending Page Address | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | Set WPP1[5:0] | 39 |
| | | 1 | 0 | 0 | 0 | # | # | # | # | # | # | | |
| 36 | Enable Window Program | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | # | Set AC[3] | 0:Disable |
| 37 | Set MTP Operation control (double-byte command) | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | Set MTPC[4:0] | 10H |
| | | 1 | 0 | 0 | 0 | 0 | # | # | # | # | # | | |
| 38 | Set MTP Write Mask (double-byte command) | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Set MTPM[5:0] | 00H |
| | | 1 | 0 | 0 | 0 | # | # | # | # | # | # | | |
| 39 | Set MTP Read Potentiometer | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | Set RV[7:0] (BR=00b) | 00H |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 40 | Set MTP Program/Erase Potentiometer | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | Set WV[7:0] (BR=10b) | 46H |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 41 | Set MTP Write Timer (double-byte command) | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Set WT[7:0] | 40H |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |
| 42 | Set MTP Read Timer (double-byte command) | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | Set RT[7:0] | 03H |
| | | 1 | 0 | # | # | # | # | # | # | # | # | | |

Notes:

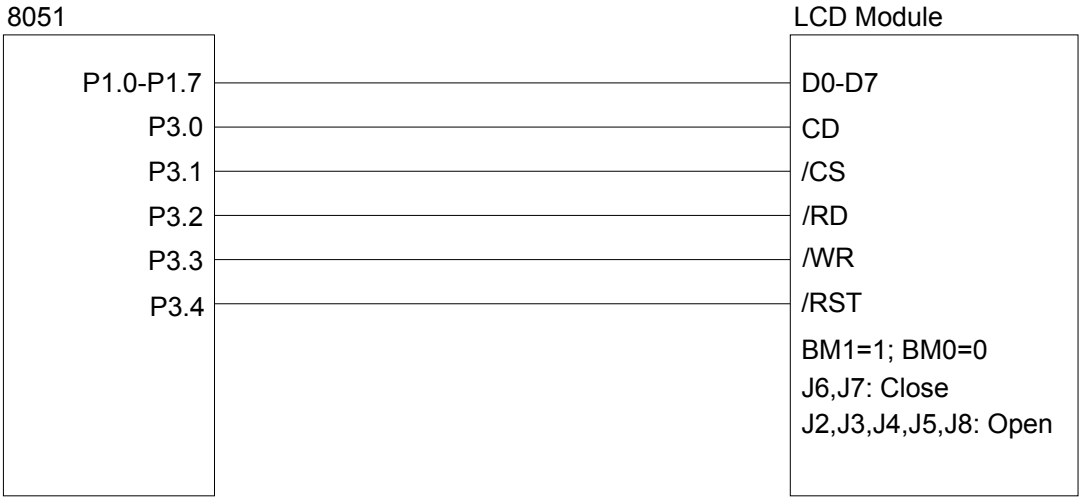
1. Please refer to UC1638c datasheet for details.
2. Any bit patterns other than the commands listed above may result in undefined behavior.
3. MTP function is disabled for this lcm.

## *5. CONNECTION WITH MPU*

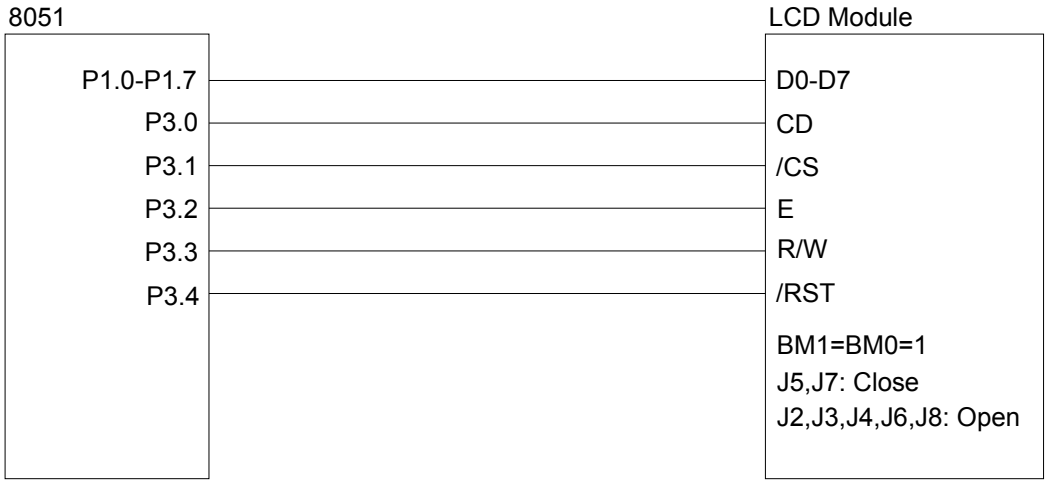
This lcm supports two parallel bus protocols (8080 or 6800 in 8-bit bus width) and three serial bus protocols (4/3-wire SPI and $I^2C$). Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to save the I/O terminals. The interface bus mode is determined by BM[1:0] and D1 by the following relationship.

| Bus type | | 8080 | 6800 | S8(4-wire) | S9(3-wire) | $I^2C$(2-wire) |
|---|---|---|---|---|---|---|
| Width | | 8-bit | 8-bit | Serial | | |
| Access | | Read/Write | | Read(status only)/Write | | Read/Write |
| Control & Data Pins | BM[1:0] | 10 | 11 | 00 | 01 | 00 |
| | /CS(CS0) | Chip Select | | | | A2 |
| | CD | Control/Data | | | | 0 |
| | /WR(R/W) | /WR | R/W | 0 | | |
| | /RD(E) | /RD | E | 0 | | |
| | D[7:6] | Data | Data | ACK | | - |
| | D[5:3] | Data | Data | D5/D4=SDAO, D3=SDAI | | |
| | D[2] | Data | Data | - | | |
| | D[1] | Data | Data | 0 | 1 | 1 |
| | D[0] | Data | Data | SCK | | |

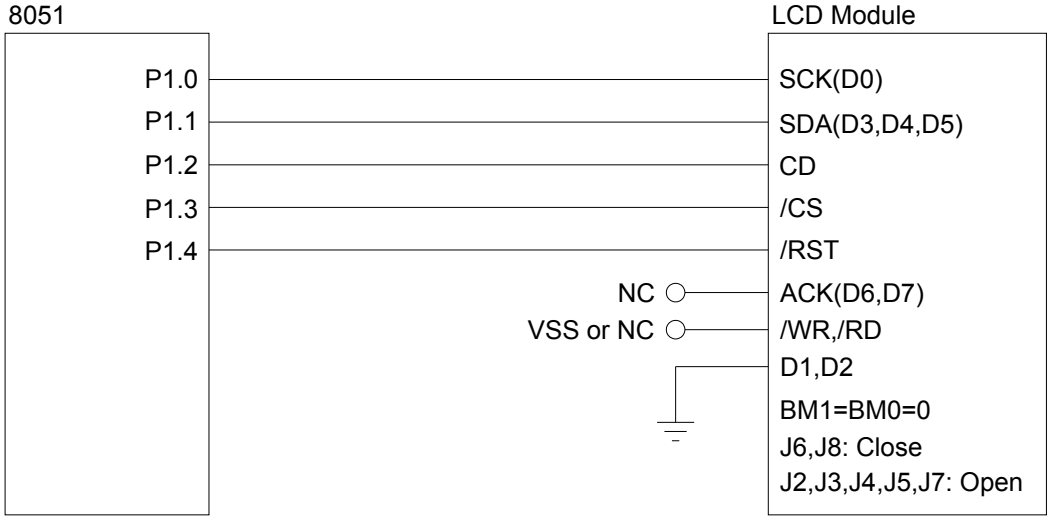
Note: CS1(A3) is internally fixed to “H”.



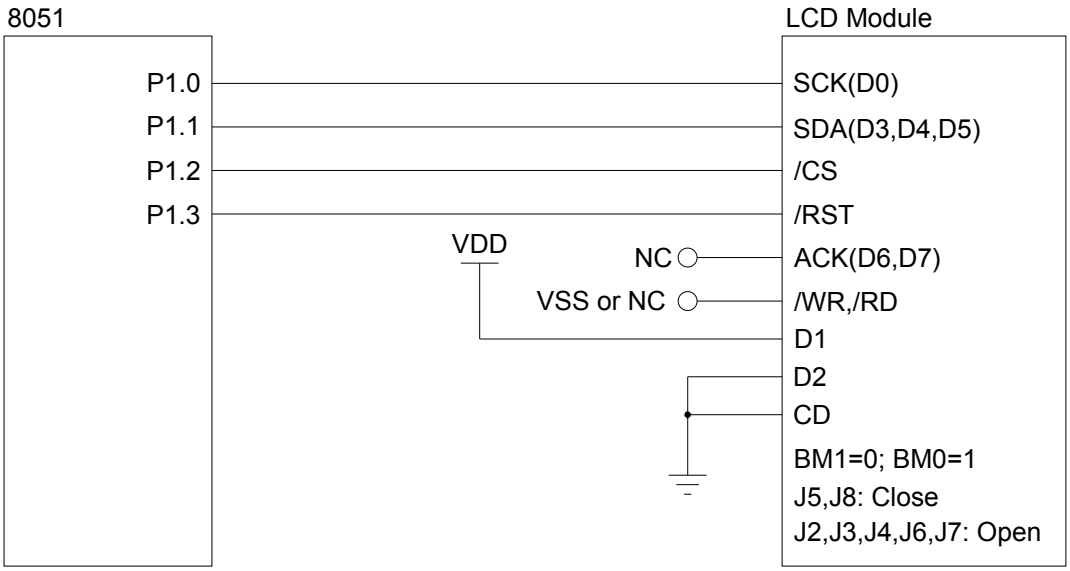

a. 8080 8-bit parallel interface



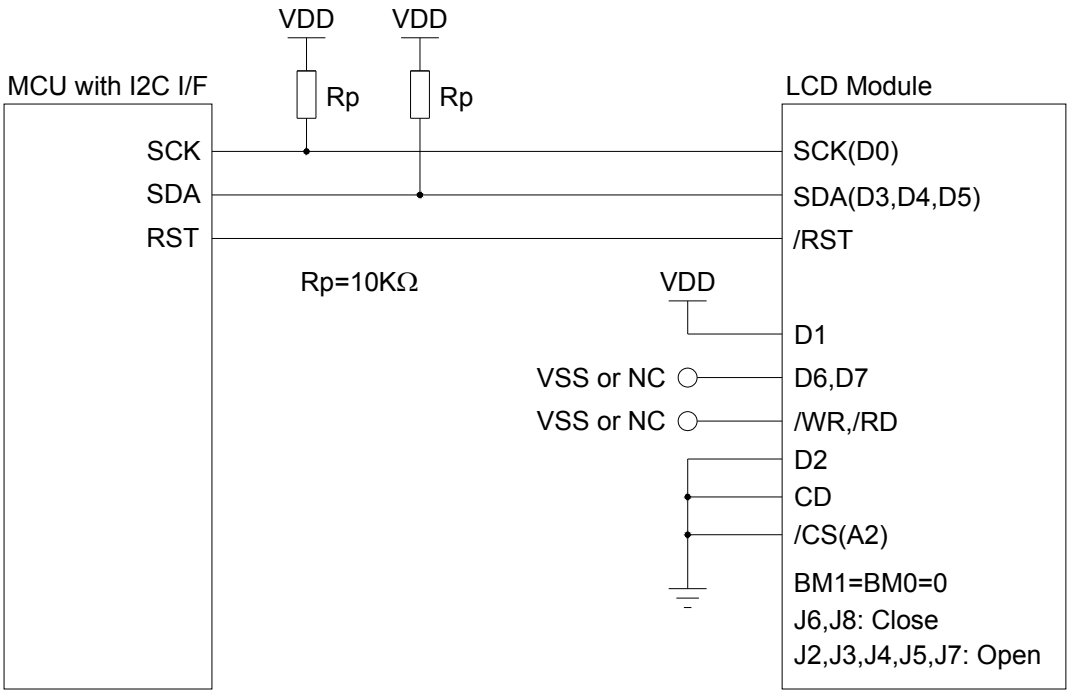

b. 6800 8-bit parallel interface




c. 4-wire SPI (S8) interface




d. 3-wire SPI (S9) interface




e. 2-wire SPI (I2C) interface

# *6. INITIALIZATION AND POWER OFF*

## 6.1 Power on Initialization Sequence

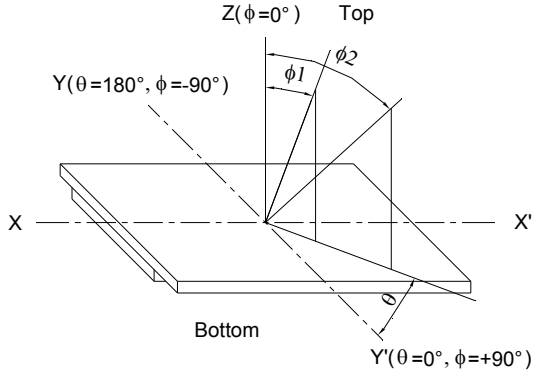
| No. | Command | Operation |
|---|---|---|
| 1 | Power on | Power on. Wait 3ms until $V_{DD}$ is stabilized |
| 2 | Reset | a. Set /RST= "L"<br>b. Wait 5ms<br>c. Set /RST="H"<br>d. Wait 150ms, then start the below initialization commands. |
| 3 | Set Temperature Compensation: 24H | TC[2:0]=100b: -0.05%/°C (Compensation coefficient) |
| 4 | Set LCD Mapping Control: C4H | LC1(MY)=1b: COM reverse<br>LC0(MX)=0b: SEG normal |
| 5 | Set Line Rate: A2H | LC[3:2]=10b: 12.8klps (On/Off mode) |
| 6 | Set Pump Control: 2DH | PC=1b: Internal $V_{LCD}$ (10x charge pump) |
| 7 | Set LCD Bias Ratio: EAH | BR[1:0]=10b: 1/11 bias |
| 8 | Set $V_{BIAS}$ Potentiometer: 81H, 93 | PM[7:0]=93. 93 is a reference value, modify this value to get the best display contrast. Because of the manufacturing dispersion of LCD modules, potentiometer (PM[7:0]) value may need be changed to match the driving voltage (VLCD) of different LCD modules. |
| 9 | Set RAM Address Control: 89H | AC[2:0]=001b: CA (column address) increases (+1) first until CA reaches CA boundary, then PA (page address) will increase by (+1). CA or PA will restart when reaching the boundary. |
| 10 | Set COM Scan Function: 86H | CFS=0b: Interlace scan |
| 11 | Set Partial Display Control: 85H | LC8=1b: Enable partial display function |
| 12 | Set COM End: F1H, 159 | CEN[7:0]=159 |
| 13 | Set Partial Display Start: F2H, 64 | DST[7:0]=64, starts from COM65 |
| 14 | Set Partial Display End: F3H, 159 | DEN[7:0]=159, ends with COM160 |
| 15 | Set Display Mode: 95H | DC[5:4]=01b: 1 bit per pixel, pattern 0 |
| 16 | Set Display Enable: C9H, ADH | DC[3:2]=01b: B/W mode, display on |
| 17 | Wait 10ms | Wait for internal DC-DC converter stabilized |
| 18 | End of initialization | |

## 6.2 Power off Sequence

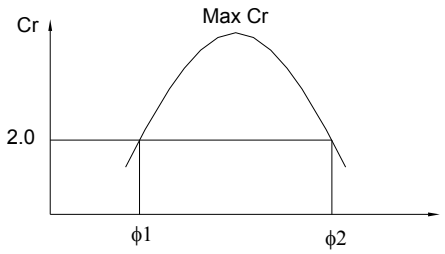
| No. | Command | Description |
|---|---|---|
| 1 | Optional status | Normal operation |
| 2 | Set Display Enable: C9H, ACH | DC[3:2]=00b: B/W mode, display disable |
| 3 | Wait 1ms | Drain DC-DC converter capacitors |
| 4 | Power off | Power off |

# *7. ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)*

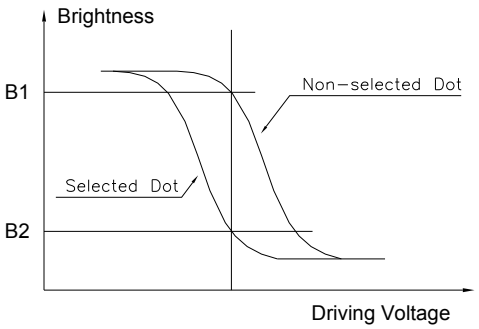
| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| View Angle | Φ2-Φ1 | Cr≥2 , θ=0° | - | 70 | - | Deg | Note1, Note2 |
| Contrast Ratio | Cr | Φ=0°,θ=0° | 3 | - | - | - | Note3 |
| Response Time | tr (rise) | Φ=0°,θ=0° | - | 200 | - | ms | Note4 |
| | tf (fall) | Φ=0°,θ=0° | - | 250 | - | ms | |




Note1: Definition of viewing angle ϕ, θ

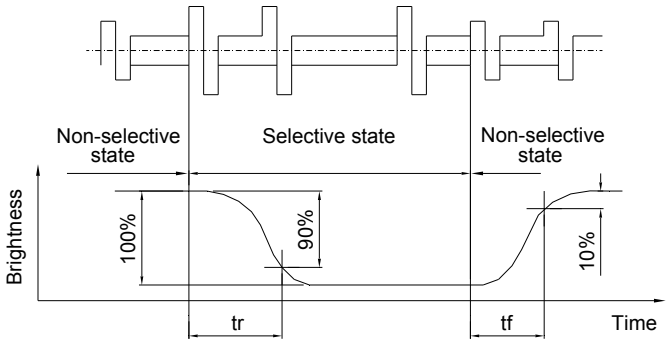



Note2: Definition of viewing angle range ϕ1, ϕ2



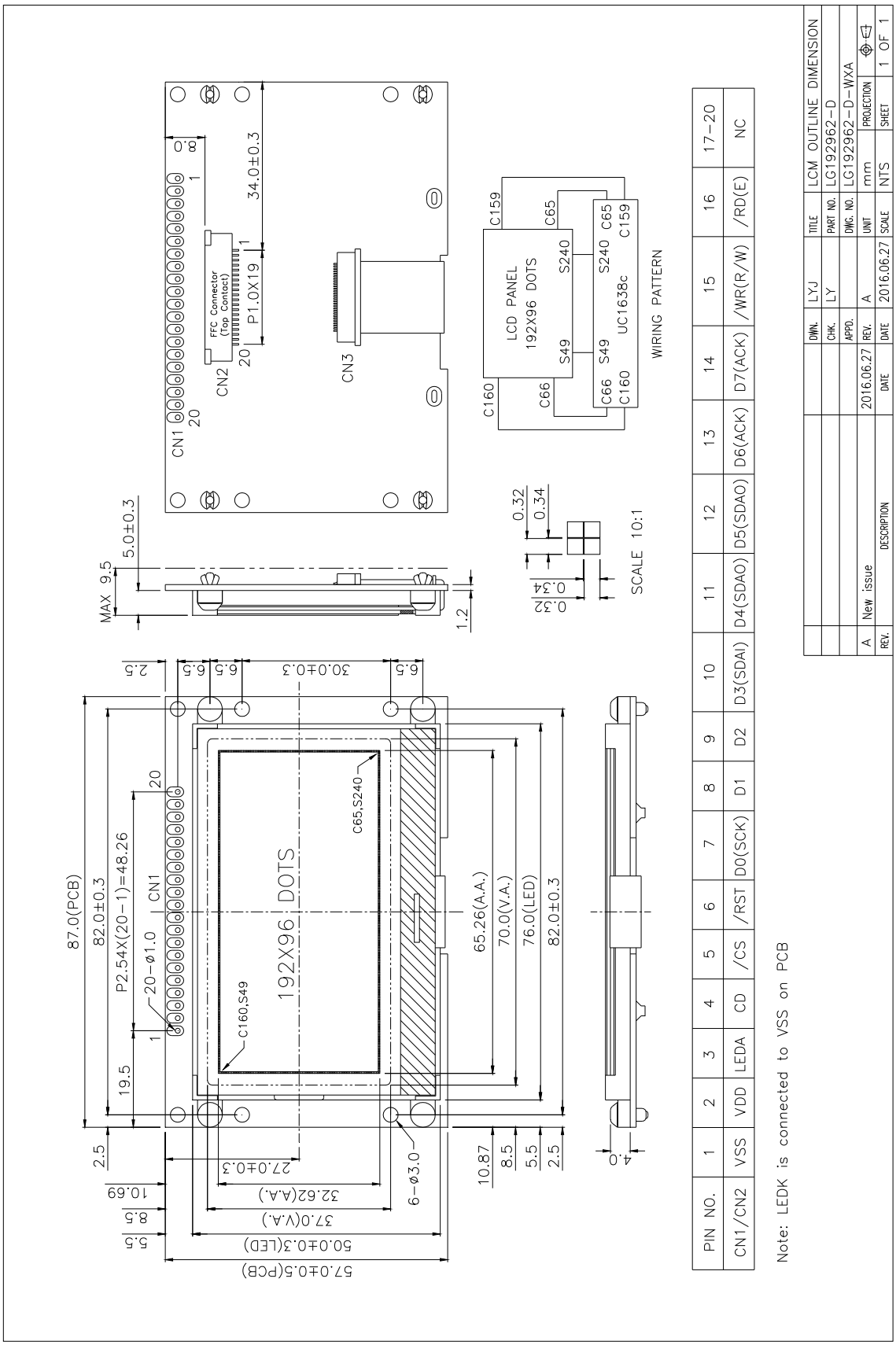

$$\text{Contrast Ratio} = \frac{\text{Brightness of non-selected dot (B1)}}{\text{Brightness of selected dot (B2)}}$$

Note3: Definition of contrast ratio (positive type)




Note3: Definition of response time

# 8. DIMENSIONAL OUTLINE




| PIN NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17-20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CN1/CN2 | VSS | VDD | LEDA | CD | /CS | /RST | D0(SCK) | D1 | D2 | D3(SDAI) | D4(SDAO) | D5(SDAO) | D6(ACK) | D7(ACK) | /WR(R/W) | /RD(E) | NC |

## *9. LCD MODULE NUMBERING SYSTEM*

| L | G | 192 | 96 | 2 | - | F | F | D | W | H | 6 | V | - | V33 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (1) | (2) | (3) | (4) | (5) | | (6) | (7) | (8) | (9) | (10) | (11) | (12) | | (13) |

**(1)** Brand

**(2)** Module type

**C** - Character module

**G** - Graphic module

**(3)** Display format

Character module : Number of characters per line, two digits XX

Graphic module : Number of columns, three digits XXX

**(4)** Display format

Character module : Number of lines, one digit X

Graphic module : Number of rows, two or three digits XX or XXX

**(5)** Development number : One or two digits X or XX

**(6)** LCD mode

**T** - TN Positive, Gray **N** - TN Negative, Blue

**S** - STN Positive, Yellow green **G** - STN Positive, Gray

**B** - STN Negative, Blue **F** - FSTN Positive, White

**K** - FSTN Negative, Black **L** - FSTN Negative, Blue

**Q** - FFSTN Negative, Black

**(7)** Polarizer mode

**R** - Reflective **F** - Transflective **M** - Transmissive

**(8)** Backlight type

**N** - Without backlight **L** - Array LED **D** - Edge light LED **E** - EL **C** - CCFL

**(9)** Backlight color

**Y** - Yellow green **B** - Blue **W** - White **G** - Green

**A** - Amber **R** - Red **M** - Multi color **N or Nil** - Without backlight

**(10)** Operating temperature range

**S** - Standard temperature (0 to +50 $^{o}$C) **H** - Extended temperature (-20 to +70 $^{o}$C)

**(11)** Viewing direction

**3** - 3:00 **6** - 6:00 **9** - 9:00 **U** - 12:00

**(12)** DC-DC Converter

**N or Nil** - Without DC-DC converter **V** - Built in DC-DC converter

**(13)** Version code

**V33** - 3.3V for VDD and LED backlight

# *10. PRECAUTIONS FOR USE OF LCD MODULE*

## 10.1 Handing Precautions

1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
2) If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth. If the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
3) Do not apply excessive force on the surface of display or the adjoining areas of LCD module since this may cause the color tone to vary.
4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
5) If the display surface of LCD module becomes contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents.
   · Isopropyl alcohol
   · Ethyl alcohol
   Solvents other than those mentioned above may damage the polarizer.
   Especially, do not use the following:
   · Water
   · Ketone
   · Aromatic Solvents
6) When mounting the LCD module make sure that it is free of twisting, warping, and distortion. Distortion has great influence upon display quality. Also keep the stiffness enough regarding the outer case.
7) Be sure to avoid any solvent such as flux for soldering never stick to Heat-Seal. Such solvent on Heat-Seal may cause connection problem of heat-Seal and TAB.
8) Do not forcibly pull or bend the TAB I/O terminals.
9) Do not attempt to disassemble or process the LCD module.
10) NC terminal should be open. Do not connect anything.
11) If the logic circuit power is off, do not apply the input signals.
12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
   · Be sure to ground the body when handling the LCD module.
   · Tools required for assembly, such as soldering irons, must be properly grounded.
   · To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
   · The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

## 10.2 Storage Precautions

1) When storing the LCD module, avoid exposure to direct sunlight or to the light of fluorescent lamps and high temperature/high humidity. Whenever possible, the LCD module should be stored in the same conditions in which they were shipped from our company.

2) Exercise care to minimize corrosion of the electrodes. Corrosion of the electrodes is accelerated by water droplets or a current flow in a high humidity environment.

### 10.3 Design Precautions

1) The absolute maximum ratings represent the rated value beyond which LCD module can not exceed. When the LCD modules are used in excess of this rated value, their operating characteristics may be adversely affected.
2) To prevent the occurrence of erroneous operation caused by noise, attention must be paid to satisfy VIL, VIH specification values, including taking the precaution of using signal cables that are short.
3) The liquid crystal display exhibits temperature dependency characteristics. Since recognition of the display becomes difficult when the LCD is used outside its designated operating temperature range, be sure to use the LCD within this range. Also, keep in mind that the LCD driving voltage levels necessary for clear displays will vary according to temperature.
4) Sufficiently notice the mutual noise interference occurred by peripheral devices.
5) To cope with EMI, take measures basically on outputting side.
6) If DC is impressed on the liquid crystal display panel, display definition is rapidly deteriorated by the electrochemical reaction that occurs inside the liquid crystal display panel. To eliminate the opportunity of DC impressing, be sure to maintain the AC characteristics of the input signals sent to the LCD Module.

### 10.4 Others

1) Liquid crystals solidify under low temperatures (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white).
   Air bubbles may also be generated if the LCD module is subjected to a strong shock at a low temperature.
2) If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
3) To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity, etc., exercise care to avoid touching the following sections when handling the module:
   · Terminal electrode sections.
   · Part of pattern wiring on TAB, etc.