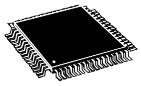
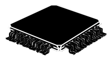
High-density performance 32-bit ARM® MCU with 256 KB Flash / 36 KB SRAM, 7 TIMs, 12-bit ADC, 11 comm.interfaces, USB, support ChibiOS & QMK design



LQFP64 (10 x 10 mm)



LQFP48 (7 x 7 mm)

Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 96 MHz maximum frequency
  - Dedicated instruction and data caches support 0 wait state memory access
  - Single-cycle multiplication and hardware division
  - AHB,APB1 and APB2 clocks are independent of each other
- Memories
  - 256Kbytes Flash memory
  - 36Kbytes SRAM
- Reset and supply management
  - Dual power supply, main power VDD:2.0V~3.6V, Backup battery power VBAT:1.8V~3.6V
  - Power On Reset(POR),Power Down Reset(PDR), Programmable Voltage Detector (PVD)
- Clock
  - 4 ~ 16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 48 MHz factory-trimmed RC
  - Internal 32 kHz RC for WDG
  - 32.768KHz oscillator for RTC with calibration
- Low power
  - Trickle-Powe: Sleep, Stop and Standby modes
  - Dynamic current(Rum mode, disable peripherals): ~140uA/MHz@3.3V
  - Stop mode: ~35uA@3.3V
  - Standby mode: ~4.5uA@3.3V
  - VBAT with RTC: ~1.1uA@3.3V
  - VBAT operation is activated when VDD is not present ,supplies the 84-byte backup registers.
- Operation temperature
  - Industrial temperature range: -40°C~+85°C
  - Commercial temperature range: 0°C~85°C
- 12-bit mode ADC
  - Max convert rate: 1Msps
  - Up to 16 A/D channels
  - Flexible sample and converter modes.
  - Temperature sensor
- Special design to support
  - ChibiOS and QMK.
- Up to 51 fast I/O ports
  - 37 or 51 I/Os, all mappable on 16 external interrupt vectors
- Debug mode
  - Serial wire debug (SWD) interface
- Up to 10 communication interfaces
  - Up to 2 I2C interfaces (SMBus)
  - Up to 3 UART (6 Mbit/s)
  - Up to 3 SPIs, 1 QSPI
  - 1 USB 2.0 full-speed device controller
- Up to 7 timers
  - Up to three 20-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - One 20-bit motor control PWM timer with dead-time generation and emergency stop
  - 2 watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
- 2 DMA controller, triggered by Timers, ADC, SPIs, I2Cs, UARTs
- RTC clock counter
- CRC calculation unit, 96-bit unique ID
- USB boot code to allow download user code form USB interface

Contents

List of Figures

List of Tables

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the WB32FQ95xC high-density performance line microcontrollers.

For this series and other series of datasheets, reference manuals, product selection tables, etc., you can available from the official website(http://www.westberrytech.com/).

For information on Applications, memory and peripherals of this microcontroller please refer to the

WB32FQ95xx reference manual.

The high-density WB32FQ95xC datasheet should be read in conjunction with the WB32FQ95xx reference manual.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual.

WB32FQ95xC family products have LQFP64, LQFP48packages, different packages have different peripherals.

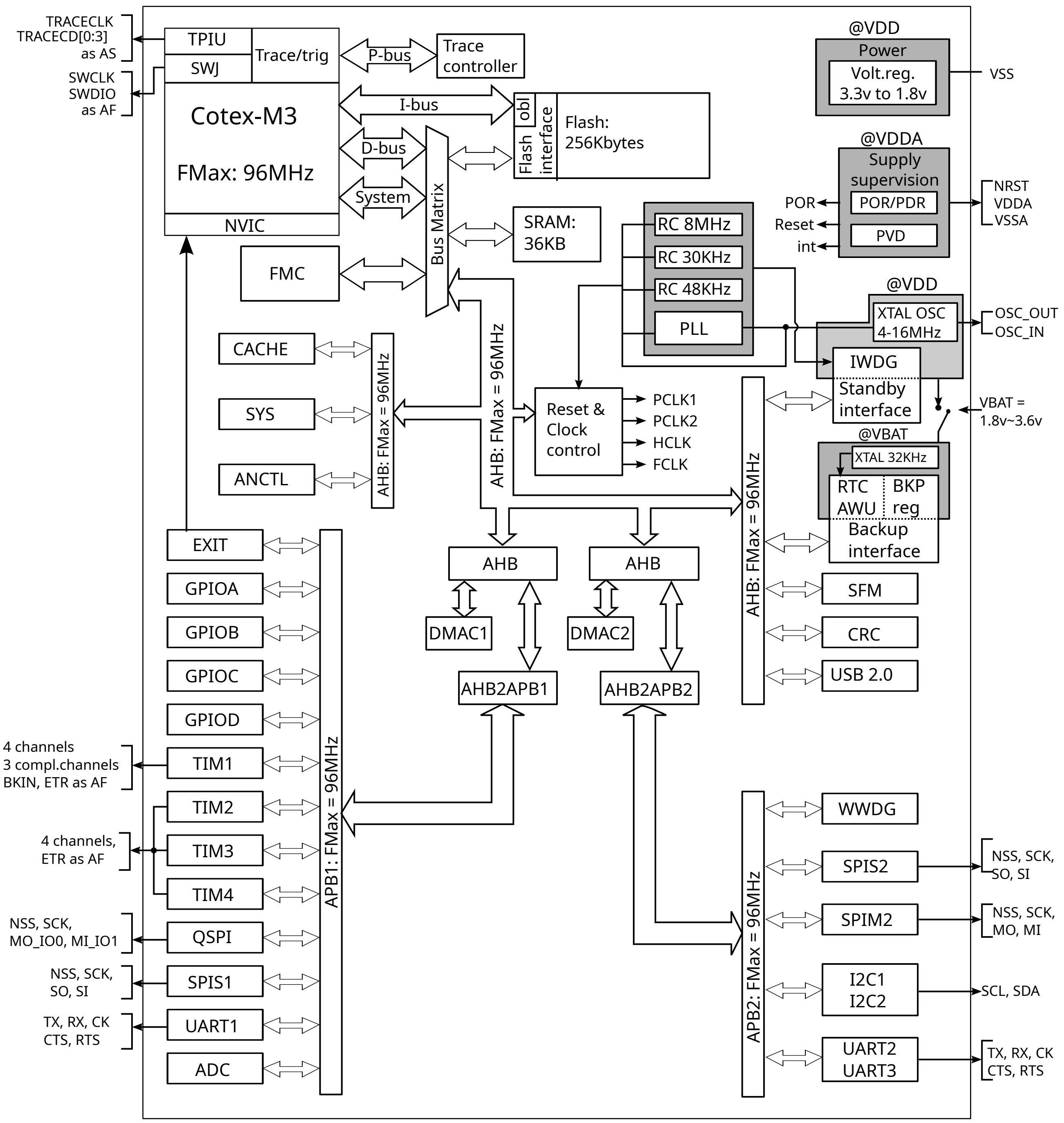
2 Overview

The WB32FQ95xC performance line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 96 MHz frequency, high-speed embedded memories (Flash memory up to 256 Kbytes and SRAM up to 36 Kbytes),

one 20-bit advanced control timer, three general purpose timers, two watchdog timers (Independent and Window), three SPI interfaces, one QSPI interface, two I2C interfaces, three UART interfaces, one USB2.0 Full Speed interface, one SAR ADC converter, two 10-channel comparators, one RTC

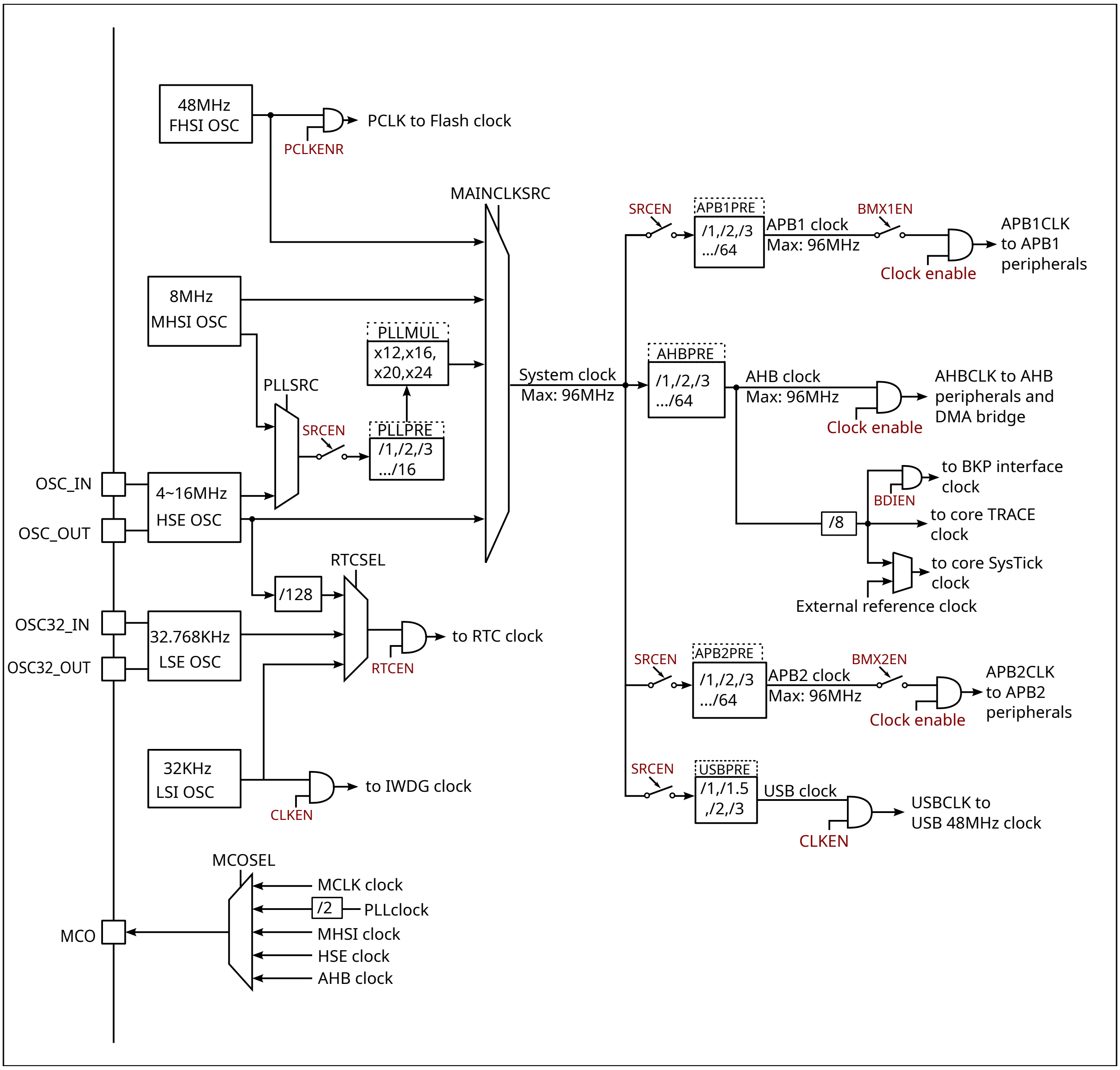
2.1 performance line block diagram

Fig 2.1-1 WB32FQ95xC performance line block diagram



2.2 clock tree

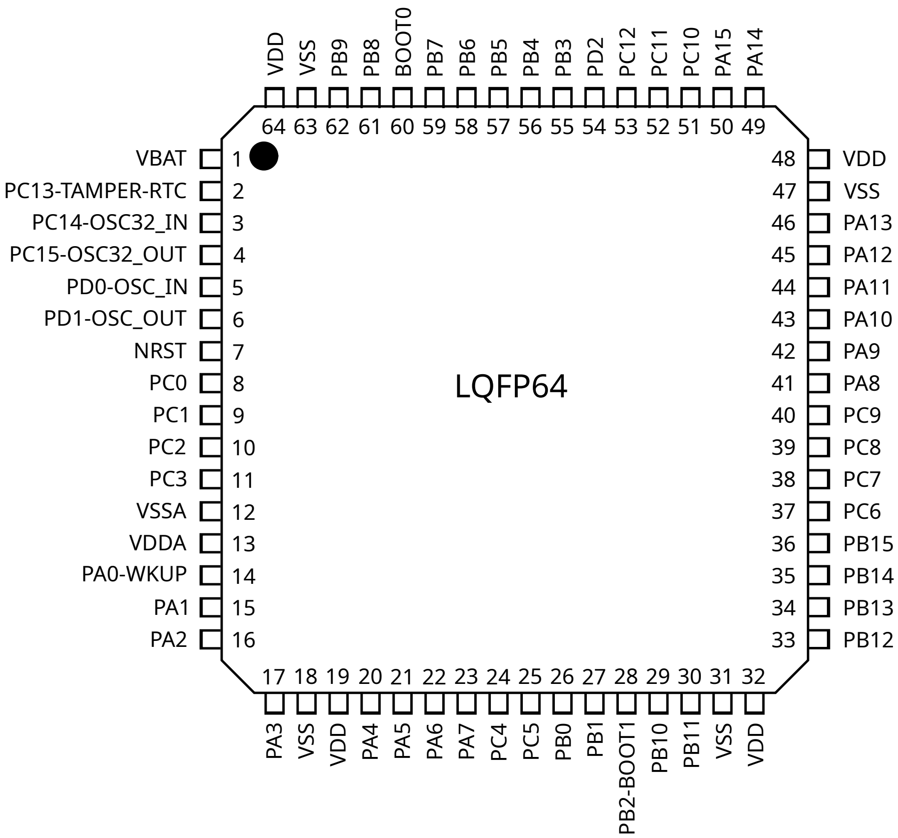
Fig 2.2-1 WB32FQ95xC clock



3 Pinouts and pin descriptions

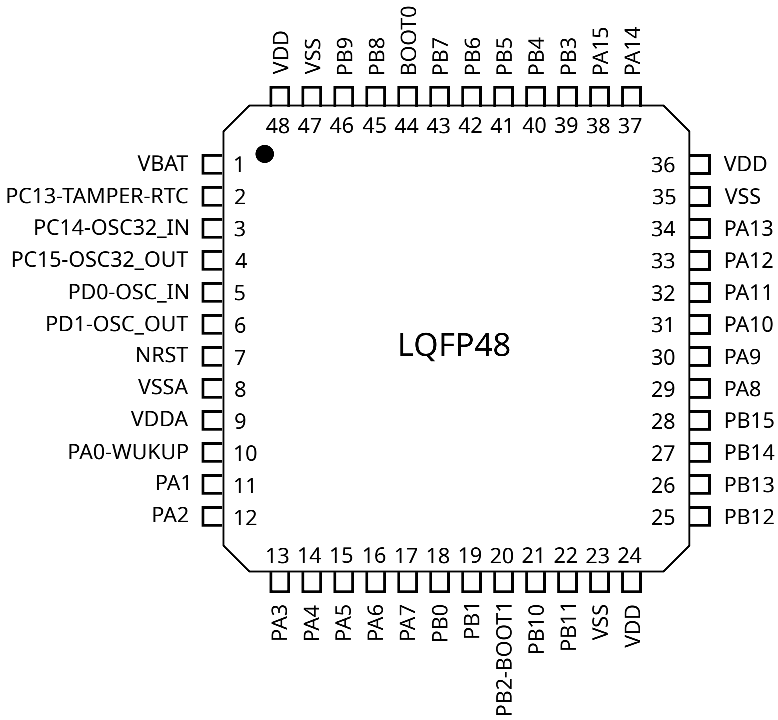
3.1 LQFP64 pinouts

Fig 3.1-1 LQFP64 pinouts



3.2 LQFP48 pinouts

Fig 3.2-1 LQFP48 pinouts



3.3 pin descriptions

Tab 3.3-1 WB32FQ95xC pin descriptions

Pin No.		Pin Name	Type	Main Function	Alternate Function	Analog Function
LQFP48	LQFP64					
1	1	VBAT	S	VBAT		
2	2	PC13	I/O	PC13	TAMPER/RTC	
3	3	PC14	I/O	PC14		OSC32_IN
4	4	PC15	I/O	PC15		OSC32_OUT
5	5	PD0	I/O	PD0		OSC_IN
6	6	PD1	I/O	PD1		OSC_OUT
7	7	NRST	I/O	NRST		
-	8	PC0	I/O	PC0	SPIM2_NSS0 / SPIS2_NSS	ADC_IN10
-	9	PC1	I/O	PC1	SPIM2_SCK / SPIS2_SCK	ADC_IN11
-	10	PC2	I/O	PC2	SPIM2_MI / SPIS2_SO	ADC_IN12
-	11	PC3	I/O	PC3	SPIM2_MO / SPIS2_SI	ADC_IN13
8	12	VSSA	S	VSSA		
9	13	VDDA	S	VDDA		
10	14	PA0	I/O	PA0/WKUP	TIM2_CH1_ETR / UART2_CTS / WKUP	ADC_IN0
11	15	PA1	I/O	PA1	TIM2_CH2 / UART2_RTS	ADC_IN1
12	16	PA2	I/O	PA2	TIM2_CH3 / UART2_TX	ADC_IN2
13	17	PA3	I/O	PA3	TIM2_CH4 / UART2_RX	ADC_IN3
-	18	VSS_4	S	VSS_4		
-	19	VDD_4	S	VDD_4		
14	20	PA4	I/O	PA4	QSPI_NSS0 / SPIS1_NSS / UART2_CK	ADC_IN4
15	21	PA5	I/O	PA5	QSPI_SCK / SPIS1_SCK	ADC_IN5
16	22	PA6	I/O	PA6	TIM1_BKIN / TIM3_CH1 / QSPI_MI_IO1 / SPIS1_SO	ADC_IN6
17	23	PA7	I/O	PA7	TIM1_CH1N / TIM3_CH2 / QSPI_MO_IO0 / SPIS1_SI	ADC_IN7
-	24	PC4	I/O	PC4	TRACECK	ADC_IN14
-	25	PC5	I/O	PC5	SPIM2_NSS2 / TRACED0	ADC_IN15
18	26	PB0	I/O	PB0	TIM1_CH2N / TIM3_CH3 / QSPI_IO2	ADC_IN8
19	27	PB1	I/O	PB1	TIM1_CH3N / TIM3_CH4 / QSPI_IO3	ADC_IN9
20	28	PB2	I/O	PB2/BOOT1		
21	29	PB10	I/O	PB10	TIM2_CH3 / TIM4_CH1 / QSPI_NSS2 / UART3_TX	
22	30	PB11	I/O	PB11	TIM2_CH4 / SPIM2_NSS1 / UART3_RX	
23	31	VSS_1	S	VSS_1		
24	32	VDD_1	S	VDD_1		
25	33	PB12	I/O	PB12	TIM1_BKIN / SPIM2_NSS0 / SPIS2_NSS / UART3_CK	
26	34	PB13	I/O	PB13	TIM1_CH1N / SPIM2_SCK / SPIS2_SCK / UART3_CTS	
27	35	PB14	I/O	PB14	TIM1_CH2N / SPIM2_MI / SPIS2_SO / UART3_RTS	
28	36	PB15	I/O	PB15	TIM1_CH3N / SPIM2_MO / SPIS2_SI	
-	37	PC6	I/O	PC6	TIM3_CH1	
-	38	PC7	I/O	PC7	TIM3_CH2	
-	39	PC8	I/O	PC8	TIM3_CH3	
-	40	PC9	I/O	PC9	TIM3_CH4 / TRACED1	
29	41	PA8	I/O	PA8	TIM1_CH1 / UART1_CK / MCO	
30	42	PA9	I/O	PA9	TIM1_CH2 / UART1_TX	
31	43	PA10	I/O	PA10	TIM1_CH3 / UART1_RX	
32	44	PA11	I/O		TIM1_CH4 / UART1_CTS	USBDM
33	45	PA12	I/O		TIM1_ETR / UART1_RTS	USBDP
34	46	PA13	I/O	SWDIO	QSPI_NSS1	
35	47	VSS_2	S	VSS_2		

(continued)

Pin No. LQFP48	Pin No. LQFP64	Pin Name	Type	Main Function	Alternate Function	Analog Function
36	48	VDD_2	S	VDD_2		
37	49	PA14	I/O	SWDCLK	QSPI_NSS2	
38	50	PA15	I/O	PA15	TIM2_CH1_ETR / I2C1_SMBAI / QSPI_NSS0 / SPIS1_NSS	
-	51	PC10	I/O	PC10	UART3_TX / TRACED2	
-	52	PC11	I/O	PC11	UART3_RX / TRACED3	
-	53	PC12	I/O	PC12	TIM4_ETR / UART3_CK	
-	54	PD2	I/O	PD2	TIM3_ETR	
39	55	PB3	I/O	PB3	SWO / TIM2_CH2 / QSPI_SCK / SPIS1_SCK	
40	56	PB4	I/O	PB4	TIM3_CH1 / QSPI_MI_IO1 / SPIS1_SO	
41	57	PB5	I/O	PB5	TIM3_CH2 / I2C1_SMBAI / QSPI_MO_IO0 / SPIS1_SI	
42	58	PB6	I/O	PB6	TIM4_CH1 / I2C1_SCL / QSPI_NSS1 / UART1_TX	
43	59	PB7	I/O	PB7	TIM4_CH2 / I2C1_SDA / SPIM2_NSS1 / UART1_RX	
44	60	BOOT0	I	BOOT0		
45	61	PB8	I/O	PB8	TIM4_CH3 / I2C1_SCL / SPIM2_NSS2 / UART1_CTS	
46	62	PB9	I/O	PB9	TIM4_CH4 / I2C1_SDA / UART1_RTS	
47	63	VSS_3	S	VSS_3		
48	64	VDD_3	S	VDD_3		

[1] Function availability depends on the chosen device.

[2]Symbols: S-supply, I-input, I/O-input/outp

Tab 3.3-2 WB32FQ95xC alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS	TIM1/2	TIM3/4		I2C	SPI(M)	SPI(S)	UART
PA0	WKUP	TIM2_CH1 TIM2_ETR						UART2_CTS
PA1		TIM2_CH2						UART2_RTS
PA2		TIM2_CH3						UART2_TX
PA3		TIM2_CH4						UART2_RX
PA4						QSPI_NSS0	SPIS1_NSS	UART2_CK
PA5						QSPI_SCK	SPIS1_SCK	
PA6		TIM1_BKIN	TIM3_CH1			QSPI_MI_IO1	SPIS1_SO	
PA7		TIM1_CH1N	TIM3_CH2			QSPI_MO_IO0	SPIS1_SI	
PA8	MCO	TIM1_CH1						UART1_CK
PA9		TIM1_CH2						UART1_TX
PA10		TIM1_CH3						UART1_TX
PA11		TIM1_CH4						UART1_TX
PA12		TIM1_ETR						UART1_RTS
PA13	SWO_DIO					QSPI_NSS1		
PA14	SWO_CLK					QSPI_NSS2		
PA15		TIM2_CH1 TIM2_ETR			I2C_SMBAI	QSPI_NSS0	SPIS1_NSS	
PB0		TIM1_CH2N	TIM3_CH3			QSPI_IO2		
PB1		TIM1_CH3N	TIM3_CH4			QSPI_IO3		
PB2	BOOT1							
PB3	SWO	TIM2_CH2				QSPI_SCK	SPIS1_SCK	
PB4			TIM3_CH1			QSPI_MI_IO1	SPIS1_SO	

(continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS	TIM1/2	TIM3/4		I2C	SPI(M)	SPI(S)	UART
PB5			TIM3_CH2		I2C1_SMBAI	QSPI_MO_IO0	SPIS1_SI	
PB6			TIM4_CH1		I2C1_SCL	QSPI_NSS1		UART1_TX
PB7			TIM4_CH2		I2C1_SDA	SPIM2_NSS1		UART1_RX
PB8			TIM4_CH3		I2C1_SCL	SPIM2_NSS2		UART1_CTS
PB9			TIM4_CH4		I2C1_SDA			UART1_RTS
PB10		TIM2_CH3	TIM4_CH1		I2C2_SCL	QSPI_NSS2		UART3_TX
PB11		TIM2_CH4			I2C2_SDA	SPIM2_NSS1		UART3_RX
PB12		TIM1_BKIN				SPIM2_NSS0	SPIS2_NSS	UART3_CK
PB13		TIM1_CH1N				SPIM2_SCK	SPIS2_SCK	UART3_CTS
PB14		TIM1_CH2N				SPIM2_MI	SPIS2_SO	UART3_RTS
PB15		TIM1_CH3N				SPIM2_MO	SPIS2_SI	
PC0						SPIM2_NSS0	SPIS2_NSS	
PC1						SPIM2_SCK	SPIS2_SCK	
PC2						SPIM2_MI	SPIS2_SO	
PC3						SPIM2_M0	SPIS2_SI	
PC4	TRACECK							
PC5	TRACED0					SPIM2_NSS2		
PC6			TIM3_CH1					
PC7			TIM3_CH2					
PC8			TIM3_CH3					
PC9	TRACED1		TIM3_CH4					
PC10	TRACED2							UART3_TX
PC11	TRACED3							UART3_RX
PC12			TIM4_ETR					UART3_CK
PC13	TAMPER_RTC							
PC14	OSC32_IN							
PC15	OSC32_OUT							
PD0	OSC_IN							
PD1	OSC_OUT							
PD2			TIM3_ETR					

4 Device description

4.1 ARM® Cortex™-M3 core

The 32-bit Arm® Cortex®-M3 core processor is designed for high-performance, real-time processing in cost-constrained applications and can handle complex tasks. Any Arm® Cortex®-M3 microcontroller offers high scalability combined with an optimal trade-off between performance and cost.

- Three-stage pipeline and branch prediction to improve the instruction execution speed of the processor.
- Adopt Harvard structure, with independent instruction bus and data bus, which can make instruction fetch and data access parallel.
- Built-in Nested Vectored Interrupt Controller (NVIC).
- Support for bit-binding operations.
- Support for SWD Debug.
- Support for low power modes.
- Uses the efficient Thumb2 16/32-bit mixed instruction set.
- 32-bit hardware division and single-cycle multiplication.
- Support for unaligned memory accesses.

With its embedded ARM core, WB32FQ95xC performance line family is compatible with all ARM tools and software.

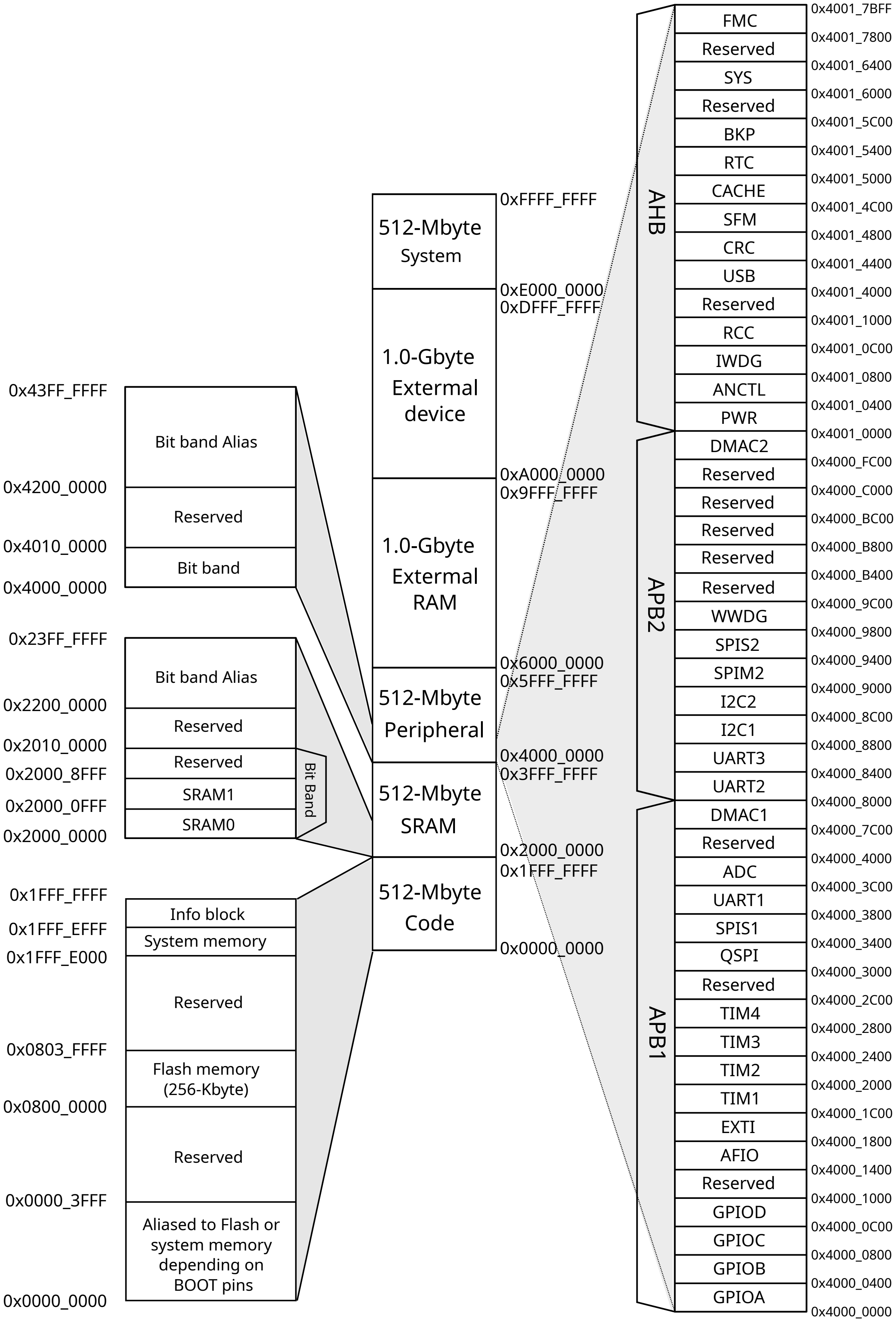
4.2 Memory mapping

WB32FQ95xC has up to 4-Gbyte address space, which can be divided into six areas: code area, SRAM area, peripherals area, external RAM area, external device area, and system area.

- Code area(0.5-Gbyte)
  - Boot map memory(256-Kbyte): Aliased to Flash orsystem memory depending on BOOT pins.
  - Main Flash memory (256 Kbyte): For storing user programs and data. The size of main flash memory depends on the selected device, for the flash size of different models of MCU please refer to the Tab7.0-1.
  - System memory(4-Kbyte): For stores the boot program in bootstrap mode.
  - information memory(INFO)(4Kbyte): Store system security configuration information for setting system security configuration.
- SRAM area(0.5-Gbyte): WB32FQ95xC has up to 36 Kbyte of available SRAM space, divided into SRAM0 and SRAM1 part, they are all in the bit-band region. The size of SRAM depends on the selected device, for the SRAM size of different models of MCU please refer to the Tab7.0-1.
- Peripherals area(0.5-Gbyte): All peripheral registers are located in this region and are in the bitband region of this region.
- External device area(1-Gbyte)
- external Device area(1-Gbyte)
- System area(0.5-Gbyte): The internal peripherals of the Cortex™-M3 are in this area.

The memory map is shown in Fig4.2-1.

Fig 4.2-1 WB32FQ95xC Memory map



The Cortex®-M3 memory map includes two bit-band regions:SRAM area and peripherals area.These regions map each word in an alias region of memory to a bit in a bit-band region of memory. For specific operation methods, please refer to ”Cortex™-M3 Core Manual”.

Note: *The unlisted areas are reserved areas or system internal configuration areas and cannot be accessed by users.*

4.3 Embedded Flash memory

Up to 256 Kbytes of embedded Flash is available for storing programs and data. The flash memory can be programmed through the flash memory control module(FMC).

4.4 Embedded SRAM

Up to 36 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

4.5 Clock

Four different clock sources can be used to drive the system main clock(MAINCLK):

- MHSI(8Mhz) internal oscillator clock
- FHSI(48MHz) internal oscillator clock
- HSE external oscillator clock
- PLL clock

System main clock selection is performed on startup, however the internal RC 8 MHz oscillator (MHSI) is selected as default CPU clock on reset. An external 4-16 MHz clock (HSE) can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB, APB1 and APB2 frequency.The maximum frequency of the AHB, APB1 and APB2 domains is 96 MHz. See Fig2.2-1 for details on the clock tree.

4.6 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using UART1.

4.7 Nested vectored interrupt controller (NVIC)

The WB32FQ95xC performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

4.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB1 clock period.

4.9 Power supply schemes

- VDD = 2.0V ~ 3.6V: VDD powers the I/O pins and the internal voltage regulator (LDO).
- VDDA = 2.4V ~ 3.6V: VDDA powers the microcontroller analog block.
- VBTA = 1.8V ~ 3.6V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.

4.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when VDD is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the VDD power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD drops below the V_{PVD} threshold and/or when VDD is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

4.11 System reset

Any source above can trigger the sysrem reset. When the working voltage is proper, the MHSI will be turned on and keep active. When NRST is asserted to high level, the oscillator will start running, and the flash controller will finish the device initilization.

- Power on reset (POR)
- A low level on the NRST pin (external reset)
- A software reset (SW reset)
- Window watchdog end of count condition (WWDG reset)
- Independent watchdog end of count condition (IWDG reset)
- Low-power management reset (PWR)

4.12 Low-power modes

WB32FQ95xC performance line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

4.12.1 Sleep mode

Sleep mode can reduce system dynamic power consumption by processor, memory and internal bus.

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and all instruction execution is suspended until an interrupt/event occurs. At this time, the clocks of the peripherals are controlled by registers and can generate interrupts to wake up the microcontroller to continue executing instructions.

In Sleep mode all peripheral registers, memory data and I/O pins keep the same states as in Run mode.

4.12.2 Stop mode

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal, low-power mode, or ultra-low-power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

4.12.3 Standby mode

The Standby mode is used to achieve the lowest power consumption. The internalvoltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the MHSI, the FHSI and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

In addition, power and clocking of used peripherals can be optimized to reduce system power consumption in normal run mode.

4.13 Real-time clock (RTC) and backup registers(BKP)

The RTC and the backup registers are supplied through a switch that takes power either on VDD supply when present or through the VBAT pin.

The RTC and the backup registers are supplied through a switch that takes power either on VDD supply when present or through the VBAT pin. The backup registers are twenty-one 16-bit registers used to store 84 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 30 kHz. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

4.14 cyclic redundancy check(CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial. WB32FQ95xC supports four general-purpose CRC polynomial algorithms: CRC-8, CRC-16/MOUBUS, CRC-16/CCITT, CRC - 32-bit hardware division and single-cycle multiplication.

4.15 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

4.16 Direct memory access controller(DMAC)

The flexible 6-channel general-purpose DMAs (3 channels for DMA1 and 3 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-toperipheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent. The DMA can be used with the main peripherals: SPI, I2C, UART, general-purpose, basic and advanced-control timers TIMx, I2S and ADC.

4.17 Analog to digital converter(ADC)

Three 12-bit analog-to-digital converters are embedded into WB32FQ95xC performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

The ADC requires an independent power supply, VDDA, with a power supply range of 2.4V to 3.6V. The ADC measurement range is from 0V to VDDA. The embedded temperature sensor is internally connected to the input channel of ADC_IN16 to convert the sensor output to a digital value.

4.18 Timers(TIMx)

The high-density WB32FQ95xC performance line devices include up to one advancedcontrol timer and three general-purpose timers. Tab4.18-1 compares the features of the advanced-control, general-purpose and basic timers.

Tab 4.18-1 High-density timer feature comparison

Timer	Resolution	Type	Prescaler	Capture/compare channels	Complementary outputs
TIM1	20-bit	Up, down, up/down	Any integer between 1 and 65536	4	Yes
TIM2/TIM3/TIM4	20-bit	Up, down, up/down	Any integer between 1 and 65536	4	No

Advanced-control timers (TIM1)based on a 20-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or onepulse mode output. In addition, channels 1 3 have complementary PWM outputs ithprogrammable inserted dead-times.

General-purpose timers (TIM2/TIM3/TIM4) based on a 20-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or onepulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages.

4.19 SysTick timer(Systick)

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

4.20 watchdog(WDG)

Two built-in watchdogs: independent watchdog and window watchdog, can be used to detect and solve faults caused by software errors, providing higher security, time accuracy and flexibility of use.

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 30 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the INFO block.

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

4.21 Universal serial bus (USB)

The WB32FQ95xC performance line embed a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the system main clock(MAINCLK).

4.22 Serial peripheral interface (SPI)

Up to 4 SPI interfaces: 2 master interfaces (one quad SPI master interface), 2 slave interfaces. The communication rate can be up to 24Mbit/s in master mode, and 18Mbit/s in slave mode. These SPI interfaces supports multiple frame size configurations, which can be configured to 4/8/16/32 bits per frame.

All SPIs can be served by the DMA controller.

4.23 Inter-integrated circuit (I2C) interface

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard, fast and high-speed modes. They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave) and they support SMBus 2.0.

All I2Cs can be served by the DMA controller.

4.24 Universal asynchronous receiver transmitters(UART)

Up to 3 UART interfaces, which provide asynchronous communication , support RS232 serial communication protocol and IrDA SIR infrared transmission protocol.

All UARTs can be served by the DMA controller.

5 Electrical Characteristics

5.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.1.1 Voltage characteristics

Tab 5.1-1 Voltage characteristics

Symbol	Ratings	Min	Max	Unit
VDD - VSS	External main supply voltage (including VDDA, VDD)[1]	-0.5	3.6	V
VIN	Input voltage on pin [2]	VSS - 0.3	VDD + 0.5	
$\|\Delta VDDx\|$	Variations between different VDD power pins	-	50	mV
$\|VSSx - VSS\|$	Variations between all the different ground pins	-	50	

[1] All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power.

[2] VIN maximum value must always be respected.

5.1.2 Current characteristics

Tab 5.1-2 Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into VDD power lines (source)[1]	60	mA
I_{VSS}	Total current out of VSS ground lines (sink)	60	
I_{IO}	Output current sunk by any I/O and control pin	16	
	Output current source by any I/Os and control pin	-16	
$I_{INJ(PIN)}$ [2]	Injected current on five-volt tolerant I/O	60	
$\sum I_{INJ(PIN)}$ [3]	Total injected current (sum of all I/O and control pins)	60	

[1] All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

[2] $I_{INJ(PIN)}$ must never be exceeded. A positive injection is induced by VIN>VDD while a negative injection is induced by VIN<VSS.

[3] When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.1.3 Thermal characteristics

Tab 5.1-3 Thermal characteristics

Symbol	Rating	Value	Unit
T_{STG}	Storage temperature range	-40 ~ +150	°C
T_J	Maximum junction temperature	100	

5.2 Operating conditions

5.2.1 General operating conditions

Symbel	Parameter	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	96	
f_{PCLK2}	Internal APB2 clock frequency	0	96	
VDD	Standard operating voltage	2	3.6	V
VDDA	Analog operating voltage(ADC not used)	2	3.6	
	Analog operating voltage(ADC used)	2.4	3.6	
VBAT	Backup operating voltage	1.8	3.6	
T	Ambient temperature	-40	85	°C

[1] It is recommended to power VDD and VDDA from the same source. A maximum difference of 300 mV between VDD and VDDA can be tolerated during power-up and operation

5.2.2 Embedded reset and power control block characteristics

Tab 5.2-2 Power on Reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Uint
T_{delay}	RSTN establish time	-	-	40	-	us
$V_{POR/PDR}$	Power on reset threshold	rising edge	-	1.92	-	V
		falling edge	-	1.88	-	V

Tab 5.2-3 PVD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector select (rising edge)	PLS[2:0] = 000	-	2.25	-	V
		PLS[2:0] = 001	-	2.35	-	
		PLS[2:0] = 010	-	2.45	-	
		PLS[2:0] = 011	-	2.55	-	
		PLS[2:0] = 100	-	2.65	-	
		PLS[2:0] = 101	-	2.75	-	
		PLS[2:0] = 110	-	2.85	-	
		PLS[2:0] = 111	-	2.95	-	
	Programmable voltage detector select (falling edge)	PLS[2:0] = 000	-	2.14	-	
		PLS[2:0] = 001	-	2.24	-	
		PLS[2:0] = 010	-	2.34	-	
		PLS[2:0] = 011	-	2.44	-	
		PLS[2:0] = 100	-	2.54	-	
		PLS[2:0] = 101	-	2.64	-	
		PLS[2:0] = 110	-	2.74	-	
		PLS[2:0] = 111	-	2.84	-	

5.2.3 External user clock characteristics

Tab 5.2-4 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	8	16	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7VDD	-	VDD	V
V_{HSEL}	OSC_IN input pin low level voltage		VSS	-	0.3VDD	
$t_{w(HSE)}$	OSC_IN high or low time		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	5	
$C_{in(HSE)}$	OSC_IN input capacitance		-	5	-	pf
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%

Tab 5.2-5 Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	-	MHz
V_{LSEH}	OSC_IN input pin high level voltage		0.7VDD	-	VDD	V
V_{LSEL}	OSC_IN input pin low level voltage		VSS	-	0.3VDD	
$t_{w(LSE)}$	OSC_IN high or low time		450	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	50	
$C_{in(LSE)}$	OSC_IN input capacitance		-	5	-	pf
$DuCy_{(LSE)}$	Duty cycle		45		70	%
$T_{SU(LSE)}$	startup time	VDD is stabilized	-	2	-	s

5.2.4 Internal clock source characteristics

Tab 5.2-6 High-speed internal (MHSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MHSI}	Frequency	-	-	8	-	MHz
$DuCy_{(MHSI)}$	Duty cycle	-	45	-	55	%
$ACC_{(MHSI)}$	Accuracy of the MHSI oscillator	T_A = -10 to 85°C	-1.5	-	2.2	%
		T_A = 0 to 75°C	-1.3	-	2	%
		T_A = 25°C	-1.1	-	1.8	%
$T_{SU(MHSI)}$	MHSI oscillator startup time	VSS ⩽ Vin ⩽ VDD	1	-	2	us
$I_{DD(MHSI)}$	MHSI oscillator power consumption	-	-	25	-	uA

Tab 5.2-7 High-speed internal (FHSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{FHSI}	Frequency	-	-	48	-	MHz
$DuCy_{(FHSI)}$	Duty cycle	-	45	-	55	%
$ACC_{(FHSI)}$	Accuracy of the FHSI oscillator	T_A = -10 to 85°C	-1.5	-	2.2	%
		T_A = 0 to 75°C	-1.3	-	2	%
		T_A = 25°C	-1.1	-	1.8	%

$T_{SU(FHSI)}$	FHSI oscillator startup time	VSS ⩽ Vin ⩽ VDD	200	-	500	ns
$I_{DD(FHSI)}$	FHSI oscillator power consumption	-	-	55	-	uA

Tab 5.2-8 Low-speed internal (LSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	20	-	40	kHz
$T_{SU(LSI)}$	LSI oscillator startup time	-	-	-	85	us
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	250	-	nA

5.2.5 PLL characteristics

Tab 5.2-9 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	1	8	16	MHz
	PLL input clock duty cycle	-	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	-	12	-	96	MHz
T_{LOCK}	PLL lock time	-	-	-	200	us
Jitter	Cycle-to-cycle jitter	-	-	-	300	ps

5.2.6 Memory characteristics

Tab 5.2-10 Memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PROG}	Page program time	-	-	2.1	-	ms
t_{ERASE}	Page erase time	-	-	6.4	-	
t_{ME}	Mass erase time	-	-	25.6	-	
IDD_{PROG}	Page program current	-	-	-	2	mA
IDD_{ERASE}	Page erase current	-	-	-	1.5	
IDD_{READ}	Read current@48MHz	-	-	-	4.7	
	Read current@24MHz	-	-	-	2.5	

Tab 5.2-11 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance	-	100	-	-	kcycles
T_{RET}	Data retention	-	10	-	-	year

5.2.7 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size is either 3 parts (cumulative mode) or 3 parts x(n + 1) supply pins (non-cumulative mode). The human body model (HBM) can be simulated. The tests are compliant with JESD22-A114/C101 standard.

Tab 5.2-12 ESD absolute maximum ratings

Symbol	Ratings	Conditions	class	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JEDEC JS-001-2017	2	2000	V
$V_{ESD(CMD)}$	Electrostatic discharge voltage (charge device mode)	T_A = +25 °C, conforming to JEDEC JS-002-2018	II	500	

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with ANSI/ESDA/JEDEC IC latch-up standard.

Tab 5.2-13 Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +25 °C, compliant with JEDEC 2016	II level A

5.2.8 EFT Characteristics

Tab 5.2-14 EFT Characteristics

Symbol	Parameter	Standard	Voltage	Class
EFT_{IO}	EFT to IO	(IEC61000-4-4)	2KV	4
EFT_{Power}	EFT to Power	(IEC61000-4-4)	4KV	4

Software suggestion

Software flow must contain code to prevent CPU run away, for example:

- Crashed Program Counter.
- Unpredicted Reset.
- Crashed important data in control register.

Increase driven strength of IOs improve the capability of EFT.

5.2.9 IO characteristics

Tab 5.2-15 IO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	-	0.65VDD	2.1	-	V
V_{IL}	Input low level voltage	-	-0.5	6.4	-	V

V_{hys}	Schmitt trigger voltage hysteresis	-	0.05VDD	25.6	-	V
I_{lkg}	Input leakage current	VSS ⩽ Vin ⩽ VDD	-	-	±1	uA
R_{pu}	Weak pull-up equivalent resistor	Vin = VSS	30	40	50	KΩ
R_{pd}	Weak pull-down equivalent resistor	Vin = VDD	30	40	50	KΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pf

Tab 5.2-16 Input/output AC characteristics

Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I/O low-speed						
$f_{max(IO)out}$	Maximum frequency	C_L = 50pf VDD=2V to 3.6V	-	-	10	MHz
$t_{f(IO)out}$	Output high to low level fall time		-	-	125	ns
$t_{r(IO)out}$	Output low to high level rise time		-	-	125	ns
I/O high-speed						
$f_{max(IO)out}$	Maximum frequency	C_L = 50pf VDD=2V to 3.6V	-	-	50	MHz
$t_{f(IO)out}$	Output high to low level fall time		-	-	25	ns
$t_{r(IO)out}$	Output low to high level rise time		-	-	25	ns

5.2.10 TIM characteristics

Tab 5.2-17 TIM characteristics

Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
$T_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution	-	-	20	bit
$t_{COUNTER}$	20-bit counter clock period when internal clock is selected	-	1	1048576	$t_{TIMxCLK}$
t_{MAX_COUNT}	Maximum possible count	-	1	65536 x 1048576	$t_{TIMxCLK}$

5.2.11 USB characteristics

Note: *Guaranteed by design, not tested in production.*

Tab 5.2-18 USB DC electrical characteristics

Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
VDD	USB operating voltage	-	3.0	3.6	V
V_{DI}	Differential input sensitivity	I(USBDP, USBDM)	0.2	-	V
V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	2.5	V
V_{SE}	Single ended receiver threshold	-	1.3	2.0	V
V_{OL}	Static output level low	1.5K resistor to 3.6V	-	0.3	V
V_{OH}	Static output level high	1.5K resistor to VSS	2.8	3.6	V

[1] To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range

Tab 5.2-19 USB full-speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time	C_L = 50pf	4	20	ns
t_f	Fall time	C_L = 50pf	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
t_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

5.2.12 ADC characteristics

Tab 5.2-20 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Power supply	-	2.4	-	3.6	V
f_s	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14MHz	-	-	823	kHz
V_{AIN}	Conversion voltage range	-	0	-	VDDA	V
R_{AIN}	External input impedance	-	-	-	200	Ω
C_{AIN}	External capacitor	-	-	TBD	-	pf
I_{lkg}	Injection current on Analog input	-	-	-	10	uA
R_{ADC}	Sampling switch resistance	-	-	-	1.4	KΩ
C_{ADC}	Internal sample and hold capacitor/12-bit	-	-	15.5	-	pf

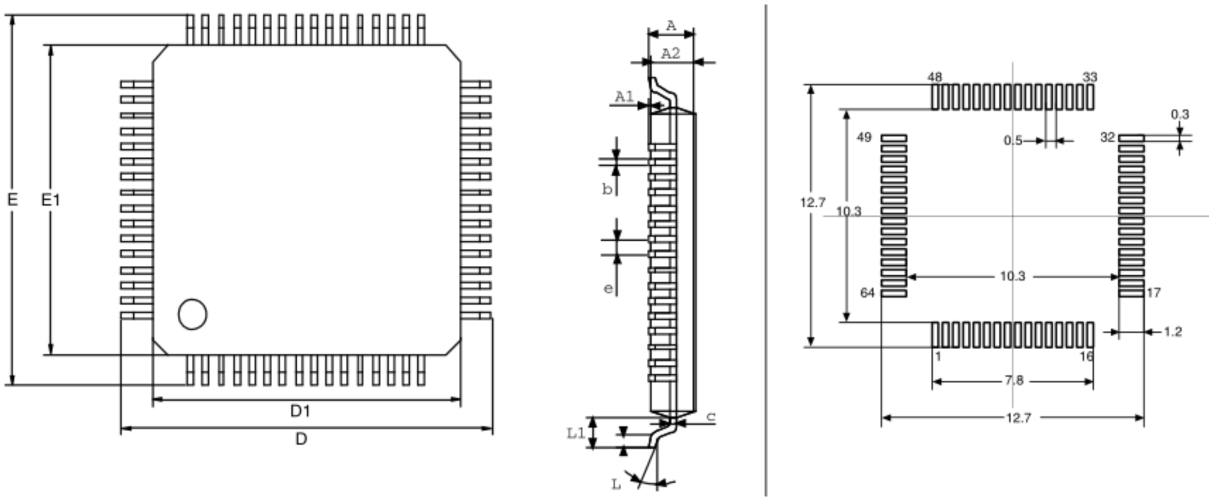
Tab 5.2-21 ADC Conversion time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{AD}	ADC clock cycle	-	62.5	-	-	ns
T_{CONV}	Conversion time	12-bit	-	$13T_{AD}$	-	ns
F_{CONV}	conversion rate	12-bit	-	-	940	KSPS
T_{SAMP}	Sampling time	12-bit	$3T_{AD}$	-	-	ns
t_{DIS}	Dis-charge time	-	-	$0.5T_{AD}$	-	ns
t_{DPU}	Power-up time	-	-	-	10	us

6 Package characteristics

6.1 LQFP64 10x10mm

Fig 6.1-1 LQFP64 10 x 10mm, 64 pin package parameters



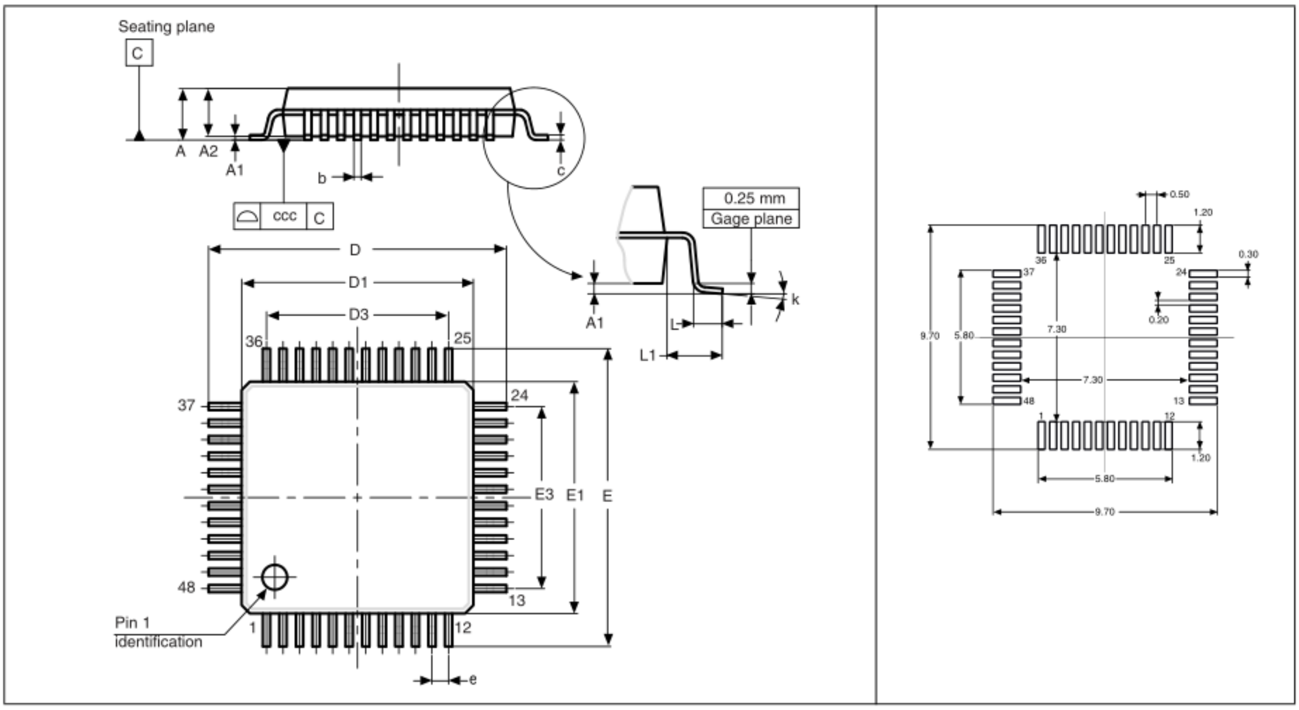
Note: *Drawing is not to scale.*

Tab 6.1-1 LQFP64, 10x20 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	**Typ**	**Max**
A	-	-	1.60
A_1	0.05	-	0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	-	12.00	-
D_1	-	10.00	-
E	-	12.00	-
E_1	-	10.00	-
e	0.50		
L	0.45	0.60	0.75
L_1	1.00		
θ	0°	3.5°	7°

6.2 LQFP48 7x7mm

Fig 6.2-1 LQFP48 7 x 7mm, 48 pin package parameters



Note: *Drawing is not to scale.*

Tab 6.2-1 LQFP48, 7x7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	**Typ**	**Max**
A	-	-	1.60
A_1	0.05	-	0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D_1	6.80	7.00	7.20
D_3	-	5.50	-
E	8.80	9.00	9.20
E_1	6.90	7.00	7.20
E_3	-	5.50	-
e	0.50		
L	0.45	0.60	0.75
L_1	1.00		
K	0°	3.5°	7°
ccc	0.08		

7 Ordering information

Fig 7.0-1 Ordering code information

WB32 F Q95 R C T 6

Device family

ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

Q95= WB32FQ95xx

Pin count

C = 48 pins
R = 64 pins

Flash memory size

C = 256 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, -40℃~85℃

Tab 7.0-1 MCU selection

Commercial Product Code	Frequency (MHz)	Core	Flash (Kbytes)	Ram (Kbytes)	Package Name	IONb	Vmin	Vmax	Nb Timer (20bit)	Nb Motor Control Timer	Nb ADC 12 bit Cell	Nb ADC Channels	Quad SPI (M)	SPI (M)	SPI (S)	I2C	UART	USB
WB32FQ95CCT6	96	Cortex-M3	256	36	LQFP48	37	2	3.6	3	1	1	10	1	1	2	2	3	1
WB32FQ95RCT6	96	Cortex-M3	256	36	LQFP64	51	2	3.6	3	1	1	16	1	1	2	2	3	1

8 Revision history

Revision	Data	Changes
01.00	2021/12/15	Draft version