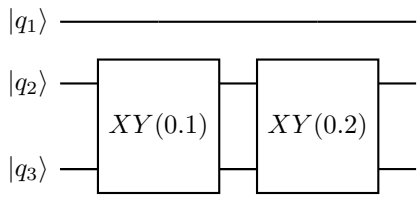
I. PROBLEM 1

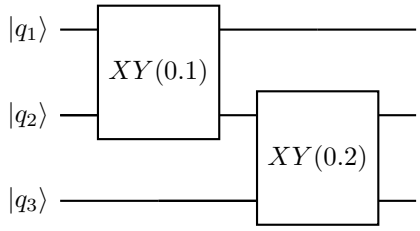
A. CIRCUIT

XY(0.1) 2 1
XY(0.2) 2 3

B. PYQUIL.LATEX OUTPUT



C. EXPECTED BEHAVIOR

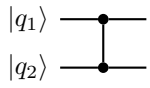


II. PROBLEM 2

A. CIRCUIT

CPHASE(0.1) 1 2

B. PYQUIL.LATEX OUTPUT



C. EXPECTED BEHAVIOR

or