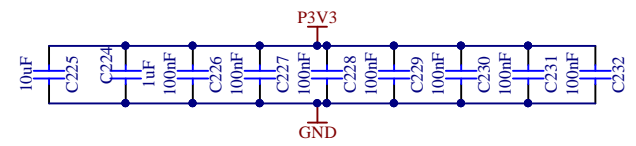


Copyright WUT ISE 2018.  
 This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (http://ohwr.org/CERNOHL). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

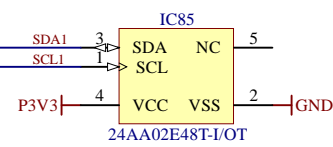
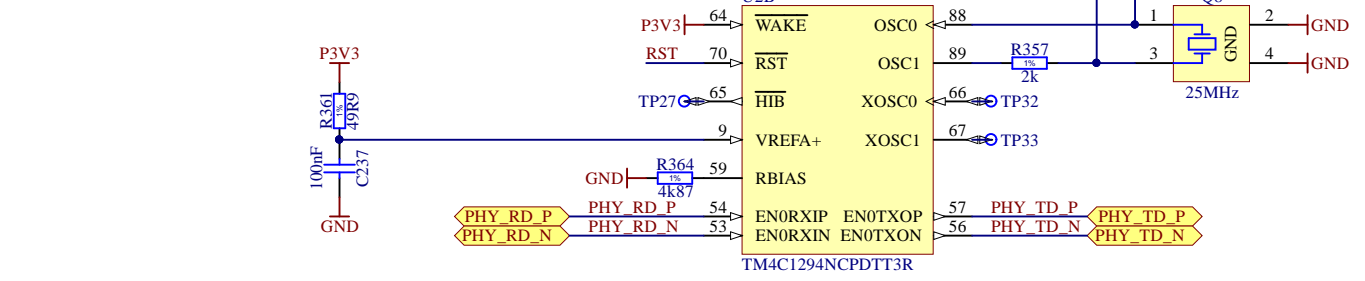
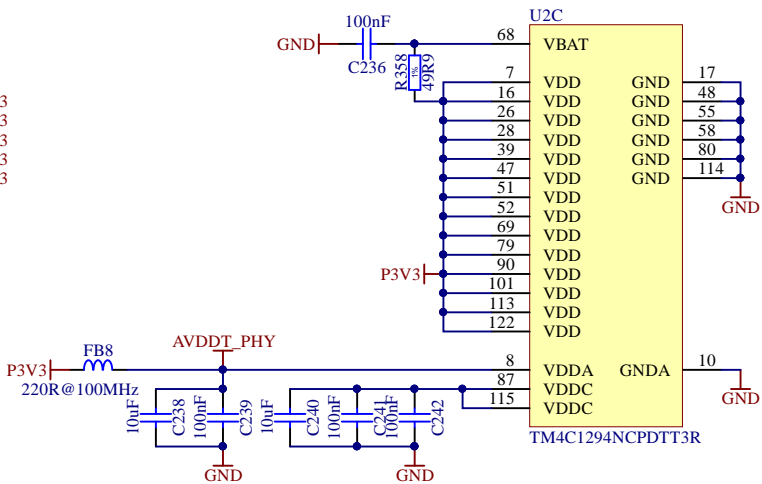
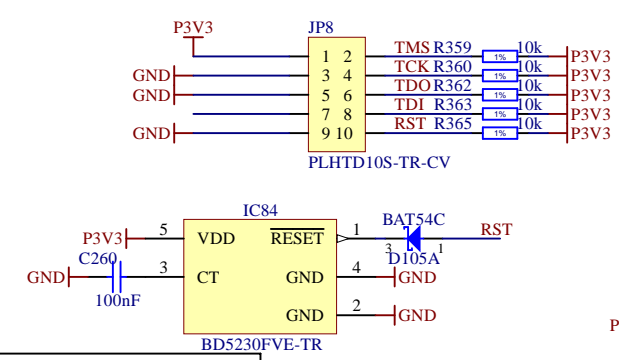
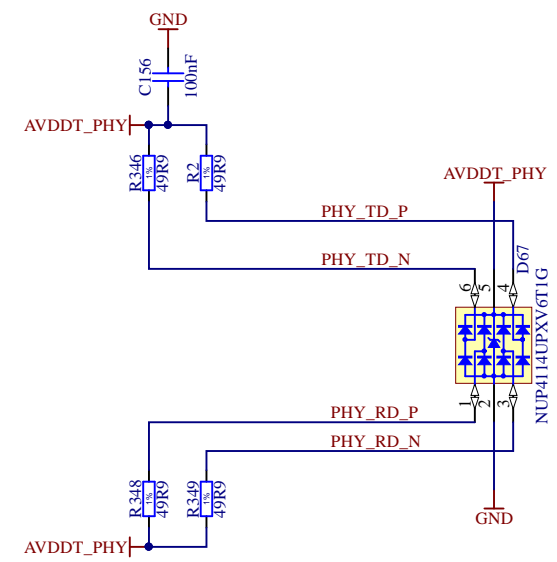
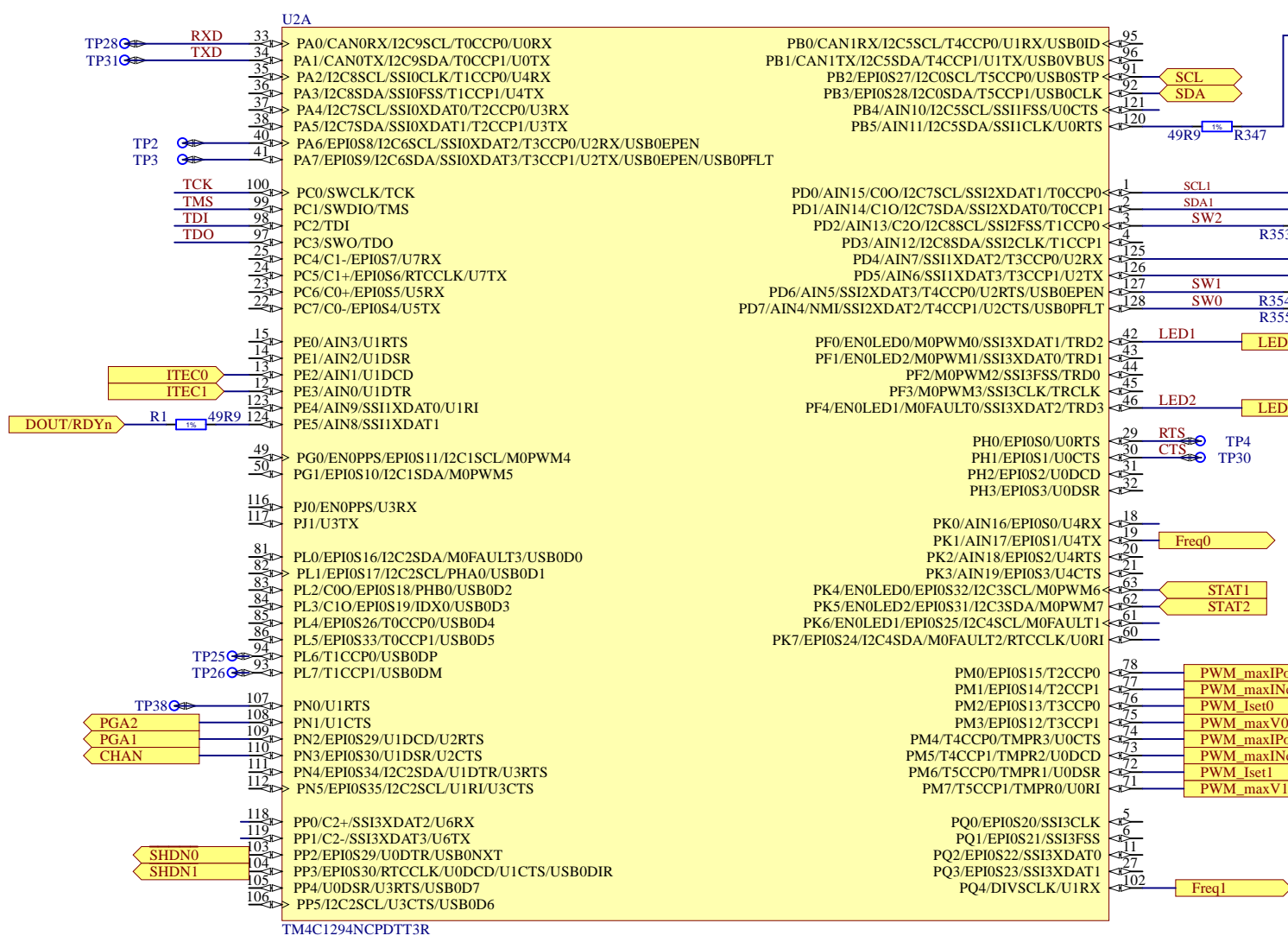


Project/Equipment		Thermostat.PrjPCB	
Document		<b>Thermostat Top v1.0</b>	
Cannot open file C:\temp\Logo-PW-duze.jpg	Designer	G.Kasprowicz	
	Drawn by	G.Kasprowicz	
	Check by	-	
	Last Mod. -	07/11/2018	
File	Thermostat.schdoc		Sheet 1 of 2
Print Date	07/11/2018 22:50:03		Size Rev
PW ISE		Contact	gkaspro@gmail.com
			A3 1.0



Port pins PM[7:4] operate as Fast GPIO pads but support only 2-, 4-, 6-, and 8-mA drive capability. Port pins PL6 and PL7 operate as Fast GPIO pads, but have 4-mA drive capability only

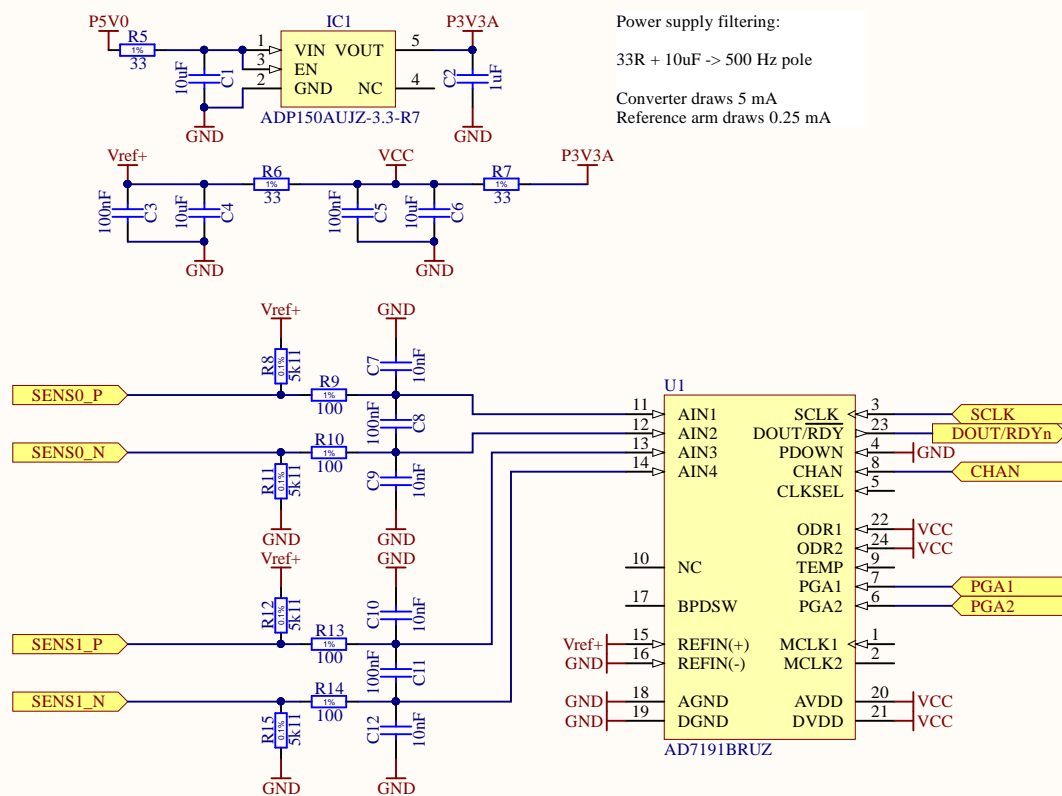
Slow GPIO : PJ1



Copyright WUT ISE 2018.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Project/Equipment		Thermostat.PrjPCB	
Document		<b>Thermostat CPU v1.0</b>	
Designer	G.Kasprowicz	Check by	-
Last Mod.	07/11/2018	Print Date	07/11/2018 22:50:03
File	CPU_ETH.SchDoc	Sheet	2 of 2
Cannot open file	C:\temp\Logo-PW-duze.jpg	Contact	gkaspro@gmail.com
PW ISE		Size	A3
		Rev	1.0



Power supply filtering:  
 33R + 10uF -> 500 Hz pole  
 Converter draws 5 mA  
 Reference arm draws 0.25 mA

Performance with a typical thermistor (R25 = 10K) :

Resolution at the gain=1, rate=10 Hz, RMS noise floor of 500 nV:  
 -50 degC to +120 degC : < 0.1 mK  
 0 degC to 35 degC : < 10 uK

Error in measured T from tempCo (5ppm) of bridge resistors:  
 0.07 mK / K @ -50 degC (thermistor)  
 0.1 mK / K @ 20 degC (thermistor)  
 0.2 mK / K @ 120 degC (thermistor)

Error from converter offset drift (150 nV / K @ gain=1):  
 < 35 uK / K (-50 degC to +120 degC thermistor)  
 2 uK / K @ 20 degC (thermistor)

Error from converter gain drift (1ppm / K):  
 1 mK / K @ -50 degC (very fast drop off to this value below -20 degC)  
 < 0.1 mK / K @ Troom > 0 degC

Total error from ambient drifts @ thermistor = 20 degC: 0.2 mK / K  
 (note that a large part of this could be removed by applying a correction calculated from the internal temperature sensor of the AD7191)

Gain drift over time: 10 ppm / 1000 hours gives < 1 mK @ Troom > 0 degC over 1000 hours

Errors from power supply noise and drift:

Supply rejection:  
 90 dB -> 30 uV / V  
 Thus 10 mV noise gives 300 nV shift -> 4 uK (nothing)

Common mode input rejection (rate=10Hz):  
 120 dB -> 1 uV / V  
 So 100 mV of 50 Hz / 60 Hz noise -> 1 uK

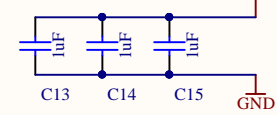
A

B

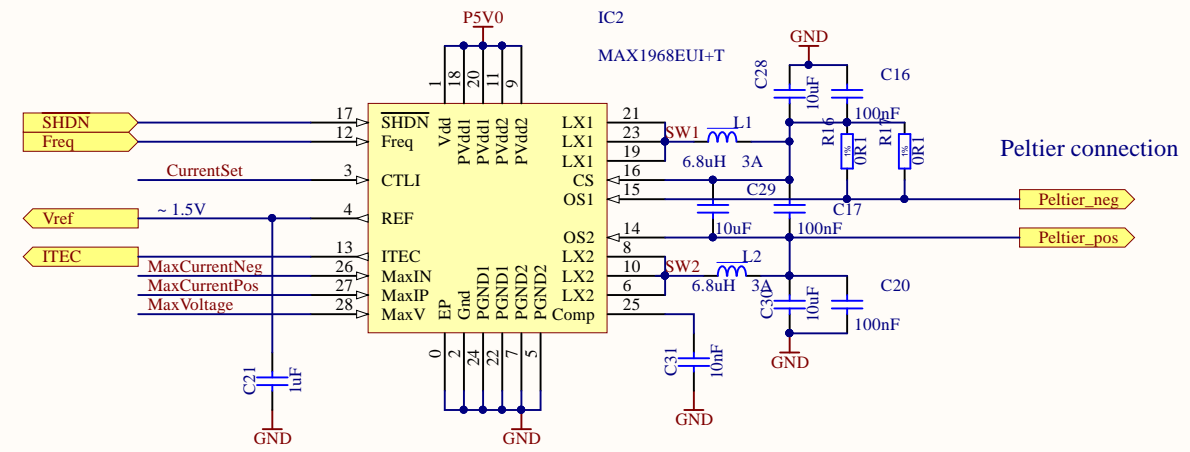
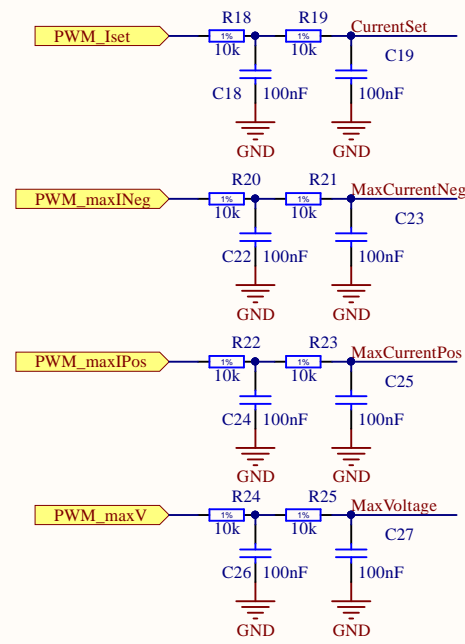
C

D

Decoupling for each of Vdd, PVdd1, PVdd2 P5V0



Freq :  
High = 1 MHz  
Low = 500 kHz

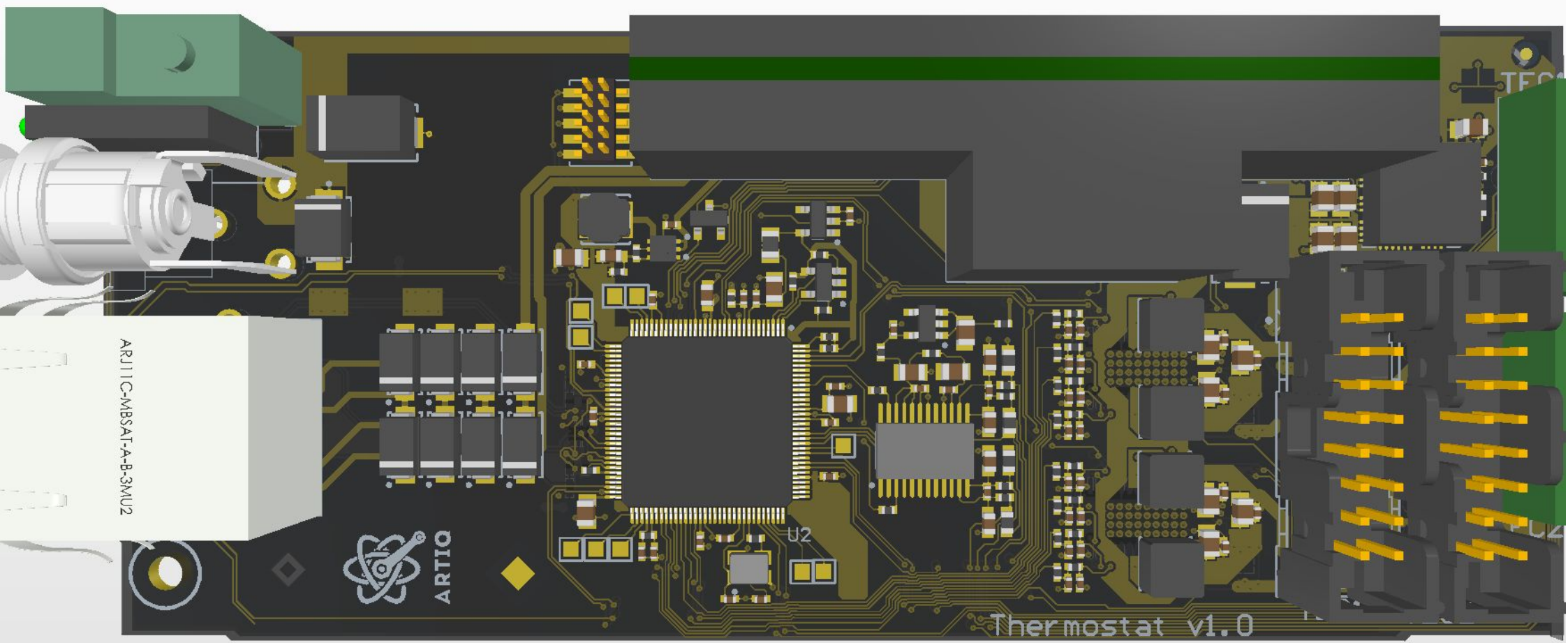


TEC current set by CTLI:  
 $I_{TEC} = 2 * (V_{CTLI} - V_{Ref})$   
 When  $V_{CTLI} > V_{Ref}$ ,  $V_{OS2} > V_{OS1}$

TEC current monitored by ITEC:  
 $V_{ITEC} = V_{Ref} + 0.4 * I_{ITEC}$

MaxIN and MaxIP set maximum negative and positive TEC currents. The limit is set by:  
 $I_{MaxP/N} = 3A * MaxIP/N / V_{Ref}$   
 i.e. to set the negative current limit to 2A set  $MaxIN = 2/3 * V_{Ref}$

MaxV sets maximum TEC voltage.  $V_{TEC\_max} = 4 * MaxV$ .  
 $MaxV \leq V_{Ref}$

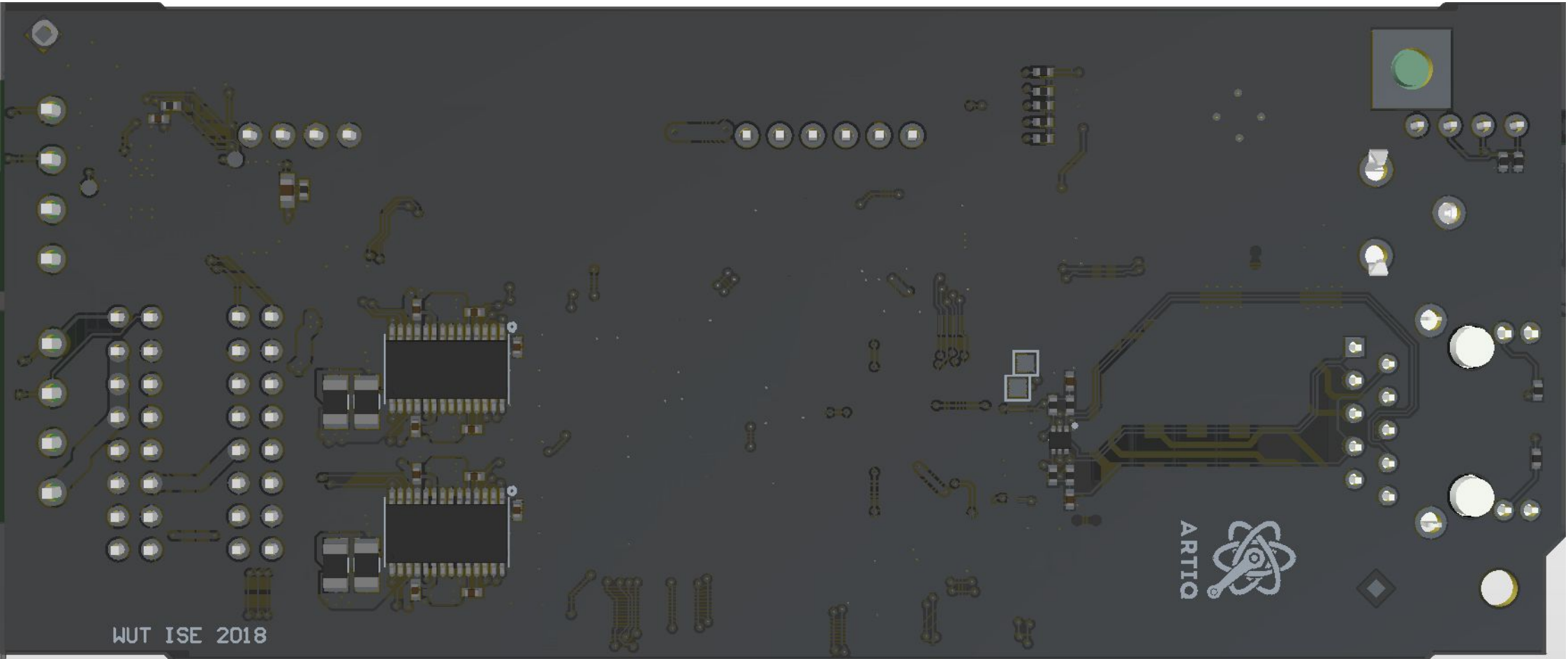


ARJ11C-MBSAT-A-B-3MU2



U2

Thermostat v1.0



WUT ISE 2018

ARTIO 

